1998

TRANSIENT VOLTAGE SUPPRESSION

HARRIS SEMICONDUCTOR

DB450.5

Transient Voltage Suppression

HARRIS
SEMICONDUCTOR

$5.00

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SEMICONDUCTOR

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Printed in USA, 2/1998

HARRIS TRANSIENT VOLTAGE SUPPRESSION DEVICES

More than ever before, today's system and equipment designers must ensure that every circuit is immune to voltage transients. This challenge results from a combination of technological, economic and legal factors:

Technological

Electrical and electronic devices are integral to the on-going activities of business, industry, government, and life in general. Businesses and consumers alike have come to expect extremely high levels of reliability from these products. However, new technology and increasing levels of complexity can make today's devices even more susceptible to electrical overstress.

Economic

Components and systems at risk from exposure to voltage transients are expensive. Many of these components control critical processes and shutdowns can have potentially devastating effects. By maintaining system functionality, adequate transient protection can minimize costs such as warranty issues.

Legal

Legislation adopted by the European Community requires that manufacturers wishing to sell products legally within the European Union must demonstrate that their products are within full compliance. Proof of compliance includes ElectroMagnetic Compatibility (EMC) testing, based upon test standards developed by the IEC. These international standards are now often referenced and specified for products intended for sale outside of Europe as well.

The products presented in this data book are designed to suppress voltage transients induced in electrical/electronic systems and circuits from common sources such as ESD, EFT, Lightning Surge, Auto Load Dump, Inductive load switching, capacitor bank switching, noise bursts, etc. Harris TVS devices are comprised of six distinct technologies in order to best fit the application and its particular transient concerns.

This data book is organized in the following manner:

- **New Products** are highlighted in Section 1.
- For those familiar with Harris TVS devices, the Section 2 **Alpha Numeric Listing** references the data sheet pages.
- Due to the breadth of the Harris TVS product portfolio, Section 3 categorizes end applications into six general **Market Segments** to aid in the selection of an appropriate device. For those not familiar with all of the technologies and products, the Market Segments provide examples of the Harris TVS device Series that is most often chosen or likely to be suited to that specific function or application.
- The core of the book is comprised of the Harris Transient Voltage Suppression Device **Data Sheets**, segregated by device Series in Sections 4 through 10.
- A comprehensive **Application Note** Section 11 supports each technology and device Series.
- Harris **Quality and Reliability** methods and procedures are explained in Section 12.

For complete, current and detailed technical specifications on any Harris devices, please contact the nearest Harris sales, representative or distributor office, listed in Section 14; or direct literature requests to:

Harris Semiconductor Data Services Department
P.O. Box 883, MS 53-204
Melbourne, FL 32902
Phone: 1-800-442-7747
Fax: 407-724-7240

For a complete listing of all Harris Semiconductor products, please refer to the Product Selection Guide (PSG201; ordering information above).

All Harris Semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.

HARRIS
SEMICONDUCTOR

TRANSIENT VOLTAGE SUPPRESSION

FOR COMMERCIAL AND MILITARY APPLICATIONS

CECC

CANADIAN STANDARDS ASSOCIATION

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I.S./ISO 9000/EN 29000

UNDERWRITERS LABORATORY

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TVS 1

NEW PRODUCTS

To address the changing application needs for transient voltage suppression, Harris has developed and brought to market a number of new products.

Highlighted in this section is a brief description of these new devices, extensions of existing products and other new enhancements to the Harris Transient Voltage Suppression Devices portfolio.

These new products and innovations are intended to:

- **Offer the designer more options in order to help protect today's electrical/electronic components and circuits.**
- **Provide the transient voltage suppression required to ensure ElectroMagnetic Compatibility (EMC) in those systems that must meet various safety standards or international legislated compliance.**
- **Provide the device performance levels required of the TVSS product industry.**

UltraMOV™

Harris has introduced a new series of Varistors called "UltraMOV™". These devices, intended for AC line applications, offer high peak current and energy capability in the 7, 10, 14, and 20mm size radial lead packages. Standard operating voltage ratings are from 130V to 625V_{RMS} for most single, split, and three phase AC applications. With peak current ratings up to a true 10kA (20mm, 8x20μs), these devices offer new options for the TVSS OEM in meeting surge requirements such as specified in the new UL1449 (revision 2) and are ideal for new designs, or existing designs presently using the Harris LA or C-III Series of radial MOVs. The data sheet is provided in Section 4.

Gas Discharge Tubes

Harris has expanded its suppression device portfolio with the introduction of its Gas Discharge Tube products. The high surge current capability and low insertion capacitance properties of the GDT technology make it well suited to applications such as telephone line, CATV, high voltage power supplies, antenna stations, and certain AC line applications. Harris offers five distinct series, leaded and non-leaded versions in industry recognized package outlines, and UL recognition were applicable. GDT data sheets are found in Section 7 and supportive application notes in Section 11.

SP723

The Integrated Protection series of IC Arrays is expanded with the addition of this higher rated type. The same patented SCR/Diode structure of the other SP Series devices is used however, the SP723 is specifically designed and rated to withstand the IEC 1000-4-2 model for ESD testing to level 4 (15kV air discharge/8kV contact discharge), as well as MIL-STD-3015.7 to 25kV.

As with the SP720 and 721 types, the SP723 is applied to protect other Silicon devices, operating up to 35VDC, on data, signal and control lines, but to very harsh ESD conditions. The SP723 is supplied in 8 lead PDIP or SOIC packages to protect up to 6 lines. Data sheets are shown in Section 6 with supplemental Application Notes in Section 11.

MLE Series

This special version of our Multilayer Series of leadless chips was specifically designed for ESD and low pass filter applications. The MLE Series is offered in 0603, 0805, and 1206 chip sizes for operation from 3.5V_{DC} to 18V_{DC}. These devices are rated to the IEC 1000-4-2 ESD level 4 (15kV air discharge, 8kV contact discharge) and, therefore, can help products meet EMC compliance. The MLE series finds application on power supply, signal/control lines, and across components subject to ESD. The inherent capacitance of this Multilayer device makes it suited to filter applications, therefore, high frequency impedance characteristics are rated as well. Section 5 contains the Multilayer data sheets.

New ML Series Types and Extended Voltage Types

Dielectric material and process advances have made possible the addition of higher voltage ML Series Multilayer Suppressors, extending the working voltage operating range of this Series. The 1210 chip size will now offer standard $85V_{DC}$ and $120V_{DC}$ devices.

Additionally, twelve new standard types have been introduced that will offer specific working voltages from $9V_{DC}$ through $60V_{DC}$ in specific sizes of either 0603, 0805, or 1210.

A new 1206 sized chip is now included with the 1210, 1812, and 2220 sizes of the automotive AUML Series.

As with all of our Multilayer families, custom voltage, capacitance and energy types can be manufactured for specific customer requirements. See Section 5 for the complete ML data sheet and Section 11 for associated application notes.

Nickel Barrier End Terminations for Multilayers

Harris has developed the world's first Nickel barrier end termination finish for Multilayer Suppressors. The Nickel barrier process has been used by other components such as leadless capacitors for some time, but due to the materials that make up the Multilayer Suppressor, a special process had to be developed and proven. This new Nickel/Tin option offers an alternative to the standard Harris Silver finish. It is intended for use in the prevention of material leaching under harsh wave solder or solder rework situations, or where the use of Silver is precluded. Read more about the attributes of this option in the Harris Multilayer data sheets in Section 5.

New Options for CA Series Varistor Discs

The CA Series of unencapsulated disc varistors are offered for the customer who desires to provide special lead assembly such as soldered terminals or pressure contact terminals. Harris now offers two metallization options for this series. One is a screened-on sintered Silver. The second is an arc-sprayed aluminum. Additionally, these discs may now be ordered with or without the resistive edge passivation.

The CA Series is supplied in 32, 40, and 60mm round disc form. Data sheets are provided in Section 4.

SPICE/PSPICE™ Models for Varistor Products and Multilayer Products

As an aid to the circuit designer Harris will provide, on request, SPICE/PSPICE design models for devices in these product families. Harris models include both "standby region" as well as "clamping region" performance characteristics for a fully representative V-I model. Contact Harris Sales for specific type requests.

PSPICE™ is a trademark of MicroSim Corporation.

TVS 2

GENERAL INFORMATION

2 GENERAL INFORMATION

Alpha Numeric Product Index

Product Index by Family

VARISTOR PRODUCTS

TVS 3

MARKET SEGMENT SELECTION GUIDE

PAGE

Market Segment Selection Guide

This section is intended to be a guide in the initial selection phase of a Transient Voltage Suppression device for users who may not be familiar with the Harris product offerings. Highlighted are the different product Series and the circuits and products (Market Segments) to which they are most often applied. Selection consideration based on EMC is also introduced.

Harris Suppression Devices

Numerous studies have documented the many causes, various energy levels and wave shapes of voltage transients. These common, real-world events raise the need for suppression devices in order to maintain safety, ensure reliable systems operation and prevent electrical interference.

Due to the varied nature of the over-voltage transient, it is understandable that no single suppression device or technology can best address each event in every application. It is for this reason that, as a leading supplier of suppression devices, Harris makes available to the circuit designer the broad variety of devices described in this data book. The Harris Suppression portfolio is comprised of six different product families of various technologies:

- Metal Oxide Varistors
- Multilayer Suppressors
- Integrated SCR/Diode Arrays
- Gas Discharge Tubes
- Surgector Thyristor/Zeners
- Arresters

A "Market Segment" Selection Approach

As part of the selection process to help match a particular Harris device to a specific application, a diverse number of electrical and electronic circuit examples have been grouped into six general categories, creating "Market Segments". These Market Segments encompass most products utilizing transient protection devices and are listed below and in the adjacent Selection Guide table.

- Low Voltage Board-Level Products
- AC Line and TVSS Products
- Automotive Electronic Products
- Telecommunications Products
- Industrial High Energy AC Products
- Arrester Products

In essence, each of the Harris devices can be "targeted" to one or more of the Market Segments as shown in the Selection Guide table. While the designer is not constrained to the device Series provided in the table, these suggestions offer the most likely products as a first consideration.

The Selection Guide table further identifies the Harris device technology, the data book section in which the specific data sheets are located, and surface mount package availability.

As shown, different product Series can be applied to a given Market Segment, offering the designer choices in the unique characteristics of a specific technology, electrical ratings and performance, or package style.

Transient Voltage Suppressor Device Selection Guide

MARKET SEGMENT	TYPICAL APPLICATIONS AND CIRCUITS EXAMPLES	DEVICE FAMILY OR SERIES	DATA BOOK SECTION	TECHNOLOGY	SURFACE MOUNT PRODUCT?
Low Voltage, Board Level Products	• Hand-Held/Portable Devices • EDP • Computer • I/O Port and Interfaces • Controllers • Instrumentation • Remote Sensors • Medical Electronics, etc.	CH	4	MOV	✔
		MA, ZA, RA	4	MOV	
		ML, MLE	5	Multilayer Suppressor	✔
		SP72X	6	SCR/Diode Array	✔ †
AC Line, TVSS Products	• UPS • AC Panels • AC Power Taps • TVSS Devices • AC Appliance/Controls • Power Meters • Power Supplies • Circuit Breakers • Consumer Electronics	UltraMOV™, "C" III, LA, HA, RA	4	MOV	
		CH	4	MOV	✔
		GDT	7	Gas Discharge Tube	
Automotive Electronics	• ABS • EEC • Instrument Cluster • Air Bag • Window Control • Wiper Modules • Multiplex Bus • EFI	CH	4	MOV	✔
		ZA	4	MOV	
		AUML, ML	5	Multilayer Suppressor	✔
		SP72X	6	SCR/Diode Array	✔ †
Telecommunications Products	• Cellular/Cordless Phone • Modems • Secondary Phone Line Protectors • Data Line Connectors • Repeaters • Line Cards	CH	4	MOV	✔
		CP, CS, ZA	4	MOV	
		ML, MLE	5	Multilayer Suppressor	✔
		SP72X	6	SCR/Diode Array	✔ †
		GDT	7	Gas Discharge Tube	
		Surgector	8	Thyristor/Zener	
Industrial, High Energy AC Products	• High Current Relays • Solenoids • Motor Drives • AC Distribution Panels • Robotics • Large Motors	DA/DB, BA/BB, CA, HA, NA, PA	4	MOV	
		GDT	7	Gas Discharge Tube	
Arrester Products	• Lightning Arrester Assemblies for High Voltage AC Power Distribution Lines and Utility Transformers	AS	9	MOV	

† Available in both surface mount and through-hole packages.

UltraMOV™ is a trademark of Harris Corporation.

EMC and Device Selection

Electrical products or systems that are immune to voltage transients within their intended application, and do not propagate transients themselves, are said to have ElectroMagnetic Compatibility or EMC. Often today, products must demonstrate compliance of EMC through applicable testing. (See application note AN9734.) These tests are derived from standards developed by industry-recognized engineering, testing and safety organizations throughout the world including the IEC, IEEE, VDE, UL, CSA, CENELEC, AEC and NEMA.

An example of the importance of achieving EMC is exemplified through the legislation enacted for compliance within the European Union as part of the mandatory "CE" marking program.

Products manufactured in each of the Market Segments of the table above have various transient voltage test standards associated with them. And, therefore, could be subject to EMC compliance. Depending upon the application, these tests are based on sources that can include:

- Lightning
- Inductive Load Switching sources such as solenoids, motors, alternator load dump, transformers, etc.
- ESD
- Relay contact/circuit breaker operation noise

Selection of a suppression device for installation within a product would ideally occur during its initial design phase, but also occurs when finished products fail to meet compliance testing. In either case, the designer would:

- Identify the applicable EMC tests and conditions for the product.
- Match the test criteria to suitable suppression device families/technologies.
- Make a final selection based upon suppression device performance/parametric limits and product sensitivity level or needs such as package style, form factor, etc.
- Verify product compliance through testing.

See the Harris Application Notes in Section 11 for detailed information and further guidance in device selection.

TVS 4

VARISTOR PRODUCTS

UltraMOV™ is a trademark of Harris Corporation.

Varistor Products Overview

The **M**etal **O**xide **V**aristor (MOV) components listed in this section are intended for a comprehensive range of applications and transient voltage suppression products. These devices find usage in 5 of the 6 electrical/electronic Market Segments described in Section 3 and and in the Transient Voltage Suppressor Device Selection Guide below.

The product series in this section vary in size, form factor, and package style as illustrated in Figure 1 in order to meet specific performance as well as manufacturing needs of the user.

Additionally, Figure 2 forms a selection guide matrix for the designer by illustrating the various device's working voltage transient energy and peak current ratings range.

The data sheets in this section have been grouped by package style and are presented in the following sequence:

- Radial Lead Styles
  - UltraMOV, LA, "C" III and ZA Series
- High Energy Industrial Varistors
  - BA/BB, DA/DB and HA Series
- High Energy Industrial Varistor Discs
  - CA and NA Series
- Other Application Specific Varistors
  - CH, CP, CS, MA, PA and RA Series

See Section 11 for comprehensive varistor application note support.

Transient Voltage Suppressor Device Selection Guide

MARKET SEGMENT	TYPICAL APPLICATIONS AND CIRCUITS EXAMPLES	DEVICE FAMILY OR SERIES	DATA BOOK SECTION	TECHNOLOGY	SURFACE MOUNT PRODUCT?
Low Voltage, Board Level Products	• Hand-Held/Portable Devices • EDP • Computer • I/O Port and Interfaces • Controllers • Instrumentation • Remote Sensors • Medical Electronics, etc.	**CH**	**4**	**MOV**	✔
		MA, ZA, RA	**4**	**MOV**	
		ML, MLE	5	Multilayer Suppressor	✔
		SP72X	6	SCR/Diode Array	✔ †
AC Line, TVSS Products	• UPS • AC Panels • AC Power Taps • TVSS Devices • AC Appliance/Controls • Power Meters • Power Supplies • Circuit Breakers • Consumer Electronics	**UltraMOV™, "C" III, LA, HA, RA**	**4**	**MOV**	
		CH	**4**	**MOV**	✔
		GDT	7	Gas Discharge Tube	
Automotive Electronics	• ABS • EEC • Instrument Cluster • Air Bag • Window Control • Wiper Modules • Multiplex Bus • EFI	**CH**	**4**	**MOV**	✔
		ZA	**4**	**MOV**	
		AUML, ML	5	Multilayer Suppressor	✔
		SP72X	6	SCR/Diode Array	✔ †
Telecommunications Products	• Cellular/Cordless Phone • Modems • Secondary Phone Line Protectors • Data Line Connectors • Repeaters • Line Cards	**CH, CP, CS, ZA**	**4**	**MOV**	
		ML, MLE	5	Multilayer Suppressor	✔
		SP72X	6	SCR/Diode Array	✔ †
		GDT	7	Gas Discharge Tube	
		Surgector	8	Thyristor/Zener	
Industrial, High Energy AC Products	• High Current Relays • Solenoids • Motor Drives • AC Dist. Panels • Robotics • Large Motors	**DA/DB, BA/BB, CA, HA, NA, PA**	**4**	**MOV**	
		GDT	7	Gas Discharge Tube	
Arrester Products	• Arrester Assemblies for AC Power Distribution Lines and Transformers	AS	9	MOV	

†Available in both surface mount and through-hole packages.

Varistor Products Overview

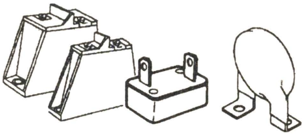
UltraMOV/"C"III/LA SERIES

- Radial Package
- AC Line Voltage Operation
- UL/CSA Recognized
- CECC Certified

ZA SERIES

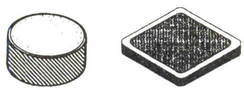
- Radial Package
- Low Voltage Operation
- UL/CSA Recognized
- CECC Certified

BB, BA, DA, DB, HA SERIES



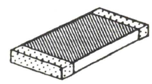
- High Energy Capability
- Rigid Terminals
- Improved Creep and Strike
- Isolated
- Low Inductance
- UL/CSA Recognized

CA, NA SERIES



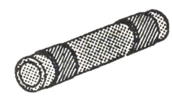
- Industrial Discs
- Solderable Contacts
- Edge Passivation

CH SERIES



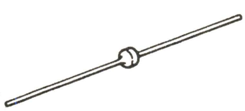
- Wide Voltage Range
- Leadless Chip
- Saves on Board Space
- UL/CSA Recognized

CP/CS SERIES CONNECTOR PIN VARISTORS



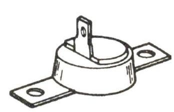
- Provides Protection in Connectors
- 22, 20 and 16 Pin Gauge Size
- Rad Hard
- Compact Size
- Solderable

MA SERIES



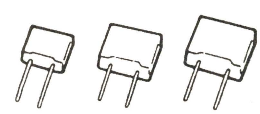
- Axial Package
- Wide Voltage Range
- 3mm Disc

PA SERIES



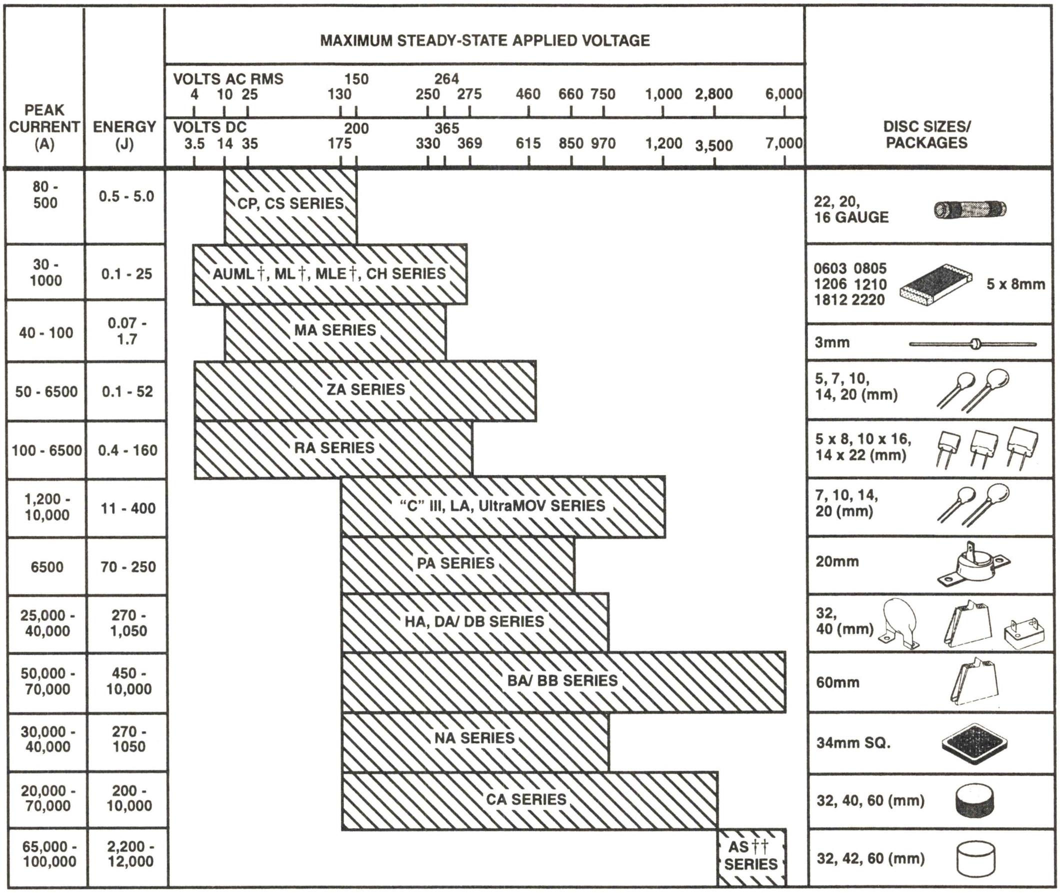
- Rigid Mountdown
- NEMA Creep and Strike Distance
- Quick Connect Terminal
- UL/CSA Recognized

RA SERIES



- Low Profile
- High Temperature Capability
- In-Line Leads
- Precise Seating Plane
- UL/CSA Recognized

FIGURE 1. VARISTOR PRODUCTS PACKAGE STYLES



†See Multilayer Section.
††See Arrester Section.

FIGURE 2. VARISTOR PRODUCT FAMILY SELECTION GUIDE

HARRIS SEMICONDUCTOR

UltraMOV™ Series

February 1998

High Energy Radial Lead Metal Oxide Varistors

Features

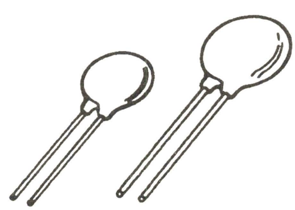
- High Peak Surge Current Rating (I_{TM}) Up to 10kA, Single 8 x 20 Pulse, 20mm
- High Energy Ratings (W_{TM})
- UL Recognized Component Listing to Safety Standard UL1449, Rev 2 (Pending)
- CSA Certification to Standard C22.2, NO.1 (Pending)
- VDE Listing (Pending)
- CECC Certified (42201- 006) (Pending)
- Standard Operating Voltage Range Compatible with Common AC Line Voltages (130VAC to 625VAC)
- Characterized for Maximum Standby Current (Leakage)
- Custom Voltage Types Available
- Standard Lead Form and Lead Space Options

Description

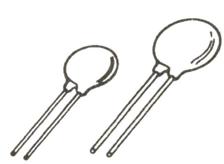
The UltraMOV Series of Metal Oxide Varistors is designed for applications requiring high peak surge current ratings and high energy absorption capability. UltraMOVs are primarily intended for use in AC Line Voltage applications such as Transient Voltage Surge Suppressors (TVSS), Uninterruptable Power Supplies (UPS), AC Power Taps, AC Power Meters, or other products that require voltage clamping of high transient surge currents from sources such as lightning, inductive load switching, or capacitor bank switching.

These devices are produced in radial lead package sizes of 7, 10, 14, and 20mm and offered in a variety of lead forms. UltraMOVs are manufactured with recognized epoxy encapsulation and are rated for ambient temperatures up to 85^{o}C with no derating. This Series is LASER-branded and is supplied in bulk, ammo pack (fan-fold), or tape and reel packaging. UltraMOVs also follow a different part number nomenclature than other Harris radial lead MOV Series.

Packaging



14mm, 20mm



7mm, 10mm

Absolute Maximum Ratings

For ratings of individual members of a series, see Device Ratings and Specifications chart

	ULTRAMOV SERIES	UNITS
Continuous:		
Steady State AC Voltage Range ($V_{M(AC)}$ RMS)	130 to 625	V
Transient:		
Single-Pulse Peak Current (I_{TM}) 8x20µs Wave (See Figure 2)	1,750 to 10,000	A
Single-Pulse Energy Range (W_{TM}) 2ms Square Wave	12.5 to 720	J
Maximum Temporary Overvoltage of $V_{M(AC)}$		
5 Minutes at 25°C	130	%
5 Minutes at 125°C	125	%
Operating Ambient Temperature Range (T_A)	-55 to 85	°C
Storage Temperature Range (T_{STG})	-55 to 125	°C
Temperature Coefficient (αV) of Clamping Voltage (V_C) at Specified Test Current	<0.01	%/°C
Hi-Pot Encapsulation Isolation Voltage Capability, Per MIL-STD-202, Method 301	2500	V

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Device Ratings and Specifications

MODEL NUMBER	DEVICE MODEL NUMBER BRANDING	MAXIMUM RATING (85°C)					SPECIFICATIONS (25°C)				
		CONTINUOUS		TRANSIENT			VARISTOR VOLTAGE AT 1mA DC TEST CURRENT		MAXIMUM CLAMPING VOLTAGE 8 x 20µs		TYPICAL CAPACITANCE
		RMS VOLTS	DC VOLTS	ENERGY 2ms	PEAK CURRENT 8 x 20µs						
		$V_{M(AC)}$	$V_{M(DC)}$	W_{TM}	I_{TM} 2 x PULSE	I_{TM} 1 x PULSE	V_{NOM} MIN	V_{NOM} MAX	V_C	I_{PK}	f = 1MHz
		(V)	(V)	(J)	(A)	(A)	(V)		(V)	(A)	(pF)
V07E130	7V130	130	170	12.5	1200	1750	184	226	340	10	180
V10E130	10V130	130	170	25	2500	3500	184	226	340	25	450
V14E130	14V130	130	170	50	4500	6000	184	226	340	50	1000
V20E130	20V130	130	170	100	6500	10000	184	226	340	100	1900
V07E140	7V140	140	180	13.5	1200	1750	200	240	360	10	160
V10E140	10V140	140	180	27.5	2500	3500	200	240	360	25	400
V14E140	14V140	140	180	55	4500	6000	200	240	360	50	900
V20E140	20V140	140	180	110	6500	10000	200	240	360	100	1750
V07E150	7V150	150	200	15	1200	1750	216	264	395	10	150
V10E150	10V150	150	200	30	2500	3500	216	264	395	25	360
V14E150	14V150	150	200	60	4500	6000	216	264	395	50	800
V20E150	20V150	150	200	120	6500	10000	216	264	395	100	1600
V07E175	7V175	175	225	17	1200	1750	243	297	455	10	130
V10E175	10V175	175	225	35	2500	3500	243	297	455	25	350
V14E175	14V175	175	225	70	4500	6000	243	297	455	50	700
V20E175	20V175	175	225	135	6500	10000	243	297	455	100	1400
V07E230	7V230	230	300	20	1200	1750	324	396	595	10	100
V10E230	10V230	230	300	42	2500	3500	324	396	595	25	250
V14E230	14V230	230	300	80	4500	6000	324	396	595	50	550
V20E230	20V230	230	300	160	6500	10000	324	396	595	100	1100

Device Ratings and Specifications (Continued)

MODEL NUMBER	DEVICE MODEL NUMBER BRANDING	MAXIMUM RATING (85°C) CONTINUOUS RMS VOLTS $V_{M(AC)}$ (V)	DC VOLTS $V_{M(DC)}$ (V)	TRANSIENT ENERGY 2ms W_{TM} (J)	PEAK CURRENT 8 x 20µs I_{TM} 2 x PULSE (A)	I_{TM} 1 x PULSE (A)	SPECIFICATIONS (25°C) VARISTOR VOLTAGE AT 1mA DC TEST CURRENT V_{NOM} MIN (V)	V_{NOM} MAX (V)	MAXIMUM CLAMPING VOLTAGE 8 x 20µs V_C (V)	I_{PK} (A)	TYPICAL CAPACITANCE f = 1MHz (pF)
V07E250	7V250	250	320	25	1200	1750	351	429	650	10	90
V10E250	10V250	250	320	50	2500	3500	351	429	650	25	220
V14E250	14V250	250	320	100	4500	6000	351	429	650	50	500
V20E250	20V250	250	320	170	6500	10000	351	429	650	100	1000
V07E275	7V275	275	350	28	1200	1750	387	473	710	10	80
V10E275	10V275	275	350	55	2500	3500	387	473	710	25	200
V14E275	14V275	275	350	110	4500	6000	387	473	710	50	450
V20E275	20V275	275	350	190	6500	10000	387	473	710	100	900
V07E300	7V300	300	385	30	1200	1750	423	517	775	10	70
V10E300	10V300	300	385	60	2500	3500	423	517	775	25	180
V14E300	14V300	300	385	125	4500	6000	423	517	775	50	400
V20E300	20V300	300	385	250	6500	10000	423	517	775	100	800
V07E320	7V320	320	420	32	1200	1750	459	561	840	10	65
V10E320	10V320	320	420	67	2500	3500	459	561	840	25	170
V14E320	14V320	320	420	136	4500	6000	459	561	840	50	380
V20E320	20V320	320	420	273	6500	10000	459	561	840	100	750
V07E385	7V385	385	505	36	1200	1750	558	682	1025	10	60
V10E385	10V385	385	505	75	2500	3500	558	682	1025	25	160
V14E385	14V385	385	505	150	4500	6000	558	682	1025	50	360
V20E385	20V385	385	505	300	6500	10000	558	682	1025	100	700
V07E420	7V420	420	560	40	1200	1750	612	748	1120	10	55
V10E420	10V420	420	560	80	2500	3500	612	748	1120	25	140
V14E420	14V420	420	560	160	4500	6000	612	748	1120	50	300
V20E420	20V420	420	560	320	6500	10000	612	748	1120	100	600
V07E440	7V440	440	585	44	1200	1750	643	787	1180	10	50
V10E440	10V440	440	585	85	2500	3500	643	787	1180	25	130
V14E440	14V440	440	585	170	4500	6000	643	787	1180	50	260
V20E440	20V440	440	585	340	6500	10000	643	787	1180	100	500
V07E460	7V460	460	615	48	1200	1750	675	825	1240	10	45
V10E460	10V460	460	615	90	2500	3500	675	825	1240	25	120
V14E460	14V460	460	615	180	4500	6000	675	825	1240	50	220
V20E460	20V460	460	615	360	6500	10000	675	825	1240	100	400
V10E510	10V510	510	670	80	2500	3500	738	902	1355	25	110
V14E510	14V510	510	670	165	4500	6000	738	902	1355	50	200
V20E510	20V510	510	670	325	6500	10000	738	902	1355	100	350

Device Ratings and Specifications (Continued)

MODEL NUMBER	DEVICE MODEL NUMBER BRANDING	MAXIMUM RATING (85°C) CONTINUOUS RMS VOLTS $V_{M(AC)}$ (V)	DC VOLTS $V_{M(DC)}$ (V)	TRANSIENT ENERGY 2ms W_{TM} (J)	PEAK CURRENT 8 x 20µs I_{TM} 2 x PULSE (A)	I_{TM} 1 x PULSE (A)	SPECIFICATIONS (25°C) VARISTOR VOLTAGE AT 1mA DC TEST CURRENT V_{NOM} MIN (V)	V_{NOM} MAX (V)	MAXIMUM CLAMPING VOLTAGE 8 x 20µs V_C (V)	I_{PK} (A)	TYPICAL CAPACITANCE f = 1MHz (pF)
V10E550	10V550	550	745	90	2500	3500	901	1001	1500	25	100
V14E550	14V550	550	745	180	4500	6000	901	1001	1500	50	180
V20E550	20V550	550	745	360	6500	10000	901	1001	1500	100	300
V10E625	10V625	625	825	100	2500	3500	900	1100	1650	25	90
V14E625	14V625	625	825	200	4500	6000	900	1100	1650	50	160
V20E625	20V625	625	825	400	6500	10000	900	1100	1650	100	250

NOTE:

1. Average power dissipation of transients should not exceed 0.25W, 0.4W, 0.6W and 1.0W for 7mm, 10mm, 14mm, and 20mm model sizes, respectively.

Power Dissipation Ratings

Continuous power dissipation capability is not an applicable parameter for a transient suppressor. When transients occur in rapid succession, the average power dissipation is the energy (watt-seconds) per pulse times the number of pulses per second. The power so developed must be within the specifications shown on the Device Ratings and Specifications table for the specific device. Furthermore, the operating values need to be derated at high temperatures as shown in Figure 1. Because varistors can only dissipate a relatively small amount of average power they are, therefore, not suitable for repetitive applications that involve substantial amounts of average power dissipation.

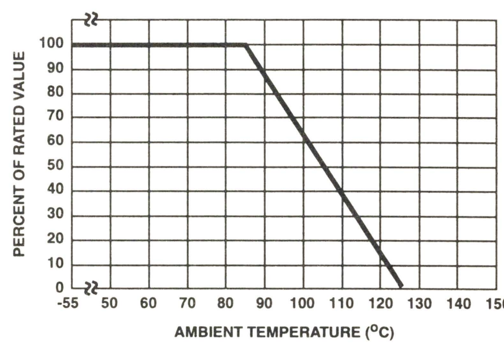
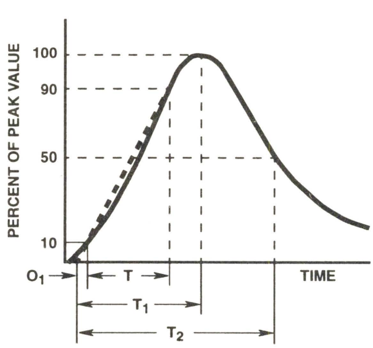


FIGURE 1. CURRENT, ENERGY AND POWER DERATING CURVE



O_1 = Virtual Origin of Wave
T = Time From 10% to 90% of Peak
T_1 = Virtual Front time = 1.25 • t
T_2 = Virtual Time to Half Value (Impulse Duration)
Example: For an 8/20µs Current Waveform:
8µs = T_1 = Virtual Front Time
20µs = T_2 = Virtual Time to Half Value

FIGURE 2. PEAK PULSE CURRENT TEST WAVEFORM

Transient V-I Characteristic Curves

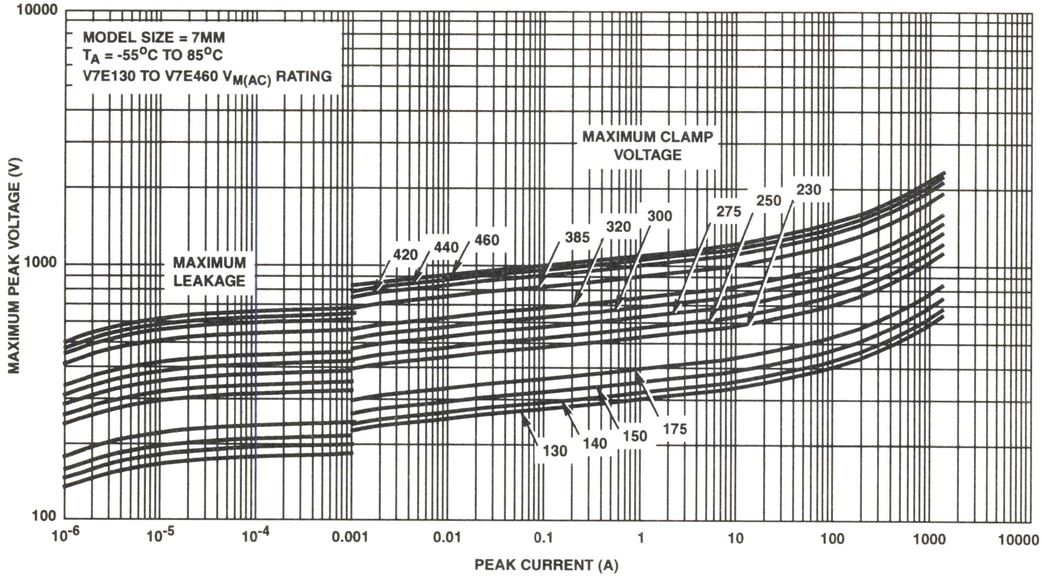


FIGURE 3.

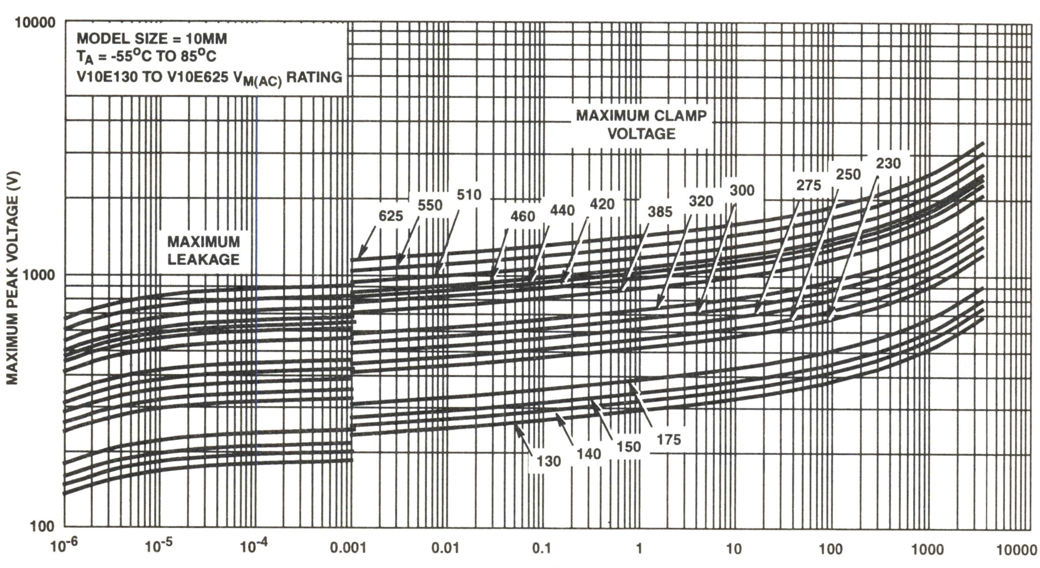


FIGURE 4.

4

VARISTOR PRODUCTS

Transient V-I Characteristic Curves (Continued)

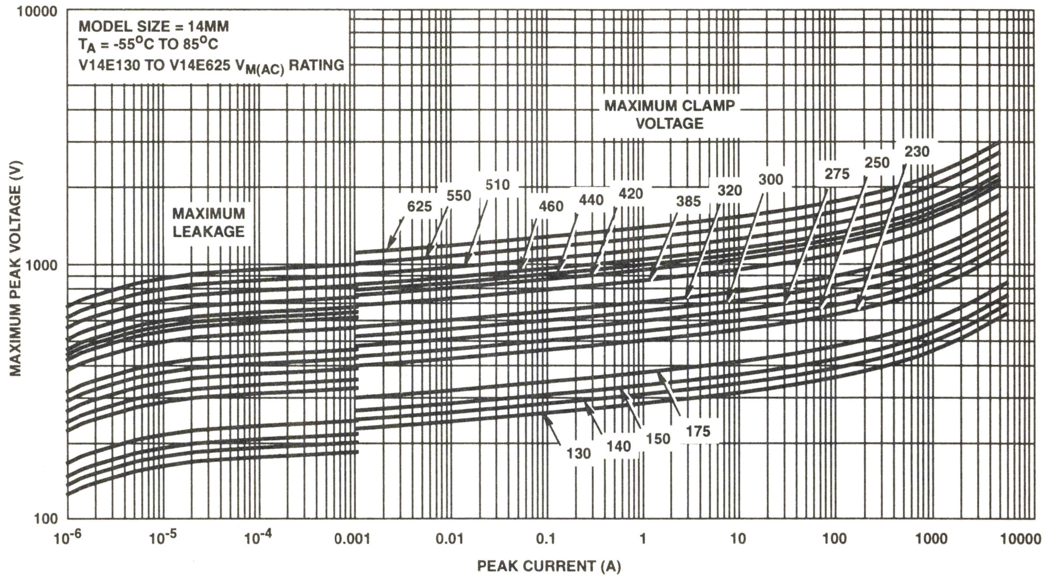


FIGURE 5.

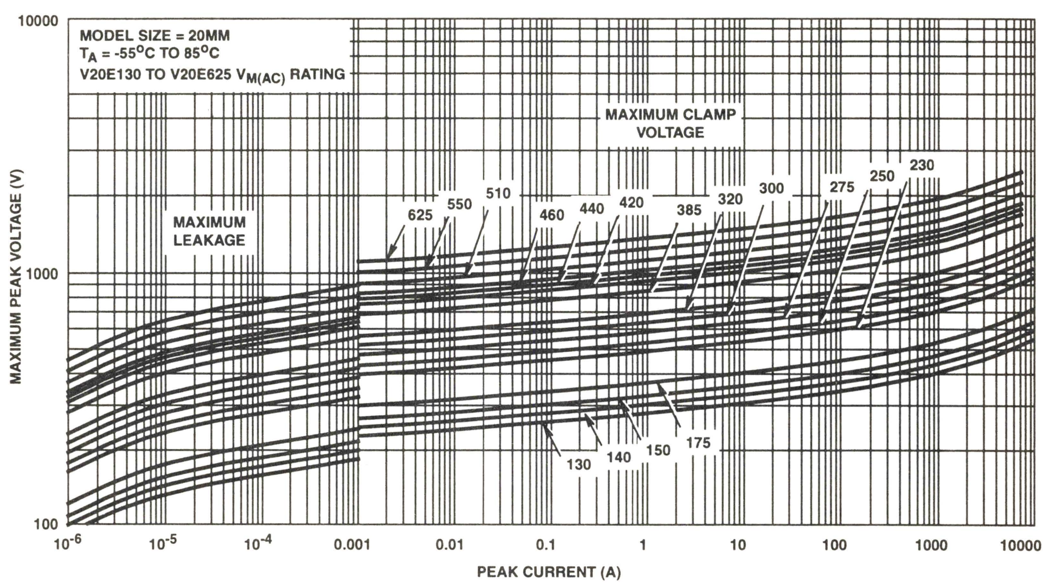


FIGURE 6.

Pulse Rating Curves

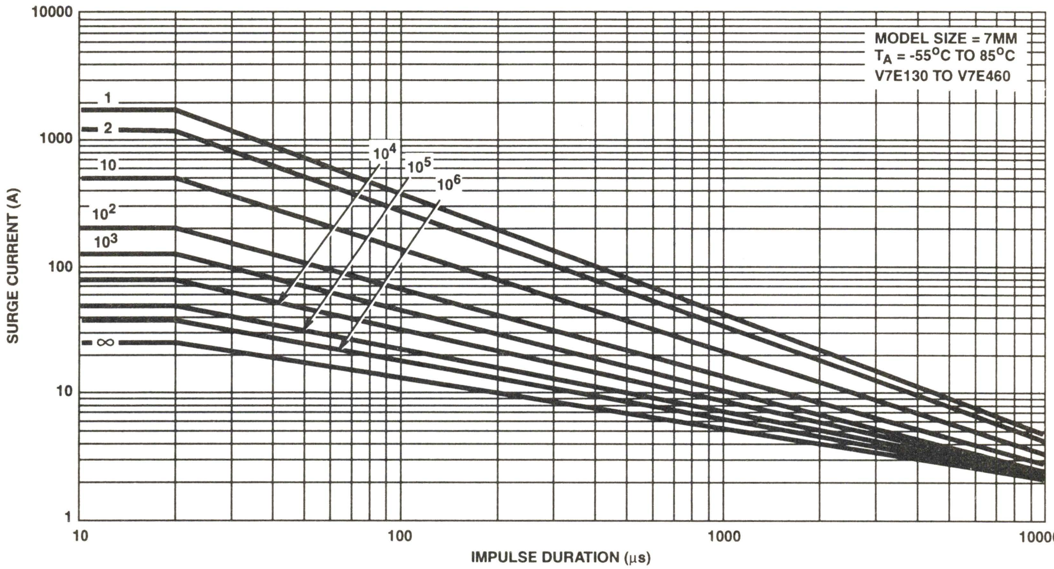


FIGURE 7.

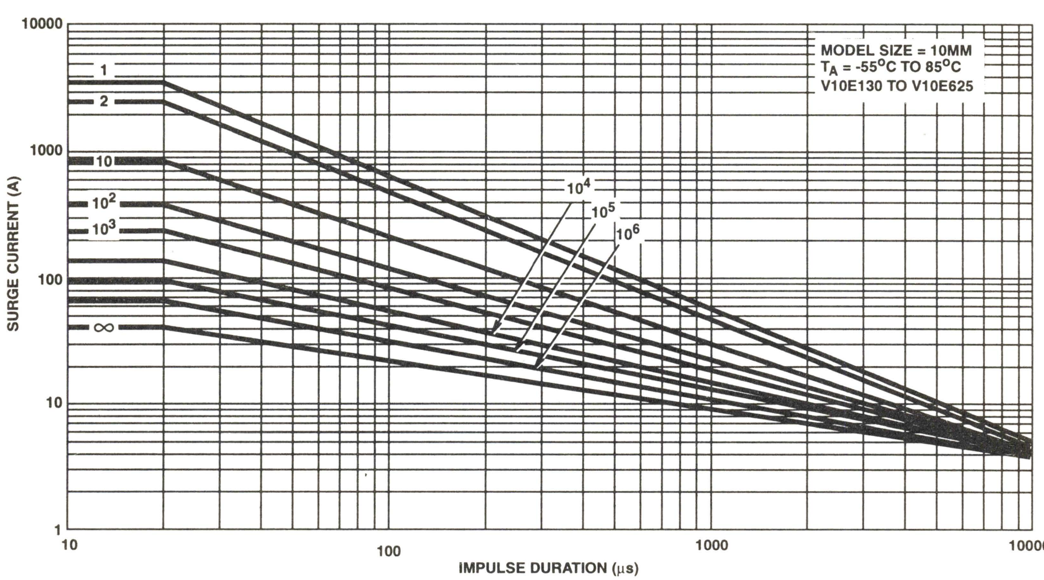


FIGURE 8.

Pulse Rating Curves (Continued)

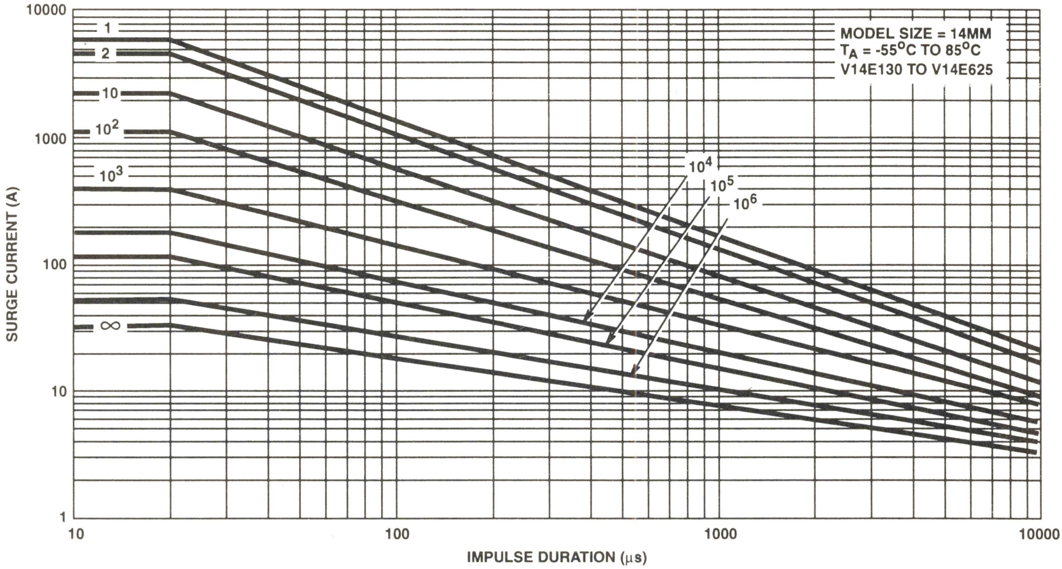


FIGURE 9.

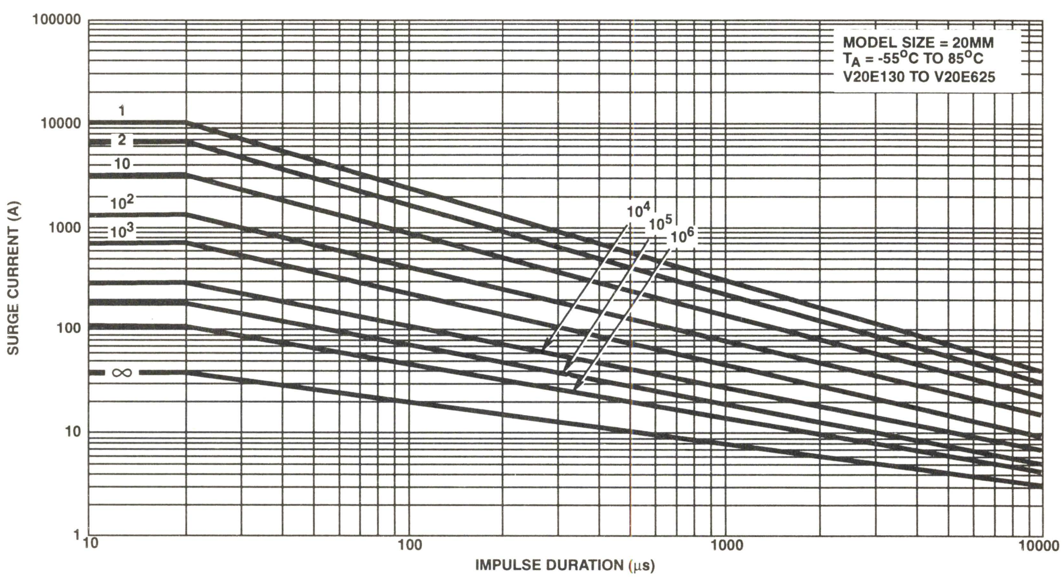
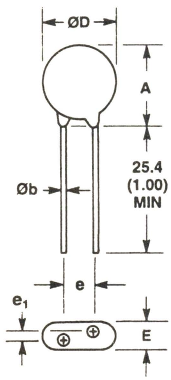


FIGURE 10.

Package Outline Dimensions (Lead Form Options L1 and L3)



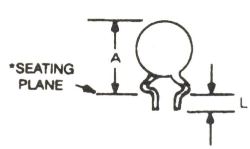
SYMBOL	V_{RMS} VOLTAGE MODEL	VARISTOR MODEL SIZE 7mm MIN	7mm MAX	10mm MIN	10mm MAX	14mm MIN	14mm MAX	20mm MIN	20mm MAX
A	130-320	-	12 (0.472)	-	16 (0.630)	-	20 (0.787)	-	26.5 (1.043)
	385-625	-	13 (0.512)	-	17 (0.689)	-	20.5 (0.807)	-	28 (1.102)
ØD	All	-	9 (0.354)	-	12.5 (0.492)	-	17 (0.669)	-	23 (0.906)
e (Note 2)	All	4 (0.157)	6 (0.236)	6.5 (0.256)	8.5 (0.335)	6.5 (0.256)	8.5 (0.335)	9 (0.354)	11 (0.433)
e_1 (Note 3)	130-320	1.5 (0.059)	3.5 (0.138)	1.5 (0.059)	3.5 (0.138)	1.5 (0.059)	3.5 (0.138)	1.5 (0.059)	3.5 (0.138)
	385-625	2.5 (0.098)	5.5 (0.217)	2.5 (0.098)	5.5 (0.217)	2.5 (0.098)	5.5 (0.217)	2.5 (0.098)	5.5 (0.217)
E	130-320	-	5.6 (0.220)	-	5.6 (0.220)	-	5.6 (0.220)	-	5.6 (0.220)
	385-625	-	7.3 (0.287)	-	7.3 (0.287)	-	7.3 (0.287)	-	7.3 (0.287)
Øb	All	0.585 (0.023)	0.685 (0.027)	0.76 (0.030)	0.86 (0.034)	0.76 (0.030)	0.86 (0.034)	0.76 (0.030) (Note 2)	0.86 (0.034) (Note 2)

Dimensions in millimeters, inches in parentheses.

NOTES:

2. Standard lead space.
3. For in-line lead option L3, dimension e_1 is "zero". Straight lead form option L1 shown.

Lead Dimensions (Lead Form Options L2 and L4)



*Seating plane interpretation per IEC-717

(Not available on tape or ammo pack)

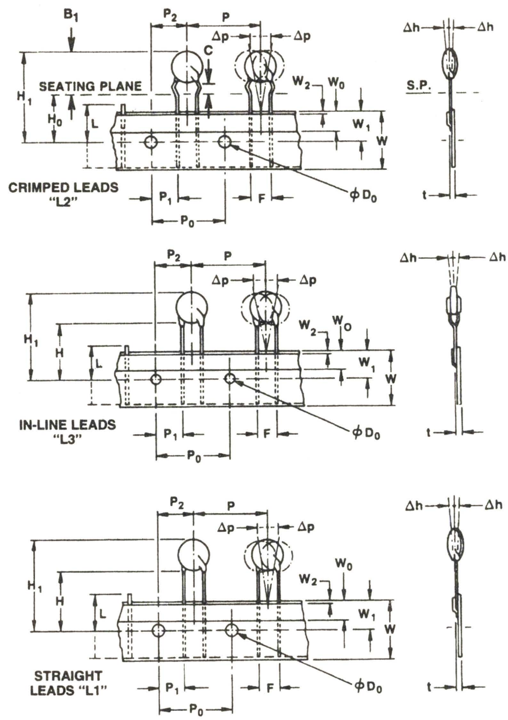
SYMBOL	VARISTOR MODEL SIZE 7mm MIN	7mm MAX	10mm MIN	10mm MAX	14mm MIN	14mm MAX	20mm MIN	20mm MAX
A	- -	15 (0.591)	- -	19.5 (0.768)	- -	22.5 (0.886)	- -	29.0 (1.142)
L (L2)	25.4 (1.00)	- -	25.4 (1.00)	- -	25.4 (1.00)	- -	25.4 (1.00)	- -
*L (L4)	2.41 (0.095)	4.69 (0.185)	2.41 (0.095)	4.69 (0.185)	2.41 (0.095)	4.69 (0.185)	2.41 (0.095)	4.69 (0.185)

Dimensions in millimeters, inches in parentheses.

Standard Bulk Pack Quantities

VARISTOR VOLTAGE MODEL	STANDARD BULK PACK QUANTITY / VARISTOR MODEL SIZE 7mm	10mm	14mm	20mm
130-275	1500	1000	700	500
300-460	1500	700	600	400
510-625	1500	700	500	400

Tape Specifications for Reel or Ammo Pack (Fan-Fold)



- Conforms to ANSI and EIA specifications.
- Can be supplied to IEC Publication 286-2.
- Radial devices on tape are offered with crimped leads, straight leads, or in-line leads. See Ordering Information.

REEL CAPACITY 330mm (13in.)

DEVICE SIZE	SHIPPING QUANTITY PER REEL
7	1000
10	1000
14	500
20	500

SYMBOL	PARAMETER	MODEL SIZE			
		7mm	10mm	14mm	20mm
B_1	Component Top to Seating Plane	13.75 ±0.75	18.50 ±0.50	21.50 ±0.50	28.00 ±0.50
C	Crimp Length	2.4 Typ	2.6 Typ	2.6 Typ	2.6 Typ
P	Pitch of Component	12.7 ± 1.0	25.4 ± 1.0	25.4 ± 1.0	25.4 ± 1.0
P_0	Feed Hole Pitch	12.7 ± 0.2	12.7 ± 0.2	12.7 ± 0.2	12.7 ± 0.2
P_1	Feed Hole Center to Pitch	3.85 ± 0.7	2.6 ± 0.7	2.6 ± 0.7	2.6 ± 0.7
P_2	Hole Center to Component Center	6.35 ± 0.7	6.35 ± 0.7	6.35 ± 0.7	6.35 ± 0.7
F	Lead to Lead Distance	5.0 ± 0.8	7.5 ± 0.8	7.5 ± 0.8	7.5 ± 0.8
Δh	Component Alignment	2.0 Max	2.0 Max	2.0 Max	2.0 Max
W	Tape Width	18.0 + 1.0 18.0 - 0.5	18.0 + 1.0 18.0 - 0.5	18.0 + 1.0 18.0 - 0.5	18.0 + 1.0 18.0 - 0.5
W_0	Hold Down Tape Width	6.0 ± 0.3	6.0 ± 0.3	6.0 ± 0.3	12.0 ± 0.3
W_1	Hole Position	9.0 + 0.75 9.0 - 0.50	9.0 + 0.75 9.0 - 0.50	9.0 + 0.75 9.0 - 0.50	9.0 + 0.75 9.0 - 0.50
W_2	Hold Down Tape Position	0.5 Max	0.5 Max	0.5 Max	0.5 Max
H	Height from Tape Center to Component Base	18.0 + 2.0 18.0 - 0.0	18.0 + 2.0 18.0 - 0.0	18.0 + 2.0 18.0 - 0.0	18.0 + 2.0 18.0 - 0.0
H_0	Seating Plane Height	16.0 ± 0.5	16.0 ± 0.5	16.0 ± 0.5	16.0 ± 0.5
H_1	Component Height	32.0 Max	36.0 Max	40.0 Max	46.5 Max
D_0	Feed Hole Diameter	4.0 ± 0.2	4.0 ± 0.2	4.0 ± 0.2	4.0 ± 0.2
t	Total Tape Thickness	0.7 ± 0.2	0.7 ± 0.2	0.7 ± 0.2	0.7 ± 0.2
L	Length of Clipped Lead	11.0 Max	11.0 Max	11.0 Max	11.0 Max
Δp	Component Alignment	3^{o} Max, 1.00mm	3^{o} Max, 1.00mm	3^{o} Max, 1.00mm	3^{o} Max

Dimensions are in mm.

Model Number Nomenclature

The UltraMOV Series follows a different part numbering procedure than other Harris Varistor products. The base part number consists of the following:

V = Harris Varistor Designation
xx = Nominal Disc Diameter (07, 10, 14, 20mm)
E = Epoxy Encapsulation (Rated to 85^{O}C)
xxx = $V_{M(AC)\ RMS}$ Voltage Rating (130V - 625V)

For example, the model number for a 7mm epoxy coated Varistor rated at 440V RMS is V07E440. (Note that this number will be abbreviated to accommodate marking (laser branding) of the Varistor body. (The part number brand is shown in the Device Ratings and Characteristics table.)

Ordering Information

To order devices in the UltraMOV Series, the base part number must be appended with lead form, packaging and lead space options as shown below.

V xx E xxx Lx X X

DEVICE FAMILY:
Harris Varistor

DISC DIAMETER:
07, 10, 14, or 20 (mm)

ENCAPSULATION:
E = Epoxy

$V_{M(AC)RMS}$:
130 to 625 (V)

LEAD FORMATION:
L1 = Straight
L2 = Crimped
L3 = In-Line
L4 = Trim/Crimp (Bulk pack only)

PACKAGING:
B = Bulk Pack
T = Tape and Reel
A = Ammo Pack

NON-STANDARD LEAD SPACING OPTIONS (DO NOT ADD IF STANDARD) (NOTE 4):
5 = 5mm Lead Spacing
7 = 7.5mm Lead Spacing
1 = 10mm Lead Spacing

NOTE:
4. Standard lead space.

Terms

Rated AC Voltage ($V_{M(AC)RMS}$)

This is the maximum continuous sinusoidal voltage which may be applied to the MOV. This voltage may be applied at any temperature up to the maximum operating temperature of 85^{O}C.

Maximum Non-Repetitive Surge Current (I_{TM})

This is the maximum peak current which may be applied for an 8/20µs impulse, with rated line voltage also applied, without causing device failure. (See Figure 2)

Maximum Non-Repetitive Surge Energy (W_{TM})

This is the maximum rated transient energy which may be dissipated for a single current pulse at a specified impulse and duration (2ms), with the rated V_{RMS} applied, without causing device failure.

Nominal Voltage ($V_{N(DC)}$)

This is the voltage at which the device changes from the off state to the on state and enters its conduction mode of operation. This voltage is characterized at the 1mA point and has specified minimum and maximum voltage levels.

Clamping Voltage (V_C)

This is the peak voltage appearing across the MOV when measured at conditions of specified pulse current amplitude and specified waveform (8/20µs).

HARRIS SEMICONDUCTOR

LA Series

ALSO SEE HARRIS ULTRAMOV SERIES

January 1998

Radial Lead Metal-Oxide Varistors for Line Voltage Operation

Features

- Recognized as "Transient Voltage Surge Suppressors", UL File #E75961 to Standard 1449
- Recognized as "Across-The-Line Components", UL File #E56529 to Standard 1414
- Recognized as "Protectors for Data Communication and Fire Alarm Circuits", UL File #E135010 to Standard 497B
- CECC Certified (42201-006)
- Recognized as "Transient Voltage Surge Suppressors", CSA File #LR91788 to Standard C22.2 No. 1 - M1981
- High Energy Absorption Capability W_{TM} . . Up to 360J
- Wide Operating Voltage Range $V_{M(AC)RMS}$. . . .130V to 1000V
- No Derating Up to 85°C Ambient
- Available in Tape and Reel or Bulk Pack

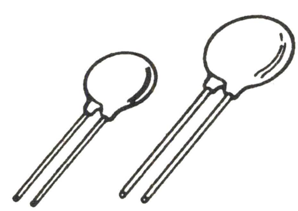
Description

The LA Series of transient voltage surge suppressors are radial-lead varistors (MOVs) that are designed to be operated continuously across AC power lines. These UL recognized varistors require very little mounting space, and are offered in various standard lead form options.

The LA Series varistors are available in four model sizes: 7mm, 10mm, 14mm and 20mm; and have a $V_{M(AC)RMS}$ voltage range from 130V to 1000V, and an energy absorption capability up to 360J. Some LA series model numbers are available with clamping voltage selections, designated by a model number suffix of either A or B. The "A" selection is the standard model; the "B" selection provides a lower clamping voltage.

See LA Series Device Ratings and Specifications table for part number and brand information.

Packaging



14mm, 20mm

7mm, 10mm

Absolute Maximum Ratings

For ratings of individual members of a series, see Device Ratings and Specifications chart

	LA SERIES	UNITS
Continuous:		
Steady State Applied Voltage:		
AC Voltage Range ($V_{M(AC)RMS}$)	130 to 1000	V
DC Voltage Range ($V_{M(DC)}$)	175 to 1200	V
Transients:		
Peak Pulse Current (I_{TM})		
For 8/20µs Current Wave (See Figure 2)	1200 to 6500	A
Single Pulse Energy Range		
For 10/1000µs Current Wave (W_{TM})	11 to 360	J
Operating Ambient Temperature Range (T_A)	-55 to 85	°C
Storage Temperature Range (T_{STG})	-55 to 125	°C
Temperature Coefficient (αV) of Clamping Voltage (V_C) at Specified Test Current	<0.01	%/°C
Hi-Pot Encapsulation (Isolation Voltage Capability) (Dielectric must withstand indicated DC voltage for one minute per MIL-STD 202, Method 301)	2500	V
Insulation Resistance	1000	MΩ

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Device Ratings and Specifications

Series LA Varistors are listed under UL file #E75961 and E56529 as a recognized component.
Series LA Varistors are listed under CSA file #LR91788 as a recognized component.

PART NUMBER	MODEL SIZE DISC DIA. (mm)	DEVICE MODEL NUMBER BRAND-ING	MAXIMUM RATING (85°C)				SPECIFICATIONS (25°C)				
			CONTINUOUS		TRANSIENT		VARISTOR VOLTAGE AT 1mA DC TEST CURRENT		MAXIMUM CLAMPING VOLTAGE 8 x 20µs		TYPICAL CAPACI-TANCE f = 1MHz
			V_{RMS}	V_{DC}	ENERGY 10 x 1000µs	PEAK CURRENT 8 x 20µs					
			$V_{M(AC)}$	$V_{M(DC)}$	W_{TM}	I_{TM}	V_{NOM} MIN	V_{NOM} MAX	V_C	I_{PK}	C
			(V)	(V)	(J)	(A)	(V)		(V)	(A)	(pF)
V130LA1	7	1301	130	175	11	1200	184	255	390	10	180
V130LA2	7	1302	130	175	11	1200	184	228	340	10	180
V130LA5	10	1305	130	175	20	2500	184	228	340	25	450
V130LA10A	14	130L10	130	175	38	4500	184	228	340	50	1000
V130LA20A	20	130L20	130	175	70	6500	184	228	340	100	1900
V130LA20B	20	130L20B	130	175	70	6500	184	220	325	100	1900
V140LA2	7	1402	140	180	12	1200	198	242	360	10	160
V140LA5	10	1405	140	180	22	2500	198	242	360	25	400
V140LA10A	14	140L10	140	180	42	4500	198	242	360	50	900
V140LA20A	20	140L20	140	180	75	6500	198	242	340	100	1750
V150LA1	7	1501	150	200	13	1200	212	284	430	10	150
V150LA2	7	1502	150	200	13	1200	212	268	395	10	150
V150LA5	10	1505	150	200	25	2500	212	268	395	25	360
V150LA10A	14	150L10	150	200	45	4500	212	268	395	50	800
V150LA20A	20	150L20	150	200	80	6500	212	268	395	100	1600
V150LA20B	20	150L20B	150	200	80	6500	212	243	360	100	1600

Device Ratings and Specifications (Continued)

Series LA Varistors are listed under UL file #E75961 and E56529 as a recognized component.
Series LA Varistors are listed under CSA file #LR91788 as a recognized component.

PART NUMBER	MODEL SIZE DISC DIA. (mm)	DEVICE MODEL NUMBER BRANDING	MAXIMUM RATING (85°C) CONTINUOUS V_{RMS}		TRANSIENT ENERGY 10 x 1000μs	PEAK CURRENT 8 x 20μs	SPECIFICATIONS (25°C) VARISTOR VOLTAGE AT 1mA DC TEST CURRENT		MAXIMUM CLAMPING VOLTAGE 8 x 20μs		TYPICAL CAPACITANCE f = 1MHz
			V_{RMS}	V_{DC}							
			$V_{M(AC)}$	$V_{M(DC)}$	W_{TM}	I_{TM}	V_{NOM} MIN	V_{NOM} MAX	V_C	I_{PK}	C
			(V)	(V)	(J)	(A)	(V)		(V)	(A)	(pF)
V175LA2	7	1752	175	225	15	1200	247	303	455	10	130
V175LA5	10	1755	175	225	30	2500	247	303	455	25	350
V175LA10A	14	175L10	175	225	55	4500	247	303	455	50	700
V175LA20A	20	175L20	175	225	90	6500	247	303	455	100	1400
V230LA4	7	2304	230	300	20	1200	324	396	595	10	100
V230LA10	10	230L	230	300	35	2500	324	396	595	25	250
V230LA20A	14	230L20	230	300	70	4500	324	396	595	50	550
V230LA40A	20	230L40	230	300	122	6500	324	396	595	100	1100
V250LA2	7	2502	250	330	21	1200	354	473	730	10	90
V250LA4	7	2504	250	330	21	1200	354	429	650	10	90
V250LA10	10	250L	250	330	40	2500	354	429	650	25	220
V250LA20A	14	250L20	250	330	72	4500	354	429	650	50	500
V250LA40A	20	250L40	250	330	130	6500	354	429	650	100	1000
V250LA40B	20	250L40B	250	330	130	6500	354	413	620	100	1000
V275LA2	7	2752	275	369	23	1200	389	515	775	10	80
V275LA4	7	2754	275	369	23	1200	389	473	710	10	80
V275LA10	10	275L	275	369	45	2500	389	473	710	25	200
V275LA20A	14	275L20	275	369	75	4500	389	473	710	50	450
V275LA40A	20	275L40	275	369	140	6500	389	473	710	100	900
V275LA40B	20	275L40B	275	369	140	6500	389	453	680	100	900
V300LA2	7	3002	300	405	25	1200	420	565	870	10	70
V300LA4	7	3004	300	405	25	1200	420	517	775	10	70
V300LA10	10	300L	300	405	46	2500	420	517	775	25	180
V300LA20A	14	300L20	300	405	77	4500	420	517	775	50	400
V300LA40A	20	300L40	300	405	165	6500	420	517	775	100	800
V320LA7	7	3207	320	420	25	1200	462	565	850	10	65
V320LA10	10	320L	320	420	48	2500	462	565	850	25	170
V320LA20A	14	320L20	320	420	80	4500	462	565	850	50	380
V320LA40B	20	320L40	320	420	150	6500	462	540	810	100	750

Device Ratings and Specifications (Continued)

Series LA Varistors are listed under UL file #E75961 and E56529 as a recognized component.
Series LA Varistors are listed under CSA file #LR91788 as a recognized component.

PART NUMBER	MODEL SIZE DISC DIA. (mm)	DEVICE MODEL NUMBER BRAND-ING	MAXIMUM RATING (85°C)				SPECIFICATIONS (25°C)				
			CONTINUOUS		TRANSIENT		VARISTOR VOLTAGE AT 1mA DC TEST CURRENT		MAXIMUM CLAMPING VOLTAGE 8 x 20µs		TYPICAL CAPACI-TANCE f = 1MHz
			V_{RMS}	V_{DC}	ENERGY 10 x 1000µs	PEAK CURRENT 8 x 20µs					
			$V_{M(AC)}$	$V_{M(DC)}$	W_{TM}	I_{TM}	V_{NOM} MIN	V_{NOM} MAX	V_C	I_{PK}	C
			(V)	(V)	(J)	(A)	(V)		(V)	(A)	(pF)
V385LA7	7	3857	385	505	27	1200	558	682	1025	10	60
V385LA10	10	385L	385	505	51	2500	558	682	1025	25	160
V385LA20A	14	385L20	385	505	85	4500	558	682	1025	50	360
V385LA40B	20	385L40	385	505	160	6500	558	682	1025	100	700
V420LA7	7	4207	420	560	30	1200	610	748	1120	10	55
V420LA10	10	420L	420	560	55	2500	610	748	1120	25	140
V420LA20A	14	420L20	420	560	90	4500	610	748	1120	50	300
V420LA40B	20	420L40	420	560	160	6500	610	720	1060	100	600
V460LA7	7	4607	460	615	37	1200	702	858	1130	10	55
V480LA7	7	4807	480	640	35	1200	670	825	1240	10	270
V480LA10	10	480L	480	640	60	2500	670	825	1240	25	120
V480LA40A	14	480L40	480	640	105	4500	670	825	1240	50	270
V480LA80B	20	480L80	480	640	180	6500	670	790	1160	100	550
V510LA10	10	510L	510	675	63	2500	735	910	1350	25	100
V510LA40A	14	510L40	510	675	110	4500	735	910	1350	50	250
V510LA80B	20	510L80	510	675	190	6500	735	860	1280	100	500
V575LA10	10	575L	575	730	65	2500	805	1000	1500	25	90
V575LA40A	14	575L40	575	730	120	4500	805	1000	1500	50	220
V575LA80B	20	575L80	575	730	220	6500	805	960	1410	100	450
V625LA10	10	625L	625	825	67	2500	940	1210	1820	25	80
V625LA40A	14	625L40	625	825	125	4500	940	1210	1820	50	210
V625LA80B	20	625L80	625	825	230	6500	940	1100	1650	100	425
V660LA10	10	660L	660	850	70	2500	940	1210	1820	50	70
V660LA50A	14	660L50	660	850	140	4500	940	1210	1820	50	200
V660LA100B	20	660L100	660	850	250	6500	940	1100	1650	100	400
V1000LA80A	14	1000L80	1000	1200	220	4500	1425	1800	2700	50	130
V1000LA160B	20	1000L160	1000	1200	360	6500	1425	1600	2420	100	250

NOTE: Average power dissipation of transients not to exceed 0.25W, 0.4W, 0.6W or 1W for model sizes 7mm, 10mm, 14mm and 20mm, respectively.

Power Dissipation Ratings

Continuous power dissipation capability is not an applicable parameter for a varistor. When transients occur in rapid succession, the average power dissipation is the energy (watt-seconds) per pulse times the number of pulses per second. The power so developed must be within the specifications shown on the Device Ratings and Specifications table for the specific device. The operating values of a MOV need to be derated at high temperatures as shown in Figure 1. Because varistors only dissipate a relatively small amount of average power they are not suitable for repetitive applications that involve substantial amounts of average power dissipation.

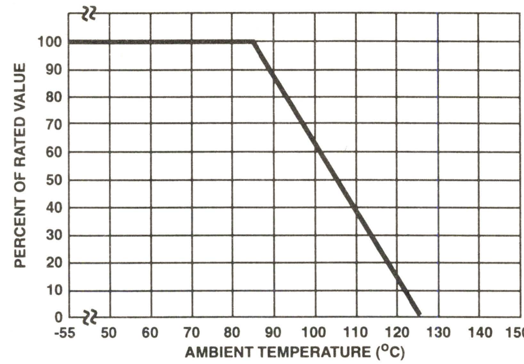
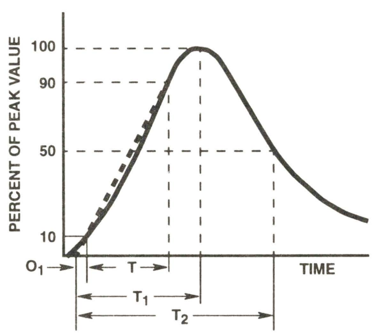


FIGURE 1. CURRENT, ENERGY AND POWER DERATING CURVE



O_1 = Virtual Origin of Wave
T = Time From 10% to 90% of Peak
T_1 = Virtual Front time = 1.25 • t
T_2 = Virtual Time to Half Value (Impulse Duration)
Example: For an 8/20μs Current Waveform:
8μs = T_1 = Virtual Front Time
20μs = T_2 = Virtual Time to Half Value

FIGURE 2. PEAK PULSE CURRENT TEST WAVEFORM

Transient V-I Characteristics Curves

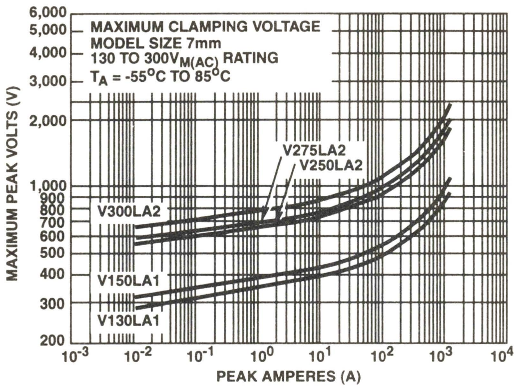


FIGURE 3. CLAMPING VOLTAGE FOR V130LA1 - V300LA2

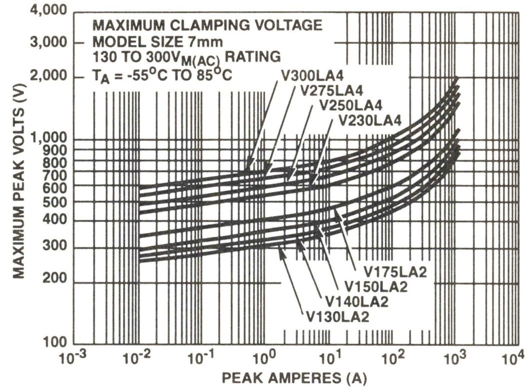


FIGURE 4. CLAMPING VOLTAGE FOR V130LA2 - V300LA4

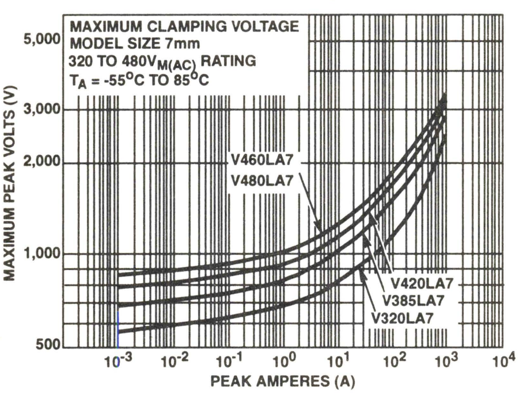


FIGURE 5. CLAMPING VOLTAGE FOR V320LA7 - V480LA7

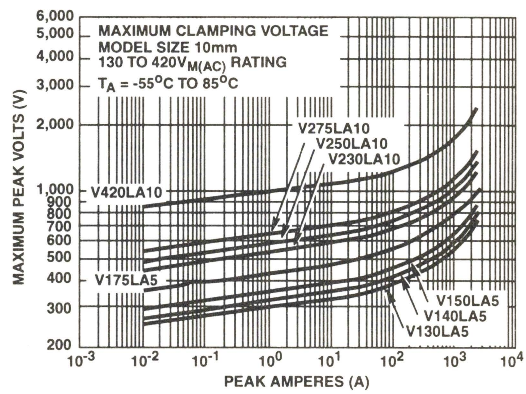


FIGURE 6. CLAMPING VOLTAGE FOR V130LA5 - V420LA10

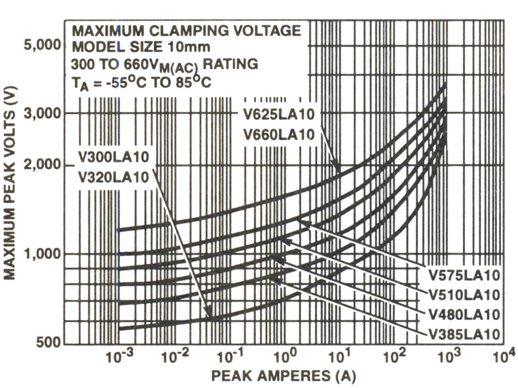


FIGURE 7. CLAMPING VOLTAGE FOR V300LA10 - V660LA10

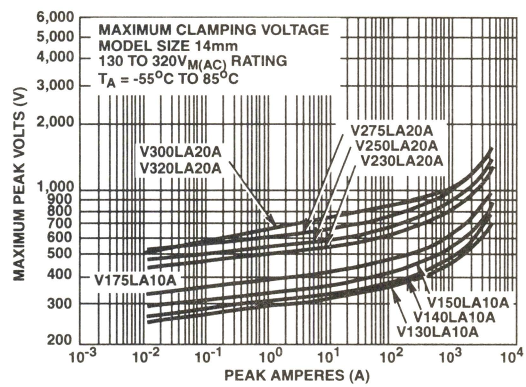


FIGURE 8. CLAMPING VOLTAGE FOR V130LA10A - V320LA20A

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VARISTOR PRODUCTS

Transient V-I Characteristics Curves (Continued)

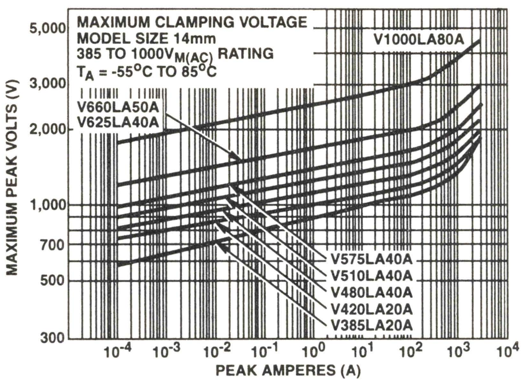


FIGURE 9. CLAMPING VOLTAGE FOR V385LA20A - V1000LA80A

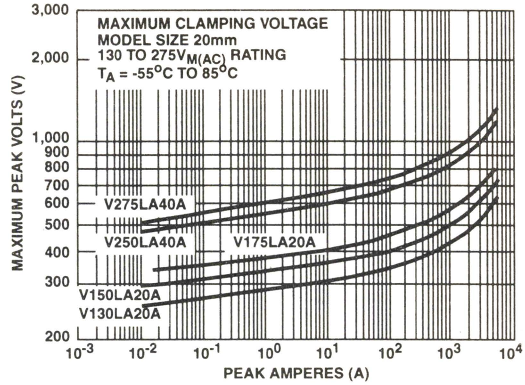


FIGURE 10. LAMPING VOLTAGE FOR V130LA20A - V275LA40A

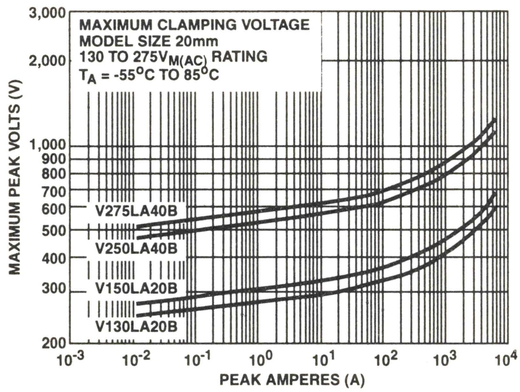


FIGURE 11. CLAMPING VOLTAGE FOR V130LA20B - V275LA40B

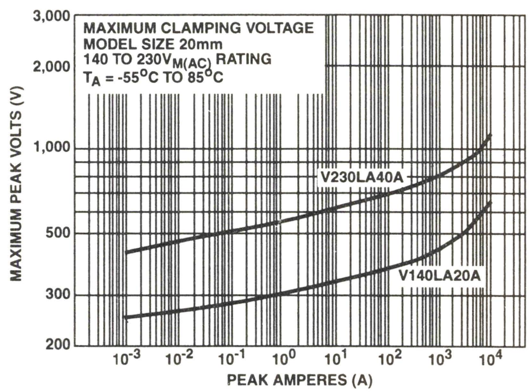


FIGURE 12. CLAMPING VOLTAGE FOR V140LA20A - V230LA40A

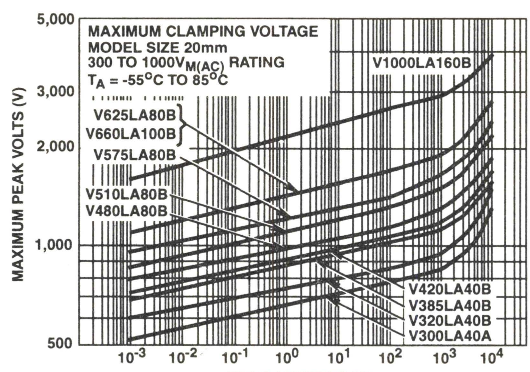


FIGURE 13. CLAMPING VOLTAGE FOR V300LA40A - V1000LA160B

Pulse Rating Curves

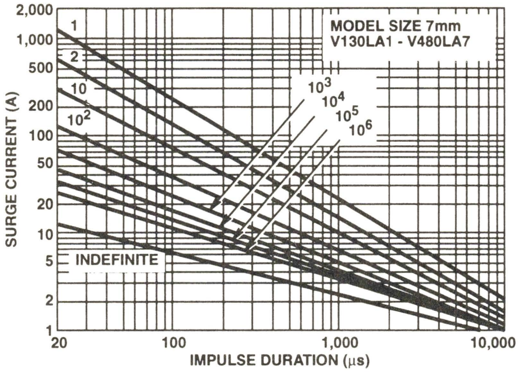


FIGURE 14. SURGE CURRENT RATING CURVES FOR V130LA1 - V480LA7

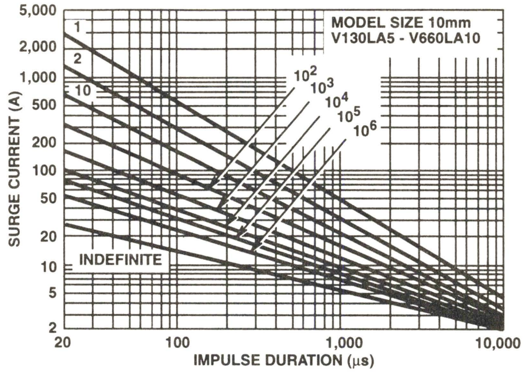


FIGURE 15. SURGE CURRENT RATING CURVES FOR V130LA5 - V660LA10

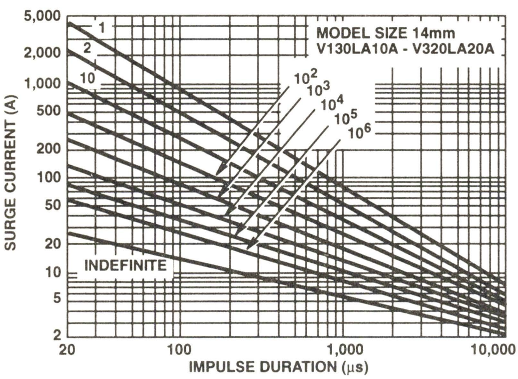


FIGURE 16. SURGE CURRENT RATING CURVES FOR V130LA10A - V320LA20A

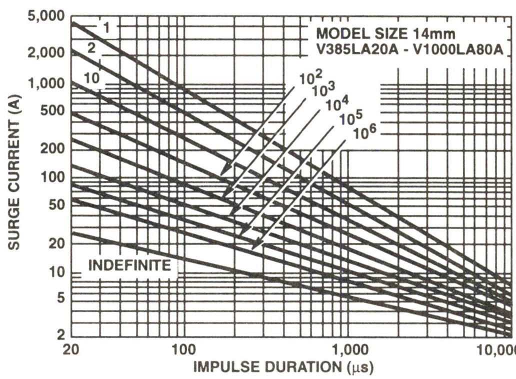


FIGURE 17. SURGE CURRENT RATING CURVES FOR V385LA20A - V1000LA80A

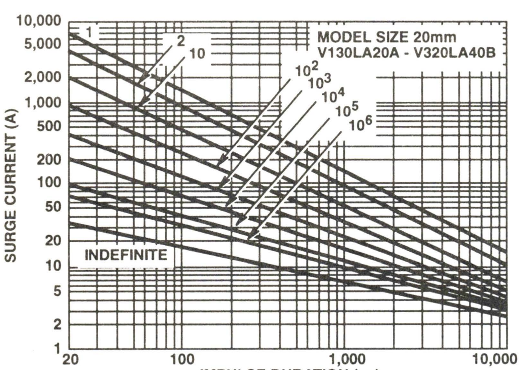


FIGURE 18. SURGE CURRENT RATING CURVES FOR V130LA20A - V320LA40B

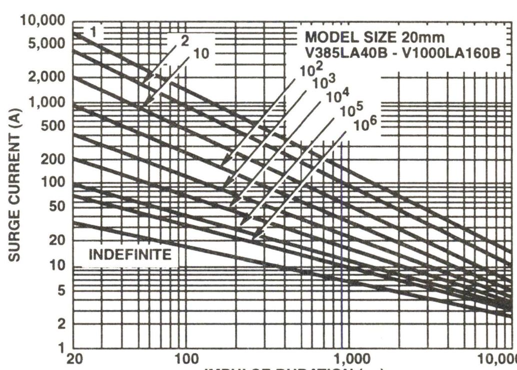
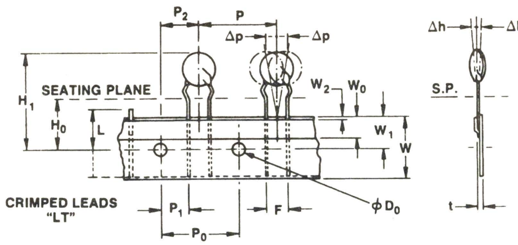
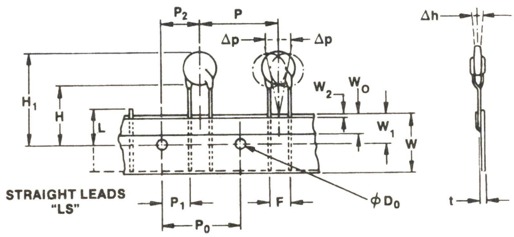


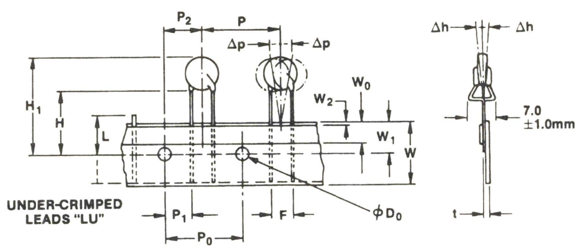
FIGURE 19. SURGE CURRENT RATING CURVES FOR V385LA40B - V1000LA160B

NOTE: If pulse ratings are exceeded, a shift of $V_{N(DC)}$ (at specified current) of more than ±10% could result. This type of shift, which normally results in a decrease of $V_{N(DC)}$, may result in the device not meeting the original published specifications, but does not prevent the device from continuing to function, and to provide ample protection.

Tape and Reel Specifications







Tape and Reel Data

- Conforms to ANSI and EIA specifications
- Can be supplied to IEC Publication 286-2
- Radial devices on tape are supplied with crimped leads, straight leads, or under-crimped leads

SYMBOL	PARAMETER	MODEL SIZE			
		7mm	10mm	14mm	20mm
P	Pitch of Component	12.7 ± 1.0	25.4 ± 1.0	25.4 ± 1.0	25.4 ± 1.0
P_0	Feed Hole Pitch	12.7 ± 0.2	12.7 ± 0.2	12.7 ± 0.2	12.7 ± 0.2
P_1	Feed Hole Center to Pitch	3.85 ± 0.7	2.6 ± 0.7	2.6 ± 0.7	2.6 ± 0.7
P_2	Hole Center to Component Center	6.35 ± 0.7	6.35 ± 0.7	6.35 ± 0.7	6.35 ± 0.7
F	Lead to Lead Distance	5.0 ± 0.8	7.5 ± 0.8	7.5 ± 0.8	7.5 ± 0.8
Δh	Component Alignment	2.0 Max	2.0 Max	2.0 Max	2.0 Max
W	Tape Width	18.0 + 1.0 18.0 - 0.5	18.0 + 1.0 18.0 - 0.5	18.0 + 1.0 18.0 - 0.5	18.0 + 1.0 18.0 - 0.5
W_0	Hold Down Tape Width	6.0 ± 0.3	6.0 ± 0.3	6.0 ± 0.3	12.0 ± 0.3
W_1	Hole Position	9.0 + 0.75 9.0 - 0.50	9.0 + 0.75 9.0 - 0.50	9.0 + 0.75 9.0 - 0.50	9.0 + 0.75 9.0 - 0.50
W_2	Hold Down Tape Position	0.5 Max	0.5 Max	0.5 Max	0.5 Max
H	Height from Tape Center to Component Base	18.0 + 2.0 18.0 - 0.0	18.0 + 2.0 18.0 - 0.0	18.0 + 2.0 18.0 - 0.0	18.0 + 2.0 18.0 - 0.0
H_0	Seating Plane Height	16.0 ± 0.5	16.0 ± 0.5	16.0 ± 0.5	16.0 ± 0.5
H_1	Component Height	32.0 Max	36.0 Max	40.0 Max	46.5 Max
D_0	Feed Hole Diameter	4.0 ± 0.2	4.0 ± 0.2	4.0 ± 0.2	4.0 ± 0.2
t	Total Tape Thickness	0.7 ± 0.2	0.7 ± 0.2	0.7 ± 0.2	0.7 ± 0.2
L	Length of Clipped Lead	11.0 Max	11.0 Max	11.0 Max	11.0 Max
Δp	Component Alignment	3^{o} Max 1.00mm	3^{o} Max 1.00mm	3^{o} Max 1.00mm	3^{o} Max

NOTE: Dimensions are in mm.

Tape and Reel Ordering Information

Crimped leads are standard on LA types supplied in tape and reel and are denoted by the model letter "T". Model letter "S" denotes straight leads and letter "U" denotes special under-crimped leads.

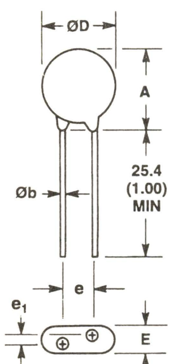
Example:

STANDARD MODEL	CRIMPED LEADS	STRAIGHT LEADS	UNDER-CRIMPED LEADS
V130LA2	V130LT2	V130LS2	V130LU2

SHIPPING QUANTITY

SIZE	RMS (MAX) VOLTAGE	QUANTITY PER REEL "T" REEL	"S" REEL	"U" REEL
7mm	All	1000	1000	1000
10mm	All	1000	1000	1000
14mm	< 300V	500	500	500
14mm	≥ 300V	500	500	500
20mm	<300V	500	500	500
20mm	≤ 300V	500	500	500

Mechanical Dimensions



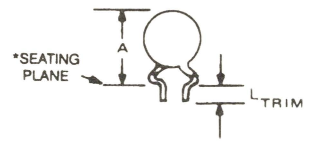
SYMBOL	VOLTAGE MODEL	VARISTOR MODEL SIZE 7mm MIN	7mm MAX	10mm MIN	10mm MAX	14mm MIN	14mm MAX	20mm MIN	20mm MAX
A	V130LA- V320LA	- -	12 (0.472)	- -	16 (0.630)	- -	20 (0.787)	- -	26.5 (1.043)
	V385LA- V1000LA	- -	13 (0.0512)	- -	17 (0.689)	- -	20.5 (0.807)	- -	28 (1.102)
ØD	All	- -	9 (0.354)	- -	12.5 (0.492)	- -	17 (0.669)	- -	23 (0.906)
e	All	4 (0.157)	6 (0.236)	6.5 (0.256)	8.5 (0.335)	6.5 (0.256)	8.5 (0.335)	6.5 (0.256) (Note 2)	8.5 (0.335) (Note 2)
e_1	V130LA- V320LA	1.5 (0.059)	3.5 (0.138)	1.5 (0.059)	3.5 (0.138)	1.5 (0.059)	3.5 (0.138)	1.5 (0.059)	3.5 (0.138)
	V385A- V1000LA	2.5 (0.098)	5.5 (0.217)	2.5 (0.098)	5.5 (0.217)	2.5 (0.098)	5.5 (0.217)	2.5 (0.098)	5.5 (0.217)
E	V130LA- V320LA	- -	5.6 (0.220)	- -	5.6 (0.220)	- -	5.6 (0.220)	- -	5.6 (0.220)
	V385LA- V660LA	- -	7.3 (0.287)	- -	7.3 (0.287)	- -	7.3 (0.287)	- -	7.3 (0.287)
	V1000LA	- -	- -	- -	- -	- -	10.8 (0.425)	- -	10.8 (0.425)
Øb	All (Note 3)	0.585 (0.023)	0.685 (0.027)	0.76 (0.030)	0.86 (0.034)	0.76 (0.030)	0.86 (0.034)	0.76 (0.030) (Note 2)	0.86 (0.034) (Note 2)

NOTES:

1. Dimensions in millimeters, inches in parentheses.
2. 10mm (9mm min, 11mm max) ALSO AVAILABLE; See Additional Lead Style Options
3. 1000V parts supplied with lead wire of diameter 1.00 ± 0.05 (0.039 ± 0.002).

Additional Lead Style Options

Radial lead types can be supplied with combination preformed crimp and trimmed leads. This option is supplied to the dimensions shown.



*Seating plane interpretation per IEC-717

CRIMPED AND TRIMMED LEAD

SYMBOL	VARISTOR MODEL SIZE							
	7mm		10mm		14mm		20mm	
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	- -	15 (0.591)	- -	19.5 (0.768)	- -	22.5 (0.886)	- -	29.0 (1.142)
L_{TRIM}	2.41 (0.095)	4.69 (0.185)	2.41 (0.095)	4.69 (0.185)	2.41 (0.095)	4.69 (0.185)	2.41 (0.095)	4.69 (0.185)

NOTE: Dimensions in millimeters, inches in parentheses.

To order this crimped and trimmed lead style, standard radial type model numbers are changed by replacing the model letter "A" with "C".

Example:

STANDARD CATALOG MODEL	ORDER AS:
V130LA2	V130LC2

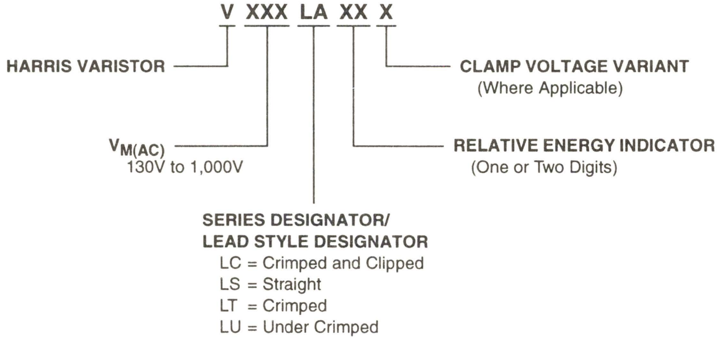
- For crimped leads without trimming and any variations to the above, contact Harris Semiconductor Power Marketing.

- For 10/±1mm lead spacing on 20mm diameter models only; append standard model numbers by adding "X10".

Example:

STANDARD CATALOG MODEL	ORDER AS:
V130LA20A	V130LA20AX10

Ordering Information



"C" III Series

ALSO SEE HARRIS ULTRAMOV SERIES

January 1998

Radial Lead Metal-Oxide Varistors

Features

- Recognized as "Transient Voltage Surge Suppressors" to UL 1449; File # E75961
- Recognized as "Transient Voltage Surge Suppressors" to CSA C22.2, No. 1; File # LR91788
- High Energy Absorption Capability
  W_{TM} . . . . 45J to 210J (2ms)
- High Peak Pulse Current Capability
  I_{TM} . . . . 6000A to 9000A (8/20µs)
- Wide Operating Voltage Range
  $V_{M(AC)RMS}$ . . . . 130V to 320V
- Available in Tape and Reel for Automatic Insertion; Also Available with Crimped and/or Trimmed Lead Styles
- No Derating Up to 85°C Ambient

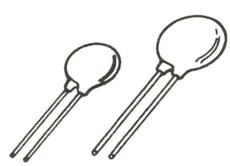
Description

The expanded version of the LA Series of metal-oxide varistors, designation "C" III Series, consists of AC line voltage rated MOVs with high current and energy handling capabilities. The "C" III Series of MOVs was primarily designed for the transient voltage surge suppressor (TVSS) product environment. They provide the increased level of protection for the transients expected in this environment. This special version of the Harris 14mm and 20mm LA Series of metal oxide varistors is also available with 10mm lead spacing, tape and reel, and in a variety of crimped and trimmed lead forms. Also see the Harris UltraMOV™ Series.

See "C" III Series Ratings table for part number and brand information.

Packaging

"C" III SERIES



Absolute Maximum Ratings

For ratings of individual members of a series, see Device Ratings and Specifications chart

	"C" III SERIES	UNITS
Continuous:		
Steady State AC Voltage Range ($V_{M(AC)RMS}$)	130 to 320	V
Transients:		
Single-Pulse Peak Current (I_{TM}) 8/20μs Wave (See Figure 2)	6000 to 9000	A
Single-Pulse Energy Range (W_{TM}) 2ms Rectangular Wave	45 to 210	J
Maximum Temporary Overvoltage of $V_{M(AC)}$, (5 Minutes Duration)	130 (25°C) 120 (125°C)	% %
Operating Ambient Temperature Range (T_A)	-55 to 85	°C
Storage Temperature Range (T_{STG})	-55 to 125	°C
Temperature Coefficient (αV) of Clamping Voltage (V_C) at Specified Test Current	<0.01	%/°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

"C" III Series Ratings

PART NUMBER	BRAND	MAXIMUM RATINGS (85°C)			
		CONTINUOUS	TRANSIENT		
		MAXIMUM V_{RMS} $V_{M(AC)}$ (V)	WITHSTANDING ENERGY (2ms) W_{TM} (⎍) (J)	PEAK CURRENT (8/20μs) I_{TM1} 1 PULSE (A)	I_{TM2} 2 PULSES (A)
V130LA10C	130L10C	130	45	6000	5000
V130LA20C	130L20C	130	90	9000	7000
V130LA20CX325	130CX325	130	90	9000	7000
V140LA10C	140L10C	140	50	6000	5000
V140LA20C	140L20C	140	100	9000	7000
V140LA20CX340	140CX340	140	100	9000	7000
V150LA10C	150L10C	150	55	6000	5000
V150LA20C	150L20C	150	110	9000	7000
V150LA20CX360	150CX360	150	110	9000	7000
V175LA10C	175L10C	175	60	6000	5000
V175LA20C	175L20C	175	120	9000	7000
V175LA20CX425	175CX425	175	120	9000	7000
V230LA20C	230L20C	230	80	6000	5000
V230LA40C	230L40C	230	160	9000	7000
V230LA40CX570	230X570	230	160	9000	7000
V250LA20C	250L20C	250	100	6000	5000
V250LA40C	250L40C	250	170	9000	7000
V250LA40CX620	250CX620	250	170	9000	7000
V275LA20C	275L20C	275	110	6000	5000
V275LA40C	275L40C	275	190	9000	7000
V275LA40CX680	275CX680	275	190	9000	7000
V300LA20C	300L20C	300	120	6000	5000
V300LA40C	300L40C	300	210	9000	7000
V300LA40CX745	300CX745	300	210	9000	7000
V320LA20C	320L20C	320	130	6000	5000
V320LA40C	320L40C	320	220	9000	7000

"C" III Series Specifications

PART NUMBER	MODEL SIZE DISC DIAMETER (mm)	SPECIFICATIONS (25°C)					
		VARISTOR VOLTAGE AT 1mA DC TEST CURRENT		MAXIMUM CLAMPING VOLTAGE (8/20µs)		DUTY CYCLE SURGE RATING	
		V_N MIN (V)	V_N MAX (V)	V_C (V)	I_P (A)	3kA (8/20µs) # PULSES	750A (8/20µs) # PULSES
V130LA10C	14	184	228	340	50	10	80
V130LA20C	20	184	228	340	100	20	120
V130LA20CX325	20	184	220	325	100	20	120
V140LA10C	14	198	242	360	50	10	80
V140LA20C	20	198	242	360	100	20	120
V140LA20CX340	20	198	230	340	100	20	120
V150LA10C	14	212	268	395	50	10	80
V150LA20C	20	212	268	395	100	20	120
V150LA20CX360	20	212	243	360	100	20	120
V175LA10C	14	247	303	455	50	10	80
V175LA20C	20	247	303	455	100	20	120
V175LA20CX425	20	247	285	425	100	20	120
V230LA20C	14	324	396	595	50	10	80
V230LA40C	20	324	396	595	100	20	120
V230LA40CX570	20	324	384	570	100	20	120
V250LA20C	14	354	429	650	50	10	80
V250LA40C	20	354	429	650	100	20	120
V250LA40CX620	20	354	413	620	100	20	120
V275LA20C	14	389	473	710	50	10	80
V275LA40C	20	389	473	710	100	20	120
V275LA40CX680	20	389	453	680	100	20	120
V300LA20C	14	420	517	775	50	10	80
V300LA40C	20	420	517	775	100	20	120
V300LA40CX745	20	420	490	745	100	20	120
V320LA20C	14	462	565	850	50	10	80
V320LA40C	20	462	565	850	100	20	120

NOTE: Average power dissipation of transients not to exceed 0.6W and 1W for model sizes 14mm and 20mm, respectively.

Power Dissipation Ratings

Continuous power dissipation capability is not an applicable parameter for a varistor. When transients occur in rapid succession, the average power dissipation is the energy (watt-seconds) per pulse times the number of pulses per second. The power so developed must be within the specifications shown on the Device Ratings and Specifications table for the specific device. The operating values of a MOV need to be derated at high temperatures as shown in Figure 1. Because varistors only dissipate a relatively small amount of average power they are not suitable for repetitive applications that involve substantial amounts of average power dissipation.

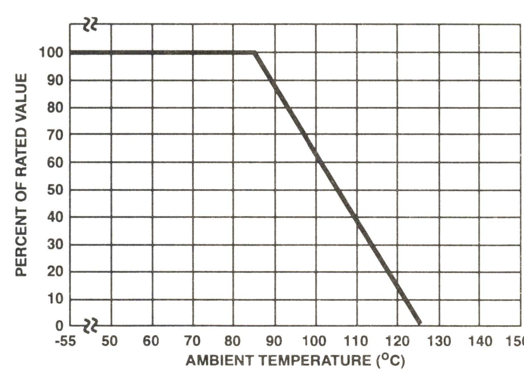


FIGURE 1. CURRENT, ENERGY AND POWER DERATING CURVE

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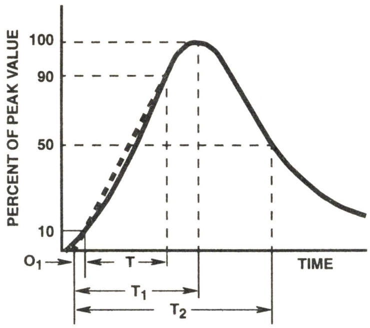
VARISTOR PRODUCTS



O_1 = Virtual Origin of Wave
T = Time From 10% to 90% of Peak
T_1 = Virtual Front time = 1.25 • t
T_2 = Virtual Time to Half Value (Impulse Duration)
Example: For an 8/20μs Current Waveform:
8μs = T_1 = Virtual Front Time
20μs = T_2 = Virtual Time to Half Value

FIGURE 2. PEAK PULSE CURRENT TEST WAVEFORM

Transient V-I Characteristics Curves

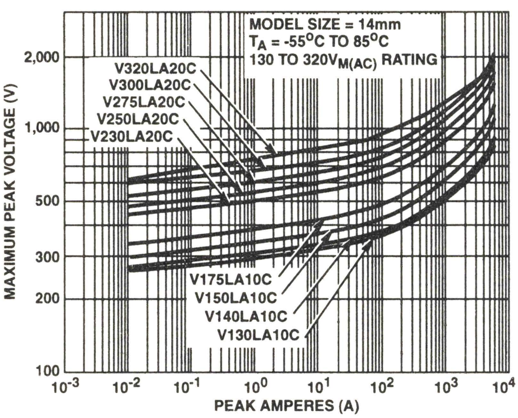


FIGURE 3. MAXIMUM CLAMPING VOLTAGE FOR V130LA10C TO V320LA20C

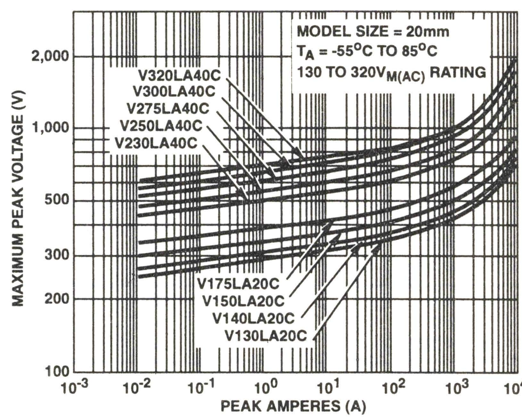


FIGURE 4. MAXIMUM CLAMPING VOLTAGE FOR V130LA20C TO V320LA40C

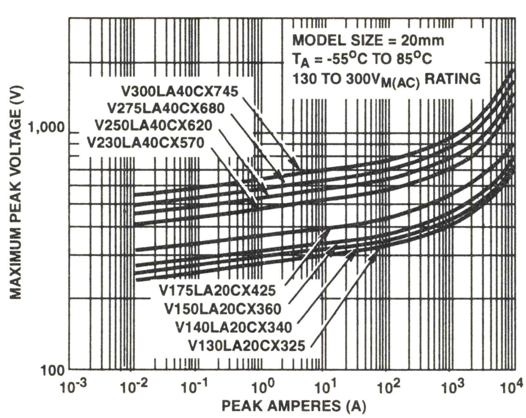


FIGURE 5. MAXIMUM CLAMPING VOLTAGE FOR V130LA20CX325 TO V300LACX745

Pulse Rating Curves

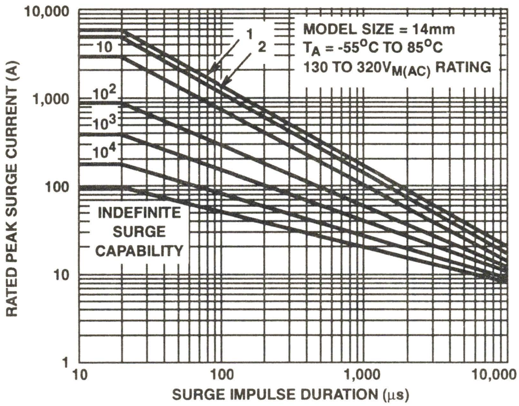


FIGURE 6. REPETITIVE SURGE CAPABILITY FOR V130LA10C TO V320LA20C

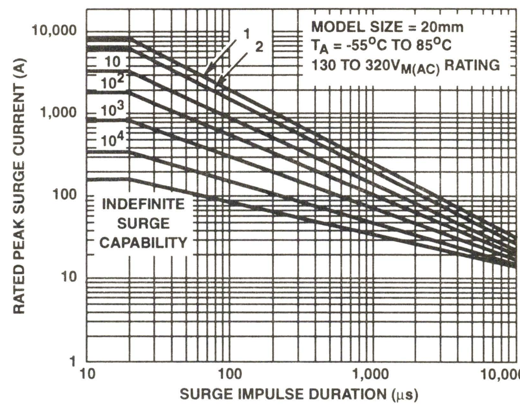
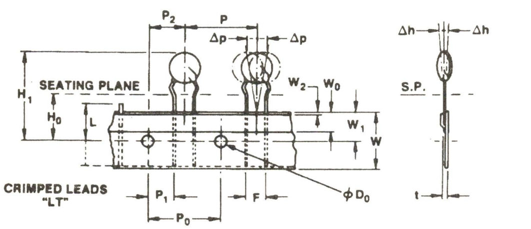
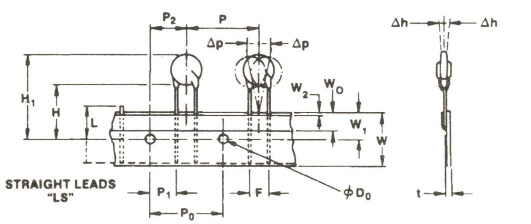
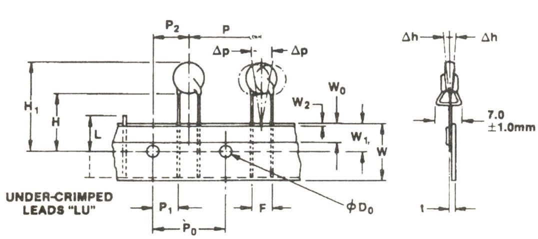


FIGURE 7. REPETITIVE SURGE CAPABILITY FOR V130LA20C TO V320LA40C

Tape and Reel Specification







SYMBOL	DESCRIPTION	MODEL SIZE	
		14mm	20mm
P	Pitch of Component	25.4 ± 1.0	
P_0	Feed Hole Pitch	12.7 ± 0.2	
P_1	Feed Hole Center to Pitch	2.60 ± 0.7	
P_2	Hole Center to Component Center	6.35 ± 1.0	
F	Lead to Lead Distance	7.50 ± 0.8	
h	Component Alignment	2.00 Max	
W	Tape Width	18.25 ± 0.75	
W_0	Hold Down Tape Width	6.00 ± 0.3	12.0 ± 0.3
W_1	Hole Position	9.125 ± 0.625	
W_2	Hold Down Tape Position	0.5 Max	
H	Height From Tape Center To Component Base	19.0 ± 1.0	
H_0	Seating Plane Height	16.0 ± 0.5	
H_1	Component Height	40 Max	46.5 Max
D_0	Feed Hole Diameter	4.0 ± 0.2	
t	Total Tape Thickness	0.7 ± 0.2	
L	Length of Clipped Lead	12.0 Max	
p	Component Alignment	3° Max	

Tape and Reel Data

- Conforms to ANSI and EIA Specifications
- Can be supplied to IEC publication 286-2
- Radial devices on tape and reel are supplied with either crimped leads, straight leads, or under-crimped leads.

Tape and Reel Ordering Information

- Crimped leads are standard on LA types supplied in tape and reel and are denoted by the model letter "T". Also, in tape and reel, model letter "S" denotes straight leads and letter "U" denotes special under-crimped leads.

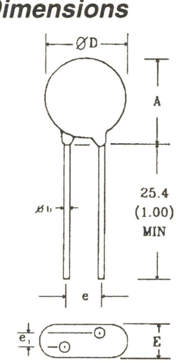
Example:

STANDARD MODEL	CRIMPED LEADS	STRAIGHT LEADS	UNDER CRIMP LEADS
V130LA20C	V130LT20C	V130LS20C	V130LU20C

Shipping Quantity

DEVICE SIZE	QUANTITY PER REEL		
	"T" REEL	"S" REEL	"U" REEL
14mm	500	500	500
20mm	500	500	500

Mechanical Dimensions



SYMBOL	VARISTOR MODEL SIZE			
	14mm		20mm	
	MIN	MAX	MIN	MAX
A	13.5 (0.531)	20 (0.787)	17.5 (0.689)	26.5 (1.043)
ØD	13.5 (0.531)	17 (0.669)	17.5 (0.689)	23 (0.906)
e	6.5 (0.256)	8.5 (0.335)	6.5 (0.256)	8.5 (0.335)
e1	1.5 (0.059)	3.5 (0.138)	1.5 (0.059)	3.5 (0.138)
E	- -	5.6 (0.220)	- -	5.6 (0.220)
Øb	0.76 (0.030)	0.86 (0.034)	0.76 (0.030)	0.86 (0.034)

Dimensions are in millimeters (inches)

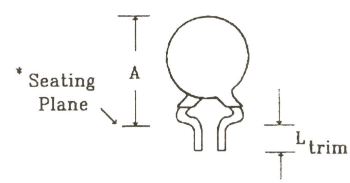
NOTE: 10mm lead spacing also available. See additional lead style options.

Additional Lead Style Options

Radial lead types can be supplied with combination pre-formed crimp and trimmed leads. This option is supplied to the dimensions shown below.

SYMBOL	VARISTOR MODEL SIZE			
	14mm		20mm	
	MIN	MAX	MIN	MAX
A	-	24.5 (0.96)	-	31 (1.22)
L_{TRIM}	2.41 (0.095)	4.69 (0.185)	2.41 (0.095)	4.69 (0.185)

NOTE: Dimensions are in millimeters (inches)



CRIMPED AND TRIMMED LEAD

*Seating plane interpretation per IEC-717

- To order this crimped and trimmed lead style, the standard radial type model number "LA" is changed to the model number "LC". This option is supplied in bulk only.

Example:

STANDARD MODEL	ORDER AS
V130LA20C	V130LC20C

- For 10 ± 1mm lead spacing on 20mm units only; append standard model numbers by adding "X10" suffix.

Example:

STANDARD MODEL	ORDER AS
V130LA20C	V130LA20CX10

- For other lead style variations to the above, please contact Harris Semiconductor Power Marketing

The Origins of Surge Overvoltages

There are a wide variety of transient overvoltage environments, each with radically different levels of exposure. Transients may be caused by lightning, which can inject very high currents into the electrical system, or by switching transients. Lightning strikes usually occur to the primary transmission lines with resulting coupling to the secondary line through mutual inductive or capacitive coupling. Even a lightning hit that misses the primary AC line can induce substantial voltage onto the primary conductors, triggering lightning arresters and thus creating transients.

Switching transients, while of a lower magnitude than lightning, occur more frequently and thus are of a greater threat to the AC system. Switching transients may result from fuse blowing, capacitor bank switching, fault clearing or grid switching.

Field studies and laboratory investigation of residential and industrial low power AC voltage systems have shown that the amplitude of a transient is proportional to the rate of its occurrence, i.e. lower magnitude transients occur most often. Governing bodies, in particular IEC, UL, IEEE and ANSI have established guidelines on the transient environment one may expect to encounter in a low voltage AC power system. Table 1 reflects the surge voltages and currents deemed to represent the indoor environment.

LOCATION CATEGORY		TRANSIENT WAVEFORM/MAGNITUDE	
A	Long Branch Circuits and Outlets	0.5µs 100kHz	6kV 200A
B	Major Feeders and Short Branch Circuits	1.2/50µs 8/20µs	6kV 3kA
		0.5µs 100kHz	6kV 500A

"C" III MOV Series

The "C" III series of Harris radial MOVs represent the third generation of improvements in device performance and characteristics. The technology effort involved in the development of this new series concentrated on extending the existing performance and capability of the Harris second generation of metal oxide varistors.

The characteristics of greatest importance for a metal oxide varistor in an AC surge environment are the peak current, energy handling, repetitive surge and temporary over-voltage capabilities. The focus of the design effort was on improving these characteristics and therefore offering the maximum protection presently available to the end user.

The "C" III series are designed to survive the harsh environments of the AC low-power indoor environment. Their much improved surge withstand capability is well in excess of the transients expected in the AC mains environment. Further design rules for the development of the "C" III series included considerations of the expected steady state operating conditions and the repetitive surge environment.

Investigation of the AC low-power indoor environment show that most transients occur where the power enters the building and at major feeders and short branch circuits. Surges recorded at this service entrance, location Category B from C62.41-1992, may be both oscillatory and unidirectional in nature. The typical "lightning surge" has been established as a 1.2/50µs voltage wave and a 8/20µs current wave. A short circuit current of 3000A and open circuit voltage 6000V are the expected worst case transients at this location.

TEST	REFERENCE STANDARD	TEST CONDITIONS	TEST RESULTS
Surge Current	UL 1449 IEEE/ANSI C62.41	9000A (8/20µs) 1 Pulse	0/165
	IEC 1051	7000A (8/20µs) 2 Pulses	0/105
		3000A (8/20µs) 20 Pulses	0/75
		750A (8/20µs) 120 Pulses	0/65
Surge Energy	UL 1449 IEEE/ANSI C62.41 IEC 1051	90J (2ms) 1 Pulse	0/125
Operating Life	Mil-Std-202 Method 204D	125°C, 1000 Hours, Rated Bias Voltage	0/180
Temporary Overvoltage	N/A	120% Maximum Rated Varistor Voltage For 5 minutes	0/70

The further into the facility one goes, the lower the magnitude of the transients encountered. ANSI/IEEE C62.41 differentiates between the service entrance and the interior of a facility. Per this specification, the internal location or long branch circuits and outlets are classified as Location Category A. The transients encountered here have oscillatory waveshapes with frequency ranges from 5kHz to 500kHz; with 100kHz deemed most common. Transients of the magnitude of 500A are expected in this location.

Reliability Performance of "C" III Series

The electrical ratings of the "C" III series of MOVs are conservatively stated. Samples of these devices have been tested under additional stresses, over and above those called out in the datasheet. The results of this testing show an enhanced device performance.

The series of stress tests to which the units were subjected are a combination of electrical, environmental and mechanical tests. A summary of the reliability tests performed on the "C" III series are described in Table 2.

AC Bias Reliability

The "C" III series of metal oxide varistors was designed for use on the AC line. The varistor is connected across the AC line and is biased with a constant amplitude sinusoidal volt-

4

VARISTOR PRODUCTS

age. It should be noted that the definition of failure is a shift in the nominal varistor voltage (V_N) exceeding $\pm$ 10%. Although this type of varistor is still functioning normally after this magnitude of shift, devices at the lower extremities of V_N tolerance will begin to dissipate more power.

Because of this possibility, an extensive series of statistically designed tests were performed to determine the reliability of the "C" III type of varistor under AC bias combined with high levels of temperature stress. To date, this test has generated over 50,000 device hours of operation at a temperature of 125°C, although only rated at 85°C. Changes in the nominal varistor voltage, measured at 1mA, of less than 2% have been recorded (Figure 8).

Transient Surge Current/Energy Capability

The transient surge rating serves as an excellent figure of merit for the "C" III suppressor. This inherent surge handling capability is one of the "C" III suppressor's best features. The enhanced surge absorption capability results from improved process uniformity and enhanced construction. The homogeneity of the raw material powder and improved control over the sintering and assembly processes are contributing factors to this improvement.

In the low power AC mains environment, industry governing bodies (UL, IEC, NEMA and IEEE) all suggest that the worst case surge occurrence will be 3kA. Such a transient event may occur up to five times over the equipment life time (approximately 10 years). While the occurrences of five 3 kiloamps transients is the required capability, the conservatively rated, repetitive surge current for the "C" III series is 20 pulses for the 20mm units and 10 pulses for the 14mm series.

As a measure of the inherent device capability, samples of the 20mm V130LA20C devices were subjected to a worst case repetitive transient surges test. After 100 pulses, each of 3kA, there was negligible change in the device characteristics. Changes in the clamping voltage, measured at 100 amps, of less than 3% were recorded (Figure 9). Samples of the 14mm Series V175LA20C were subjected to repetitive surge occurrences of 750A. Again, there was negligible changes in any of the device characteristics after 250 pulses (Figure 10). In both cases the inherent device capability is far in excess of the expected worst case scenario.

Terms and Descriptions

Rated AC Voltage ($V_{M(AC)RMS}$)

This is the maximum continuous sinusoidal voltage which may be applied to the MOV. This voltage may be applied at any temperature up to the maximum operating temperature of 85°C.

Maximum Non-Repetitive Surge Current (I_{TM})

This is the maximum peak current which may be applied for an 8/20μs impulse, with rated line voltage also applied, without causing device failure. (See Figure 2)

Maximum Non-Repetitive Surge Energy (W_{TM})

This is the maximum rated transient energy which may be dissipated for a single current pulse at a specified impulse and duration (2ms), with the rated V_{RMS} applied, without causing device failure.

Nominal Voltage ($V_{N(DC)}$)

This is the voltage at which the device changes from the off state to the on state and enters its conduction mode of operation. This voltage is characterized at the 1mA point and has specified minimum and maximum voltage levels.

Clamping Voltage (V_C)

This is the peak voltage appearing across the MOV when measured at conditions of specified pulse current amplitude and specified waveform (8/20μs)

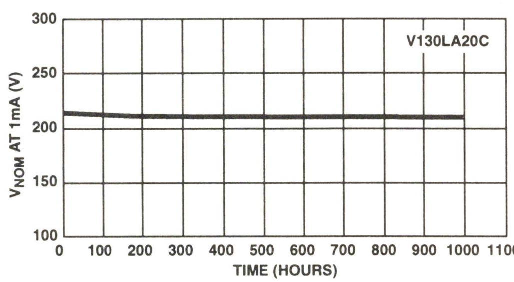


FIGURE 8. HIGH TEMPERATURE OPERATING LIFE 125°C FOR 1000 HOURS AT RATED BIAS

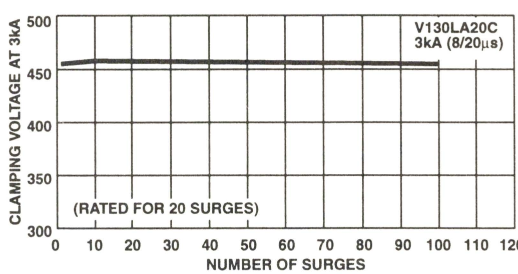


FIGURE 9. TYPICAL REPETITIVE SURGE CURRENT CAPABILITY OF "C" III SERIES MOVs

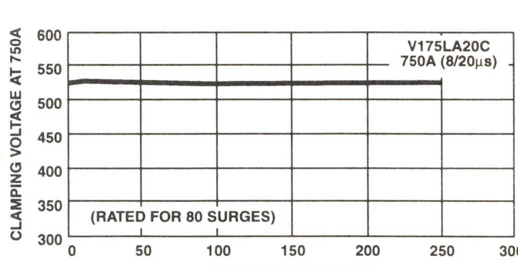


FIGURE 10. TYPICAL REPETITIVE SURGE CURRENT CAPABILITY OF "C" III SERIES MOVs

ZA Series

Radial Lead Metal-Oxide Varistors for Low to Medium Voltage Operation

January 1998

Features

- Recognized as "Protectors for Data Communications and Fire Alarm Circuits", UL File #E135010 to Std. 497B
- Wide Operating Voltage Range $V_{M(AC)RMS}$ . . 4V to 460V
- DC Voltage Ratings . . . . 5.5V to 615V
- No Derating Up to 85°C Ambient
- 5 Model Sizes Available. . . . . . . 5, 7, 10, 14, and 20mm
- Radial-Lead Package for Hard-Wired or Printed Circuit Board Designs
- Available in Tape and Reel or Bulk Pack
- Standard Lead Form Options

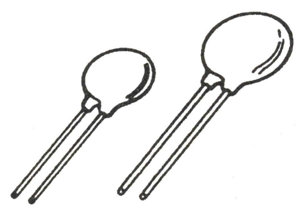
Description

The ZA Series of transient voltage surge suppressors are radial-lead varistors (MOVs) designed for use in the protection of low and medium-voltage circuits and systems. Typical applications include motor control, telecom, automotive systems, solenoid, and power supply circuits to protect circuit board components and maintain data integrity.

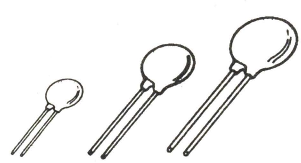
These devices are available in five model sizes: 5mm, 7mm, 10mm, 14mm and 20mm, and feature a wide V_{DC} voltage range of 5.5V to 615V.

See ZA Series Device Ratings and Specifications table for part number and brand information.

Packaging



14mm, 20mm



5mm, 7mm, 10mm

Absolute Maximum Ratings

For ratings of individual members of a series, see Device Ratings and Specifications chart

	ZA SERIES	UNITS
Continuous:		
Steady State Applied Voltage:		
AC Voltage Range ($V_{M(AC)RMS}$)	4 to 460	V
DC Voltage Range ($V_{M(DC)}$)	5.5 to 615	V
Transient:		
Peak Pulse Current (I_{TM})		
For 8/20µs Current Wave (See Figure 2)	50 to 6500	A
Single Pulse Energy Range (Note 1)		
For 10/1000µs Current Wave (W_{TM})	0.1 to 52	J
Operating Ambient Temperature Range (T_A)	-55 to 85	°C
Storage Temperature Range (T_{STG})	-55 to 125	°C
Temperature Coefficient (αV) of Clamping Voltage (V_C) at Specified Test Current	<0.01	%/°C
Hi-Pot Encapsulation (Isolation Voltage Capability)	2500	V
(Dielectric must withstand indicated DC voltage for one minute per MIL-STD 202, Method 301)		
Insulation Resistance	1000	MΩ

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Device Ratings and Specifications (Note 1)

ZA Series Varistors are listed under UL File No. E135010 as a UL recognized component.

PART NUMBER	MODEL SIZE DISC DIA. (mm)	BRAND	MAXIMUM RATING (85°C) CONTINUOUS V_{RMS} $V_{M(AC)}$ (V)	CONTINUOUS V_{DC} $V_{M(DC)}$ (V)	TRANSIENT ENERGY 10 x 1000µs W_{TM} (J)	TRANSIENT PEAK CURRENT 8 x 20µs I_{TM} (A)	SPECIFICATIONS (25°C) VARISTOR VOLTAGE AT 1mA DC TEST CURRENT V_{NOM} MIN (V)	V_{NOM} MAX (V)	MAXIMUM CLAMPING VOLTAGE 8 x 20µs V_C (V)	I_{PK} (A)	TYPICAL CAPACITANCE f = 1MHz C (pF)
V8ZA05	5	Z08	4	5.5	0.1	50	6	11	30	1	1400
V8ZA1	7	08Z1	4	5.5	0.4	100	6	11	22	2.5	3000
V8ZA2	10	08Z2	4	5.5	0.8	250	6	11	20	5	7500
V12ZA05	5	Z12	6	8	0.14	50	9	16	37	1	1200
V12ZA1	7	12Z1	6	8	0.6	100	9	16	34	2.5	2500
V12ZA2	10	12Z2	6	8	1.2	250	9	16	30	5	6000
V18ZA05	5	Z18	10	14	0.17	100	14.4	21.6	36	1	1000
V18ZA1	7	18Z1	10	14	0.8	250	14.4	21.6	36	2.5	2000
V18ZA2	10	18Z2	10	14	1.5	500	14.4	21.6	36	5	5000
V18ZA3	14	18Z3	10	14	3.5	1000	14.4	21.6	36	10	11000
V18ZA40	20	18Z40	10	14	80 (Note 2)	2000	14.4 (Note 3)	21.6	37	20	22000
V22ZA05	5	Z22	14	18	0.2	100	18.7	26	43	1	800
V22ZA1	7	22Z1	14	18	0.9	250	18.7	26	43	2.5	1600
V22ZA2	10	22Z2	14	18	2	500	18.7	26	43	5	4000
V22ZA3	14	22Z3	14	18	4	1000	18.7	26	43	10	9000
V24ZA50	20	24Z50	14	18 (Note 4)	100 (Note 2)	2000	19.2 (Note 3)	26	43	20	18000

Device Ratings and Specifications (Note 1) (Continued)

ZA Series Varistors are listed under UL File No. E135010 as a UL recognized component.

PART NUMBER	MODEL SIZE DISC DIA. (mm)	BRAND	MAXIMUM RATING (85°C) CONTINUOUS V_{RMS} $V_{M(AC)}$ (V)	MAXIMUM RATING (85°C) CONTINUOUS V_{DC} $V_{M(DC)}$ (V)	MAXIMUM RATING (85°C) TRANSIENT ENERGY 10 x 1000µs W_{TM} (J)	MAXIMUM RATING (85°C) TRANSIENT PEAK CURRENT 8 x 20µs I_{TM} (A)	SPECIFICATIONS (25°C) VARISTOR VOLTAGE AT 1mA DC TEST CURRENT V_{NOM} MIN (V)	SPECIFICATIONS (25°C) VARISTOR VOLTAGE AT 1mA DC TEST CURRENT V_{NOM} MAX (V)	MAXIMUM CLAMPING VOLTAGE 8 x 20µs V_C (V)	MAXIMUM CLAMPING VOLTAGE 8 x 20µs I_{PK} (A)	TYPICAL CAPACITANCE f = 1MHz C (pF)
V27ZA05	5	Z27	17	22	0.25	100	23	31.1	53	1	600
V27ZA1	7	27Z1	17	22	1	250	23	31.1	53	2.5	1300
V27ZA2	10	27Z2	17	22	2.5	500	23	31.1	53	5	3000
V27ZA4	14	27Z4	17	22	5	1000	23	31.1	53	10	7000
V27ZA60	20	27Z60	17	22	120 (Note 2)	2000	23 (Note 3)	31.1	50	20	13000
V33ZA05	5	Z33	20	26	0.3	100	29.5	38	65	1	500
V33ZA1	7	33Z1	20	26	1.2	250	29.5	36.5	65	2.5	1100
V33ZA2	10	33Z2	20	26	3	500	29.5	36.5	65	5	2700
V33ZA5	14	33Z5	20	26	6	1000	29.5	36.5	65	10	6000
V33ZA70	20	33Z70	21	27	150 (Note 2)	2000	29.5 (Note 3)	36.5	58	20	13000
V36ZA80	20	36Z80	23	31	160 (Note 2)	2000	32 (Note 3)	40	63	20	12000
V39ZA05	5	Z39	25	31	0.3	100	35	46	79	1	500
V39ZA1	7	39Z1	25	31	1.2	250	35	43	79	2.5	1100
V39ZA3	10	39Z3	25	31	3	500	35	43	76	5	2700
V39ZA6	14	39Z6	25	31	6	1000	35	43	76	10	6000
V39ZA20	20	39Z20	25	31	20	2000	35	43	76	20	12000
V47ZA05	5	Z47	30	38	0.4	100	42	55	93	1	400
V47ZA1	7	47Z1	30	38	1.8	250	42	52	93	2.5	800
V47ZA3	10	47Z3	30	38	4.5	500	42	52	93	5	2000
V47ZA7	14	47Z7	30	38	8.8	1000	42	52	93	10	4500
V47ZA20	20	47Z20	30	38	23	2000	42	52	93	20	11000
V56ZA05	5	Z56	35	45	0.5	100	50	66	110	1	360
V56ZA2	7	56Z2	35	45	2.3	250	50	62	110	2.5	700
V56ZA3	10	56Z3	35	45	5.5	500	50	62	110	5	1800
V56ZA8	14	56Z8	35	45	10	1000	50	62	110	10	3900
V56ZA20	20	56Z20	35	45	30	2000	50	62	110	20	10000
V68ZA05	5	Z68	40	56	0.6	100	61	80	135	1	300
V68ZA2	7	68Z2	40	56	3	250	61	75	135	2.5	600
V68ZA3	10	68Z3	40	56	6.5	500	61	75	135	5	1500
V68ZA10	14	68Z10	40	56	13	1000	61	75	135	10	3300
V68ZA20	20	68Z20	40	56	33	2000	61	75	135	20	10000
V82ZA05	5	Z82	50	68	2	400	73	97	135	5	240
V82ZA2	7	82Z2	50	68	4	1200	73	91	135	10	500
V82ZA4	10	82Z4	50	68	8	2500	73	91	135	25	1100
V82ZA12	14	82Z12	50	68	15	4500	73	91	145	50	2500

Device Ratings and Specifications (Note 1) **(Continued)**

ZA Series Varistors are listed under UL File No. E135010 as a UL recognized component.

			MAXIMUM RATING (85°C)				SPECIFICATIONS (25°C)				
			CONTINUOUS		TRANSIENT						
			V_{RMS}	V_{DC}	ENERGY 10 x 1000µs	PEAK CURRENT 8 x 20µs	VARISTOR VOLTAGE AT 1mA DC TEST CURRENT		MAXIMUM CLAMPING VOLTAGE 8 x 20µs		TYPICAL CAPACITANCE f = 1MHz
PART NUMBER	MODEL SIZE DISC DIA. (mm)	BRAND	$V_{M(AC)}$ (V)	$V_{M(DC)}$ (V)	W_{TM} (J)	I_{TM} (A)	V_{NOM} MIN (V)	V_{NOM} MAX (V)	V_C (V)	I_{PK} (A)	C (pF)
V100ZA05	5	Z100	60	81	2.5	400	90	117	165	5	180
V100ZA3	7	100Z	60	81	5	1200	90	110	165	10	400
V100ZA4	10	100Z4	60	81	10	2500	90	110	165	25	900
V100ZA15	14	100Z15	60	81	20	4500	90	110	175	50	2000
V120ZA05	5	Z120	75	102	3	400	108	138	205	5	140
V120ZA1	7	120Z	75	102	6	1200	108	132	205	10	300
V120ZA4	10	120Z4	75	102	12	2500	108	132	200	25	750
V120ZA6	14	120Z6	75	102	22	4500	108	132	210	50	1700
V120ZA20	20	120Z20	75	102	33	6500	108	132	210	100	1500
V150ZA05	5	Z150	92	127	4	400	135	173	250	5	120
V150ZA1	7	Z051	95	127	8	1200	135	165	250	10	250
V150ZA4	10	150Z4	95	127	15	2500	135	165	250	25	600
V150ZA8	14	150Z8	95	127	20	4500	135	165	250	50	1400
V150ZA20	20	150Z20	95	127	45	6500	135	165	250	100	1000
V180ZA05	5	Z180	110	153	5	400	162	207	295	5	100
V180ZA1	7	180Z	115	153	10	1200	162	198	300	10	200
V180ZA5	10	180Z5	115	153	18	2500	162	198	300	25	500
V180ZA10	14	180Z10	115	153	35	4500	162	198	300	50	1100
V180ZA20	20	180Z20	115	153	52	6500	162	198	300	100	2400
V205ZA05	5	Z205	130	170	5.5	400	184	226	340	5	100
† V220ZA05	5	Z220	140	180	6	400	198	253	360	5	90
V240ZA05	5	Z240	150	200	7	400	216	264	395	5	80
† V270ZA05	5	Z270	175	225	7.5	400	243	311	455	5	70
† V330ZA05	5	Z330	210	275	9	400	297	380	540	5	60
V360ZA05	5	Z360	230	300	9.5	400	324	396	595	5	55
† V390ZA05	5	Z390	250	330	10	400	351	449	650	5	50
† V430ZA05	5	Z430	275	369	11	400	387	495	710	5	45
V470ZA05	5	Z470	300	385	12	400	420	517	775	5	35
V620ZA05	5	Z620	385	505	13	400	558	682	1025	5	33
† V680ZA05	5	Z680	420	560	14	400	610	748	1120	5	32
V715ZA05	5	Z715	440	585	15.5	400	643	787	1180	5	31
V750ZA05	5	Z750	460	615	17	400	675	825	1240	5	30

NOTES:

1. Average power dissipation of transients not to exceed 0.2W, 0.25W, 0.4W, 0.6W or 1W for model sizes 5mm, 7mm, 10mm, 14mm and 20mm, respectively.
2. Energy rating for impulse duration of 30ms minimum to one half of peak current (auto load dump).
3. 10mA DC test current.
4. Also rated to withstand 24V for 5 minutes.
5. Higher voltages available, contact Harris Semiconductor Power Marketing.

† Also listed to UL1449 "Transient Voltage Surge Suppressors" File #E75961.

Power Dissipation Ratings

Continuous power dissipation capability is not an applicable design parameter for a suppressor. When transients occur in rapid succession, the average power dissipation required is simply the energy (watt-seconds) per pulse times the number of pulses per second. The power so developed must be within the specifications shown on the Device Ratings and Specifications table for the specific device. Furthermore, the operating values need to be derated at high temperatures as shown in Figure 1. Because varistors can only dissipate a relatively small amount of average power they are, therefore, not suitable for repetitive applications that involve substantial amounts of average power dissipation.

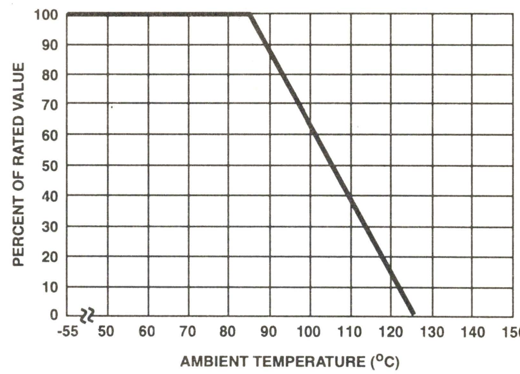
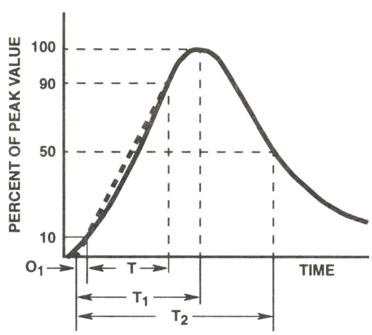


FIGURE 1. CURRENT, ENERGY AND POWER DERATING CURVE



O_1 = Virtual Origin of Wave
T = Time From 10% to 90% of Peak
T_1 = Virtual Front time = 1.25 • t
T_2 = Virtual Time to Half Value (Impulse Duration)
Example: For an 8/20μs Current Waveform:
8μs = T_1 = Virtual Front Time
20μs = T_2 = Virtual Time to Half Value

FIGURE 2. PEAK PULSE CURRENT TEST WAVEFORM

Transient V-I Characteristics Curves

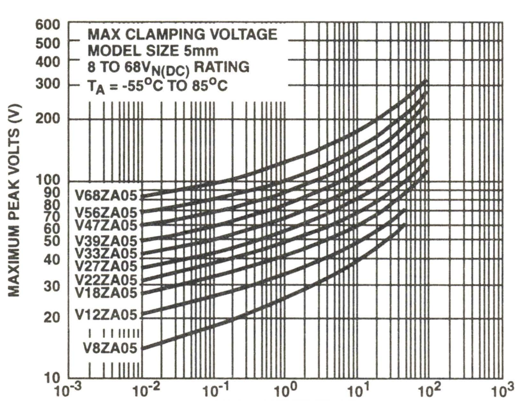


FIGURE 3. CLAMPING VOLTAGE FOR V8ZA05 - V68ZA05

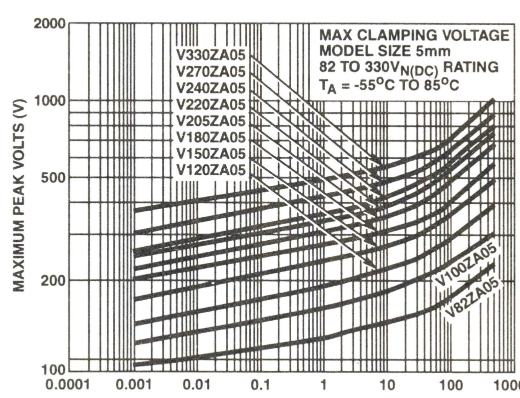


FIGURE 4. CLAMPING VOLTAGE FOR V82ZA05 - V330ZA05

4
VARISTOR PRODUCTS

Transient V-I Characteristics Curves (Continued)

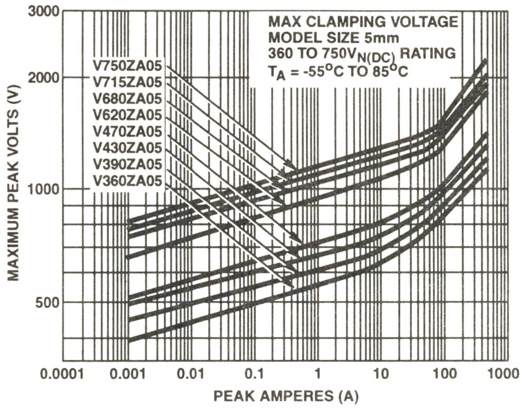


FIGURE 5. CLAMPING VOLTAGE FOR V360ZA05 - V750ZA05

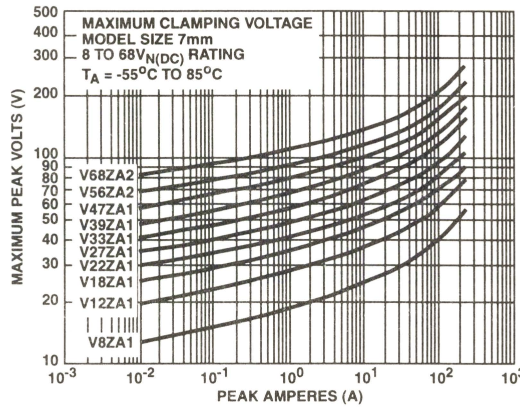


FIGURE 6. CLAMPING VOLTAGE FOR V8ZA1 - V68ZA2

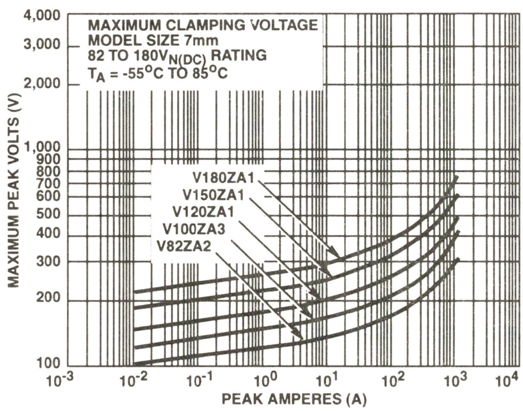


FIGURE 7. CLAMPING VOLTAGE FOR V82ZA2 - V180ZA1

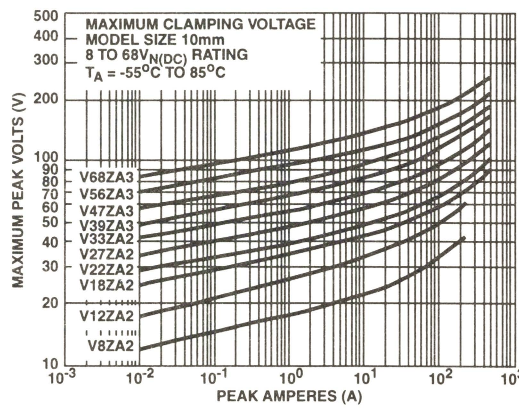


FIGURE 8. CLAMPING VOLTAGE FOR V8ZA2 - V68ZA3

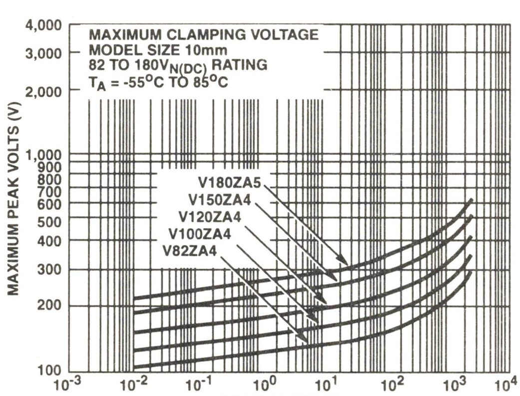


FIGURE 9. CLAMPING VOLTAGE FOR V82ZA4 - V180ZA5

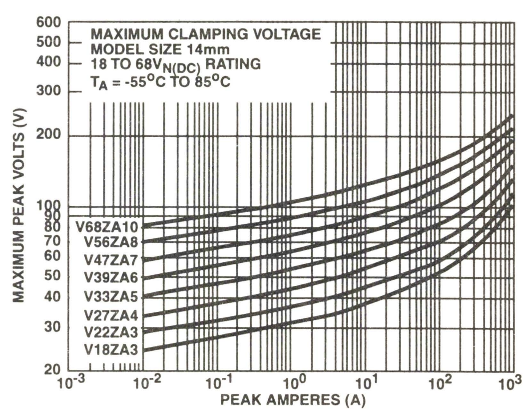


FIGURE 10. CLAMPING VOLTAGE FOR V18ZA3 - V68ZA10

Transient V-I Characteristics Curves (Continued)

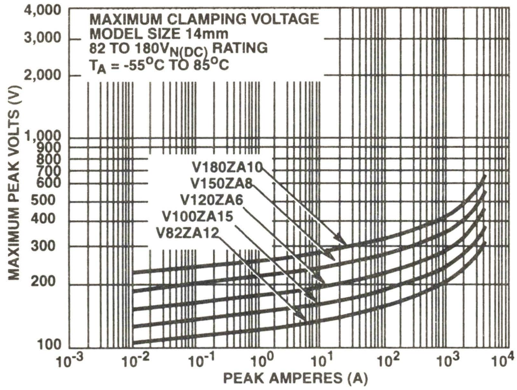


FIGURE 11. CLAMPING VOLTAGE FOR V82ZA12 - V180ZA10

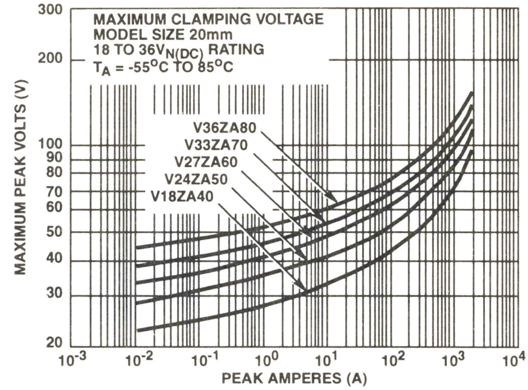


FIGURE 12. CLAMPING VOLTAGE FOR V18ZA40 - V36ZA80

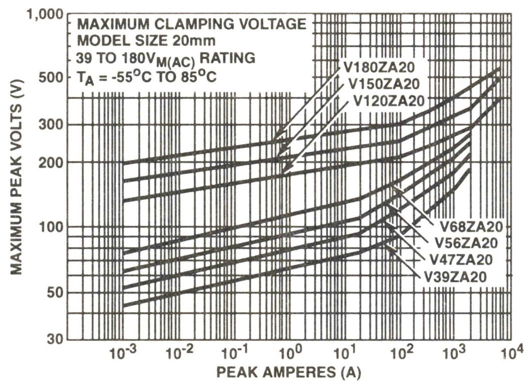


FIGURE 13. CLAMPING VOLTAGE FOR V39ZA20 - V180ZA20

Pulse Rating Curves

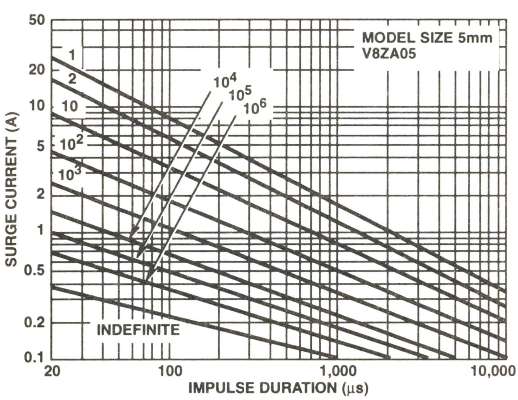


FIGURE 14. SURGE CURRENT RATING CURVES FOR V8ZA05

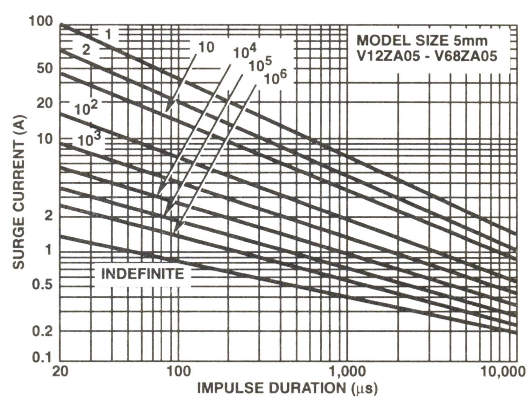


FIGURE 15. SURGE CURRENT RATING CURVES FOR V12ZA05 - V68ZA05

Pulse Rating Curves (Continued)

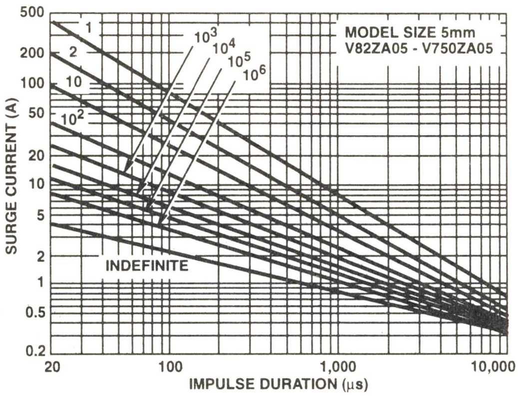


FIGURE 16. SURGE CURRENT RATING CURVES FOR V82ZA05 - V750ZA05

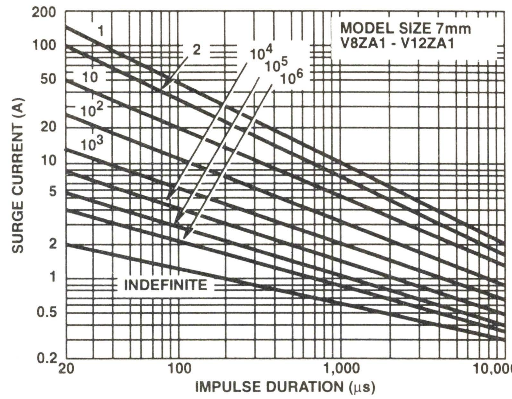


FIGURE 17. SURGE CURRENT RATING CURVES FOR V8ZA1 - V12ZA1

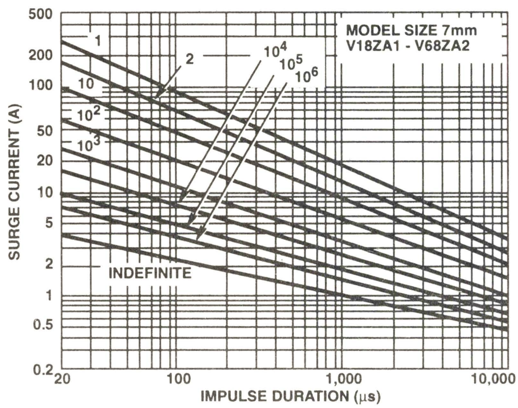


FIGURE 18. SURGE CURRENT RATING CURVES FOR V18ZA1 - V68ZA2

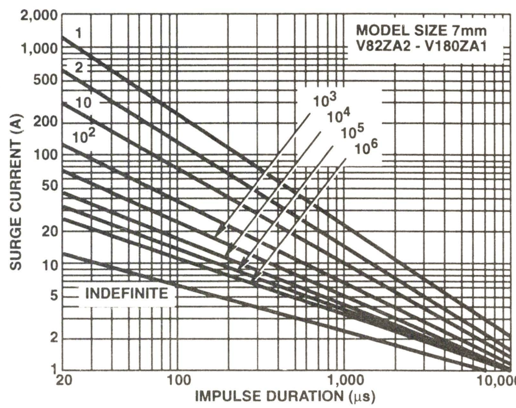


FIGURE 19. SURGE CURRENT RATING CURVES FOR V82ZA2 - V180ZA1

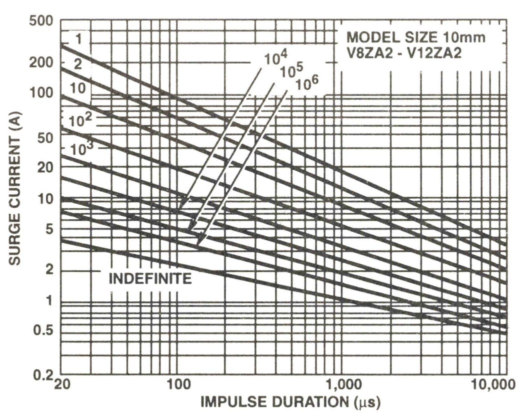


FIGURE 20. SURGE CURRENT RATING CURVES FOR V8ZA2 - V127ZA2

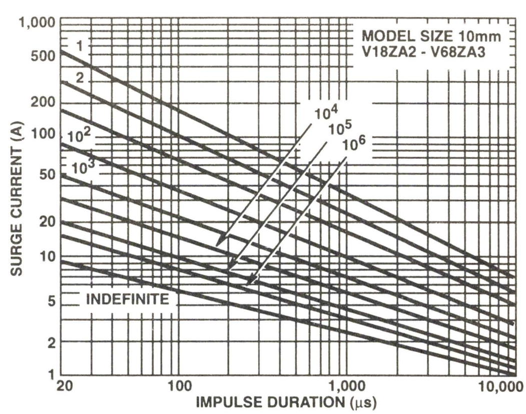


FIGURE 21. SURGE CURRENT RATING CURVES FOR V18ZA2 - V68ZA3

Pulse Rating Curves (Continued)

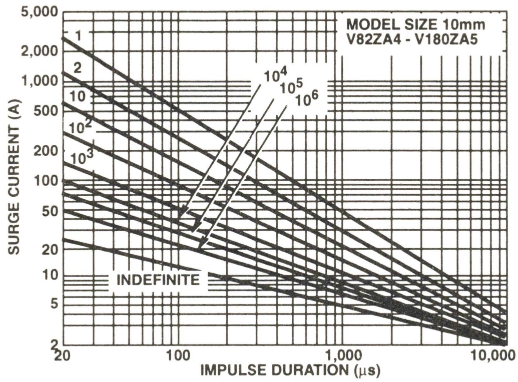


FIGURE 22. SURGE CURRENT RATING CURVES FOR V82ZA4 - V180ZA5

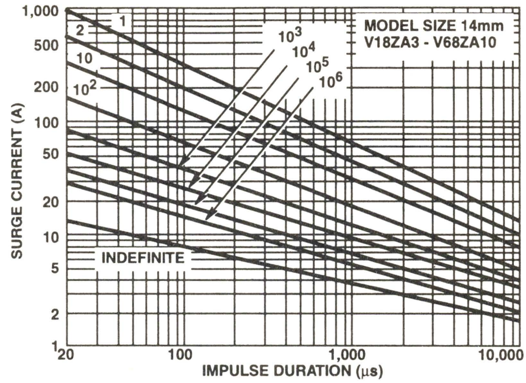


FIGURE 23. SURGE CURRENT RATING CURVES FOR V18ZA3 - V68ZA10

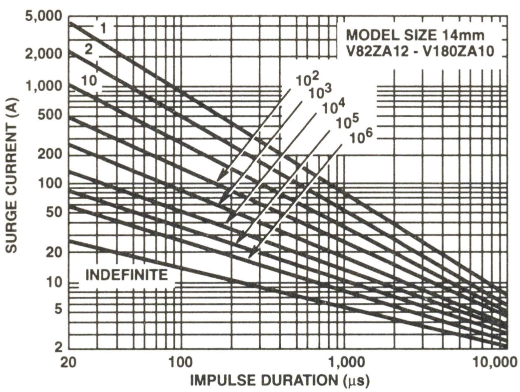


FIGURE 24. SURGE CURRENT RATING CURVES FOR V82ZA12 - V180ZA10

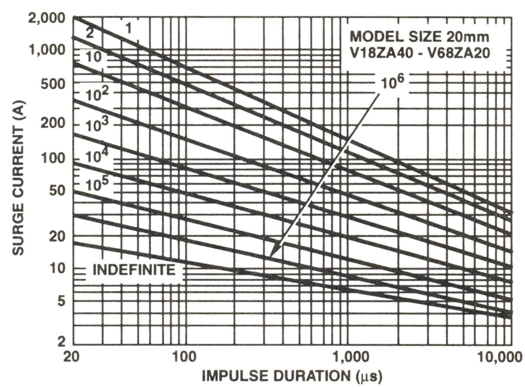


FIGURE 25. SURGE CURRENT RATING CURRENT FOR V18ZA40 - V68ZA20

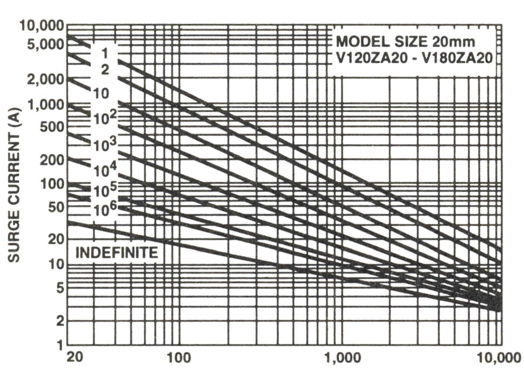
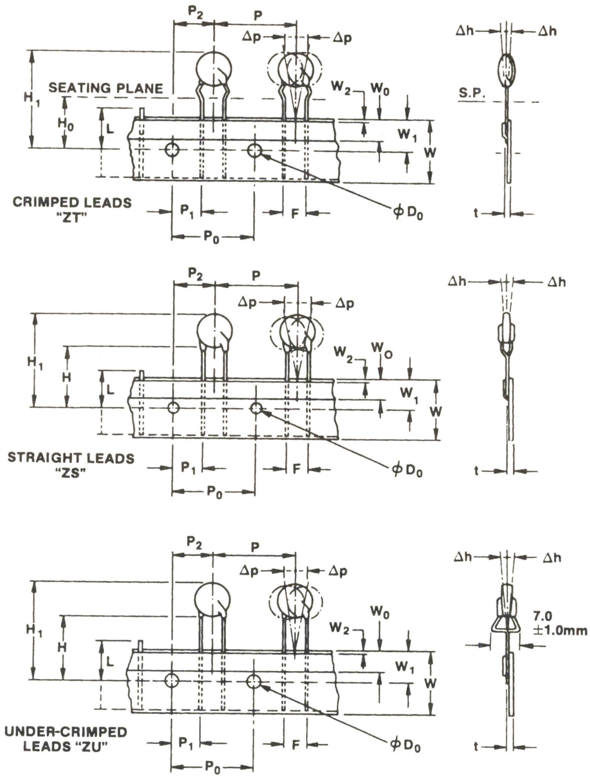


FIGURE 26. SURGE CURRENT RATING CURVES FOR V120ZA20 - V180ZA20

NOTE: If pulse ratings are exceeded, a shift of $V_{N(DC)}$ (at specified current) of more than ±10% could result. This type of shift, which normally results in a decrease of $V_{N(DC)}$, may result in the device not meeting the original published specifications, but it does not prevent the device from continuing to function, and to provide ample protection.

Tape and Reel Specifications



Tape and Reel Data

- Conforms to ANSI and EIA specifications
- Can be supplied to IEC Publication 286-2
- Radial devices on tape are supplied with crimped leads, straight leads, or under-crimped leads

SYMBOL	PARAMETER	MODEL SIZE 5mm	7mm	10mm	14mm	20mm
P	Pitch of Component	12.7 ± 1.0	12.7 ± 1.0	25.4 ± 1.0	25.4 ± 1.0	25.4 ± 1.0
P_0	Feed Hole Pitch	12.7 ± 0.2	12.7 ± 0.2	12.7 ± 0.2	12.7 ± 0.2	12.7 ± 0.2
P_1	Feed Hole Center to Pitch	3.85 ± 0.7	3.85 ± 0.7	2.6 ± 0.7	2.6 ± 0.7	2.6 ± 0.7
P_2	Hole Center to Component Center	6.35 ± 1.0	6.35 ± 1.0	6.35 ± 1.0	6.35 ± 1.0	6.35 ± 1.0
F	Lead to Lead Distance	5.0 ± 1.0	5.0 ± 1.0	7.5 ± 1.0	7.5 ± 1.0	7.5 ± 1.0
Δh	Component Alignment	2.0 Max	2.0 Max	2.0 Max	2.0 Max	2.0 Max
W	Tape Width	18.0 + 1.0 18.0 - 0.5	18.0 + 1.0 18.0 - 0.5	18.0 + 1.0 18.0 - 0.5	18.0 + 1.0 18.0 - 0.5	18.0 + 1.0 18.0 - 0.5
W_0	Hold Down Tape Width	6.0 ± 0.3	6.0 ± 0.3	6.0 ± 0.3	6.0 ± 0.3	12.0 ± 0.3
W_1	Hole Position	9.0 + 0.75 9.0 - 0.50	9.0 + 0.75 9.0 - 0.50	9.0 + 0.75 9.0 - 0.50	9.0 + 0.75 9.0 - 0.50	9.0 + 0.75 9.0 - 0.50
W_2	Hold Down Tape Position	0.5 Max	0.5 Max	0.5 Max	0.5 Max	0.5 Max
H	Height from Tape Center to Component Base	18.0 + 2.0 18.0 - 0.0	18.0 + 2.0 18.0 - 0.0	18.0 + 2.0 18.0 - 0.0	18.0 + 2.0 18.0 - 0.0	18.0 + 2.0 18.0 - 0.0
H_0	Seating Plane Height	16.0 ± 0.5	16.0 ± 0.5	16.0 ± 0.5	16.0 ± 0.5	16.0 ± 0.5
H_1	Component Height	29.0 Max	32.0 Max	36.0 Max	40.0 Max	46.5 Max
D_0	Feed Hole Diameter	4.0 ± 0.2	4.0 ± 0.2	4.0 ± 0.2	4.0 ± 0.2	4.0 ± 0.2
t	Total Tape Thickness	0.7 ± 0.2	0.7 ± 0.2	0.7 ± 0.2	0.7 ± 0.2	0.7 ± 0.2
L	Length of Clipped Lead	11.0 Max	11.0 Max	11.0 Max	11.0 Max	12.0 Max
Δp	Component Alignment	3^{o} Max	3^{o} Max	3^{o} Max	3^{o} Max	3^{o} Max

NOTE: Dimensions are in mm.

Tape and Reel Ordering Information

Crimped leads are standard on ZA types supplied in tape and reel and are denoted by the model letter "T". Model letter "S" denotes straight leads and letter "U" denotes special under-crimped leads.

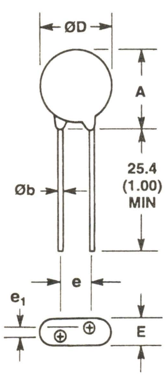
Example:

STANDARD MODEL	CRIMPED LEADS	STRAIGHT LEADS	UNDER-CRIMPED LEADS
V18ZA3	V18ZT3	V18ZS3	V18ZU3

SHIPPING QUANTITY

SIZE	RMS (MAX) VOLTAGE	QUANTITY PER REEL		
		"T" REEL	"S" REEL	"U" REEL
5mm	All	1000	1000	1000
7mm	All	1000	1000	1000
10mm	All	1000	1000	1000
14mm	< 300V	500	500	500
14mm	≥ 300V	500	500	500
20mm	< 300V	500	500	500
20mm	≥ 300V	500	500	500

Mechanical Dimensions



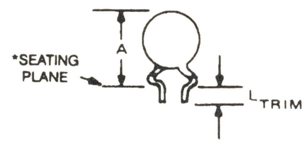
SYMBOL	VOLTAGE MODEL	VARISTOR MODEL SIZE									
		5mm		7mm		10mm		14mm		20mm	
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	All	- -	10 (0.394)	- -	12 (0.472)	- -	16 (0.630)	- -	20 (0.787)	- -	26.5 (1.043)
ØD	All	- -	7 (0.276)	- -	9 (0.354)	- -	12.5 (0.492)	- -	17 (0.669)	- -	23 (0.906)
e	All	4 (0.157)	6 (0.236)	4 (0.157)	6 (0.236)	6.5 (0.256)	8.5 (0.335)	6.5 (0.256)	8.5 (0.335)	6.5 (0.256)(Note 6)	8.5 (0.335)(Note 6)
e_1	V8ZA- V56ZA	1 (0.039)	3 (0.118)	1 (0.039)	3 (0.118)	1 (0.039)	3 (0.118)	1 (0.039)	3 (0.118)	1 (0.039)	3 (0.118)
	V68ZA- V100ZA	1.5 (0.059)	3.5 (0.138)	1.5 (0.059)	3.5 (0.138)	1.5 (0.059)	3.5 (0.138)	1.5 (0.059)	3.5 (0.138)	NA (NA)	NA (NA)
	V120ZA- V180ZA	1 (0.039)	3 (0.118)	1 (0.039)	3 (0.118)	1 (0.039)	3 (0.118)	1 (0.038)	1 (0.118)	NA (NA)	NA (NA)
	V205ZA- V750ZA	1.5 (0.059)	3.5 (0.138)	- -	- -	- -	- -	- -	- -	- -	- -
E	V8ZA- V56ZA	- -	5 (0.197)	- -	5 (0.197)	- -	5 (0.197)	- -	5 (0.197)	- -	5 (0.197)
	V68ZA- V100ZA	- -	5.6 (0.220)	- -	5.6 (0.220)	- -	5.6 (0.220)	- -	5.6 (0.220)	- -	5.6 (0.220)
	V120ZA- V180ZA	- -	5 (0.197)	- -	5 (0.197)	- -	5 (0.197)	- -	5 (0.197)	- -	5 (0.197)
	V205ZA- V750ZA	- -	5.6 (0.220)	- -	- -	- -	- -	- -	- -	- -	- -
Øb	All	0.585 (0.023)	0.685 (0.027)	0.585 (0.023)	0.685 (0.027)	0.76 (0.030)	0.86 (0.034)	0.76 (0.030)	0.86 (0.034)	0.76 (0.030)	0.86 (0.034)

NOTES: Dimensions in millimeters, inches in parentheses.

6. 10mm ALSO AVAILABLE; See Additional Lead Style Options.
7. V24ZA50 only supplied with lead spacing of 6.35mm ± 0.5mm (0.25 ± 0.0196) Dimension E = 5.85 min.

Additional Lead Style Options

Radial lead types can be supplied with combination preformed crimp and trimmed leads. This option is supplied to the dimensions shown.



*Seating plane interpretation per IEC-717

CRIMPED AND TRIMMED LEAD

SYMBOL	VARISTOR MODEL SIZE									
	5mm		7mm		10mm		14mm		20mm	
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	- -	13.0 (0.512)	- -	15 (0.591)	- -	19.5 (0.768)	- -	22.5 (0.886)	- -	29.0 (1.142)
L_{TRIM}	2.41 (0.095)	4.69 (0.185)	2.41 (0.095)	4.69 (0.185)	2.41 (0.095)	4.69 (0.185)	2.41 (0.095)	4.69 (0.185)	2.41 (0.095)	4.69 (0.185)

NOTE: Dimensions in millimeters, inches in parentheses.

- To order this crimped and trimmed lead style, standard radial type model numbers are changed by replacing the model letter "ZA" with "ZC". This option is supplied in bulk only.

Example:

STANDARD CATALOG MODEL	ORDER AS:
V18ZA3	V18ZC3

- For crimped leads without trimming and any variations to the above, contact Harris Semiconductor Power Marketing.

- For 10/±1mm lead spacing on 20mm diameter models only; append standard model numbers by adding "X10".

Example:

STANDARD CATALOG MODEL	ORDER AS:
V18ZA40	V18ZA40X10

Ordering Information

V XXX ZA XX

HARRIS VARISTOR

VARISTOR NOMINAL VOLTAGE (V_{NOM})
(One, Two or Three Digits)

SERIES DESIGNATOR/ LEAD STYLE DESIGNATOR
ZC = Crimped and Clipped
ZS = Straight
ZT = Crimped
ZU = Under Crimped

RELATIVE ENERGY INDICATOR
(One or Two Digits)

HARRIS SEMICONDUCTOR

BA/BB Series

January 1998

Industrial High Energy Metal-Oxide Varistors

Features

- **Recognized as "Transient Voltage Surge Suppressors", UL File #E75961 to Std. 1449**
- **High Energy Absorption Capability W_{TM}**
  BA Series 3200J
  BB Series 10,000J
- **Wide Operating Voltage Range $V_{M(AC)RMS}$**
  BA Series . . . . 130V to 880V
  BB Series . . . . 1100V to 2800V
- **Rigid Terminals for Secure Wire Contact**
- **Case Design Provides Complete Electrical Isolation of Disc SubAssembly**
- **Harris Largest Packaged Disc . . . . . . .60mm Diameter**
- **No Derating Up to 85°C Ambient**

Description

The BA and BB Series transient surge suppressors are heavy-duty industrial metal-oxide varistors (MOVs) designed to provide surge protection for motor controls and power supplies used in oil-drilling, mining, transportation equipment and other heavy industrial AC line applications.

These UL-recognized varistors have similar package construction but differ in size and ratings. The BA models are rated from 130 to 880$V_{M(AC)}$. The BB models from 1100 to 2800$V_{M(AC)}$.

Both the BA and BB Series feature improved creep and strike capability to minimize breakdown along the package surface, a package design that provides complete electrical isolation of the disc subassembly, and rigid terminals to insure secure wire contacts.

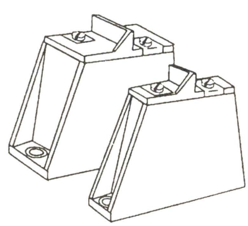
See BA/BB Series Device Ratings and Specifications table for part number and brand information.

4

VARISTOR PRODUCTS

Packaging

BB SERIES BA SERIES



File Number **2183.4**

Absolute Maximum Ratings

For ratings of individual members of a series, see Device Ratings and Specifications chart

	BA SERIES	BB SERIES	UNITS
Continuous:			
Steady State Applied Voltage:			
AC Voltage Range ($V_{M(AC)RMS}$)	130 to 880	1100 to 2800	V
DC Voltage Range ($V_{M(DC)}$)	175 to 1150	1400 to 3500	V
Transient:			
Peak Pulse Current (I_{TM})			
For 8/20μs Current Wave (See Figure 2)	50,000 to 70,000	70,000	A
Single Pulse Energy Range			
For 10/1000μs Current Wave (W_{TM})	450 to 3200	3800 to 10,000	J
Operating Ambient Temperature Range (T_A)	-55 to 85	-55 to 85	^oC
Storage Temperature Range (T_{STG})	-55 to 125	-55 to 125	^oC
Temperature Coefficient (αV) of Clamping Voltage (V_C) at Specified Test Current	<0.01	<0.01	%/^oC
Hi-Pot Encapsulation (Isolation Voltage Capability) (Dielectric must withstand indicated dc voltage for one minute per MIL-STD 202, Method 301)	5000	5000	V
Insulation Resistance	1000	1000	MΩ

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Device Ratings and Specifications

Series BA and BB Varistors are listed under UL file #E75961 as a UL recognized component.

PART NUMBER AND DEVICE BRANDING	MAXIMUM RATINGS (85^oC) CONTINUOUS V_{RMS}	CONTINUOUS V_{DC}	TRANSIENT ENERGY (2ms)	TRANSIENT PEAK CURRENT (8/20μs)	SPECIFICATIONS (25^oC) VARISTOR VOLTAGE AT 1mA DC TEST CURRENT			MAX CLAMPING VOLT V_C AT 200A CURRENT (8/20μs)	TYPICAL CAPACI-TANCE
	$V_{M(AC)}$	$V_{M(DC)}$	W_{TM}	I_{TM}	MIN	$V_{N(DC)}$	MAX	V_C	f = 1MHz
	(V)	(V)	(J)	(A)	(V)	(V)	(V)	(V)	(pF)
V131BA60	130	175	450	50000	184	200	228	340	20000
V151BA60	150	200	530	50000	212	240	268	400	16000
V251BA60	250	330	880	50000	354	390	429	620	10000
V271BA60	275	369	950	50000	389	430	473	680	9000
V321BA60	320	420	1100	50000	462	510	539	760	7500
V421BA60	420	560	1500	70000	610	680	748	1060	6000
V481BA60	480	640	1600	70000	670	750	825	1160	5500
V511BA60	510	675	1800	70000	735	820	910	1300	5000
V571BA60	575	730	2100	70000	805	910	1000	1420	4500
V661BA60	660	850	2300	70000	940	1050	1160	1640	4000
V751BA60	750	970	2600	70000	1080	1200	1320	1880	3500
V881BA60	880	1150	3200	70000	1290	1500	1650	2340	2700
V112BB60	1100	1400	3800	70000	1620	1800	2060	2940	2200
V142BB60	1400	1750	5000	70000	2020	2200	2550	3600	1800
V172BB60	1700	2150	6000	70000	2500	2700	3030	4300	1500
V202BB60	2000	2500	7500	70000	2970	3300	3630	5200	1200
V242BB60	2400	3000	8600	70000	3510	3900	4290	6200	1000
V282BB60	2800	3500	10000	70000	4230	4700	5170	7400	800

NOTE: Average power dissipation of transients not to exceed 2.5W. See Figures 3 and 4 for more information on power dissipation.

Power Dissipation Ratings

Continuous power dissipation capability is not an applicable design requirement for a suppressor, unless transients occur in rapid succession. Under this condition, the average power dissipation required is simply the energy (watt-seconds) per pulse times the number of pulses per second. The power so developed must be within the specifications shown on the Device Ratings and Characteristics table for the specific device. Furthermore, the operating values need to be derated at high temperatures as shown in Figure 1. Because varistors can only dissipate a relatively small amount of average power they are, therefore, not suitable for repetitive applications that involve substantial amounts of average power dissipation.

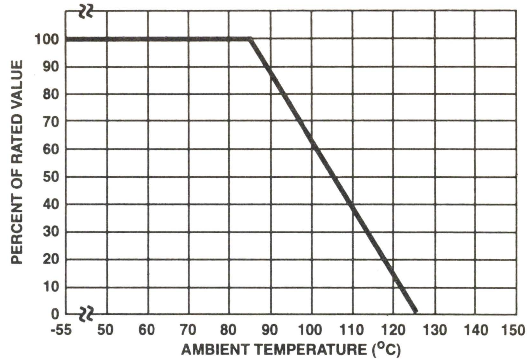
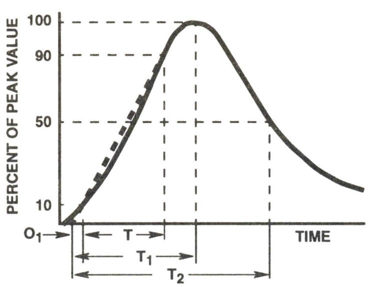


FIGURE 1. CURRENT, ENERGY AND POWER DERATING CURVE



O_1 = Virtual Origin of Wave
T = Time From 10% to 90% of Peak
T_1 = Virtual Front Time = 1.25 • t
T_2 = Virtual Time to Half Value (Impulse Duration)

Example: For an 8/20µs Current Waveform:
8µs = T_1 = Virtual Front Time
20µs = T_2 = Virtual Time to Half Value

FIGURE 2. PEAK PULSE CURRENT TEST WAVEFORM

Typical Performance Curves

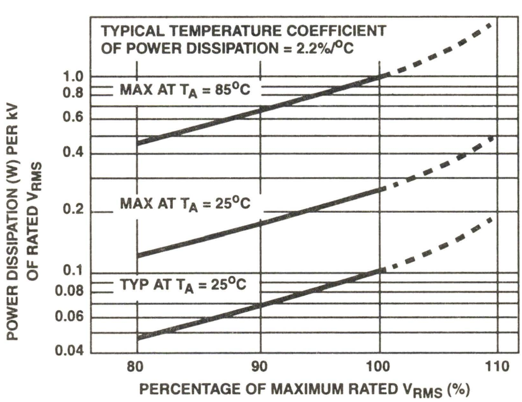


FIGURE 3. STANDBY POWER DISSIPATION vs APPLIED V_{RMS} AT VARIED TEMPERATURES

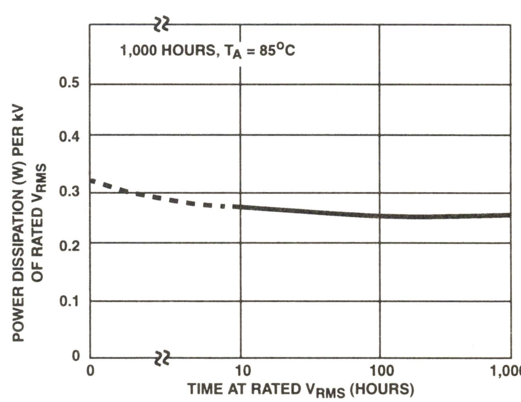


FIGURE 4. TYPICAL STABILITY OF STANDBY POWER DISSIPATION AT RATED V_{RMS} vs TIME

Transient V-I Characteristics Curves

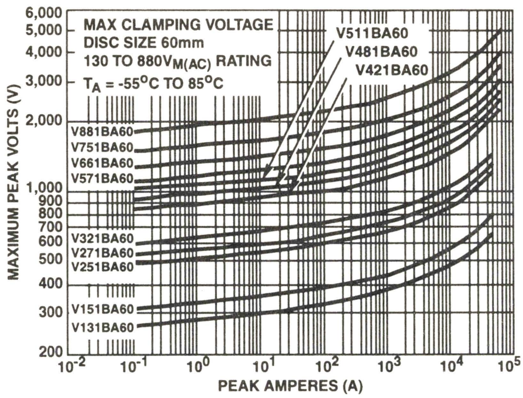


FIGURE 5. CLAMPING VOLTAGE FOR V131BA60 - V881BA60

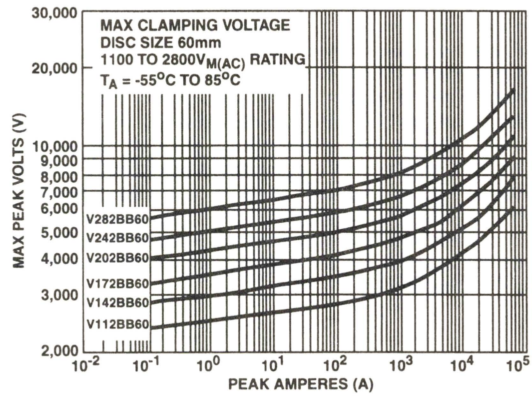


FIGURE 6. CLAMPING VOLTAGE FOR V112BB60 - V282BB60

Pulse Rating Curves

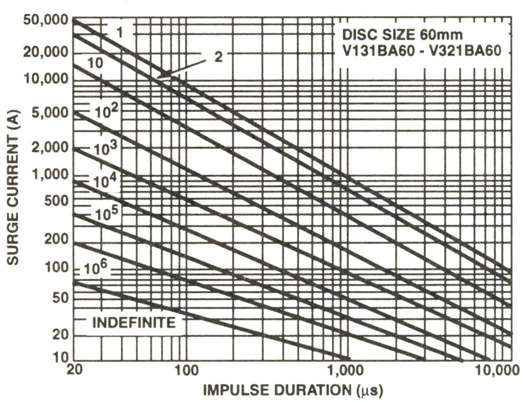


FIGURE 7. SURGE CURRENT RATING CURVES FOR V131BA60 - V321BA60

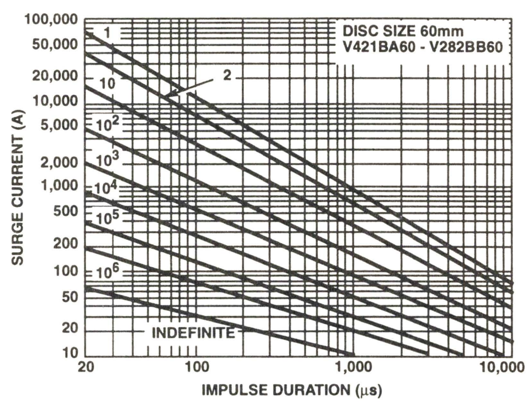
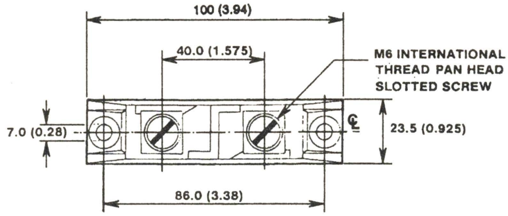


FIGURE 8. SURGE CURRENT RATING CURVES FOR V421BA60 - V282BB60

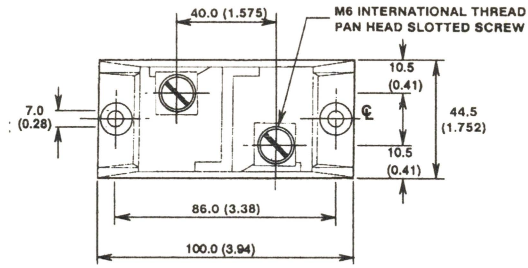
NOTE: If pulse ratings are exceeded, a shift of $V_{N(DC)}$ (at specified current) of more than ±10% could result. This type of shift, which normally results in a decrease of $V_{N(DC)}$, may result in the device not meeting the original published specifications, but it does not prevent the device from continuing to function, and to provide ample protection.

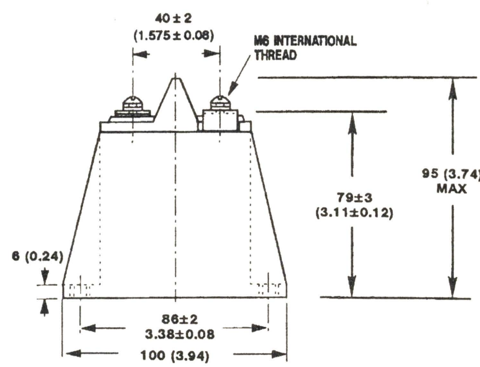
Mechanical Dimensions

BA SERIES



BB SERIES





NOTES:

1. Typical Weight:
   BA 250g
   BB 600g

Dimensions are in mm; inches in parentheses for reference only.

Ordering Information

V XX X XX 60

HARRIS VARISTOR

DISC SIZE (60mm)

$V_{M(AC)}$
First Significant Digits

SERIES DESIGNATOR

$V_{M(AC)}$
Decade Multiplier

HARRIS SEMICONDUCTOR

DA/DB Series

January 1998

Industrial High Energy Metal-Oxide Varistors

Features

- **Recognized as "Transient Voltage Surge Suppressors", UL File #E75961 to Std. 1449**
- **High Energy Absorption Capability W_{TM} Up To 1050J**
- **Wide Operating Voltage Range $V_{M(AC)RMS}$130V to 750V**
- **Screw Terminals (DA Series), Quick Connect Push-On Connectors (DB Series)**
- **Case Design Provides Complete Electrical Isolation of Disc Subassembly**
- **40mm Diameter Disc**
- **No Derating Up to 85°C Ambient**

Description

The DA and DB Series transient surge suppressors are heavy-duty industrial metal-oxide varistors designed to provide surge protection for motor controls and power supplies used in oil-drilling, mining, and transportation equipment.

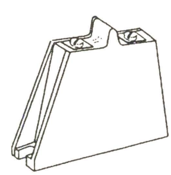
These UL-recognized varistors have identical ratings and specifications but differ in case construction to provide flexibility in equipment designs.

DA series devices feature rigid terminals to insure secure wire contacts. Both the DA and DB series feature improved creep and strike distance capability to minimize breakdown along the package surface design that provides complete electrical isolation of the disc subassembly.

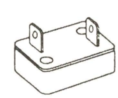
See DA/DB Series Device Ratings and Specifications table for part number and brand information.

Packaging

DA SERIES



DB SERIES



Absolute Maximum Ratings

For ratings of individual members of a series, see Device Ratings and Specifications chart

Continuous:		
Steady State Applied Voltage:		
AC Voltage Range ($V_{M(AC)RMS}$)	130 to 750	V
DC Voltage Range ($V_{M(DC)}$)	175 to 970	V
Transient:		
Peak Pulse Current (I_{TM}) For 8/20μs Current Wave (See Figure 2)	30,000 to 40,000	A
Single Pulse Energy Range For 10/1000μs Current Wave (W_{TM})	270 to 1050	J
Operating Ambient Temperature Range (T_A)	-55 to 85	°C
Storage Temperature Range (T_{STG})	-55 to 125	°C
Temperature Coefficient (αV) of Clamping Voltage (V_C) at Specified Test Current	<0.01	%/°C
Hi-Pot Encapsulation (Isolation Voltage Capability) (Dielectric must withstand indicated DC voltage for one minute per MIL-STD 202, Method 301)	5000	V
Insulation Resistance	1000	MΩ

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Device Ratings and Specifications

Series DA and DB Varistors are listed under UL file #E75961 as a UL recognized component.

PART NUMBER AND DEVICE BRANDING		MAXIMUM RATINGS (85°C)				SPECIFICATIONS (25°C)				
		CONTINUOUS		TRANSIENT						
		V_{RMS}	V_{DC}	ENERGY (2ms)	PEAK CURRENT (8/20μs)	VARISTOR VOLTAGE AT 1mA DC TEST CURRENT			MAX CLAMPING VOLT V_C AT 200A CURRENT (8/20μs)	TYPICAL CAPACI-TANCE
		$V_{M(AC)}$	$V_{M(DC)}$	W_{TM}	I_{TM}	MIN	$V_{N(DC)}$	MAX	V_C	f = 1MHz
DA	DB	(V)	(V)	(J)	(A)	(V)	(V)	(V)	(V)	(pF)
V131DA40	V131DB40	130	175	270	30000	184	200	228	345	10000
V151DA40	V151DB40	150	200	300	30000	212	240	268	405	8000
V251DA40	V251DB40	250	330	370	30000	354	390	429	650	5000
V271DA40	V271DB40	275	369	400	30000	389	430	473	730	4500
V321DA40	V321DB40	320	420	460	30000	462	510	539	830	3800
V421DA40	V421DB40	420	560	600	40000	610	680	748	1130	3000
V481DA40	V481DB40	480	640	650	40000	670	750	825	1240	2700
V511DA40	V511DB40	510	675	700	40000	735	820	910	1350	2500
V571DA40	V571DB40	575	730	770	40000	805	910	1000	1480	2200
V661DA40	V661DB40	660	850	900	40000	940	1050	1160	1720	2000
V751DA40	V751DB40	750	970	1050	40000	1080	1200	1320	2000	1800

NOTE: Average power dissipation of transients not to exceed 2.0W.

Power Dissipation Ratings

Continuous power dissipation capability is not an applicable design requirement for a suppressor, unless transients occur in rapid succession. Under this condition, the average power dissipation required is simply the energy (watt-seconds) per pulse times the number of pulses per second. The power so developed must be within the specifications shown on the Device Ratings and Specifications table for the specific device. Furthermore, the operating values need to be derated at high temperatures as shown in Figure 1. Because varistors can only dissipate a relatively small amount of average power they are, therefore, not suitable for repetitive applications that involve substantial amounts of average power dissipation.

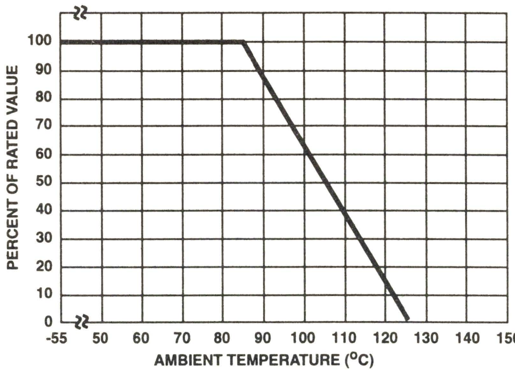
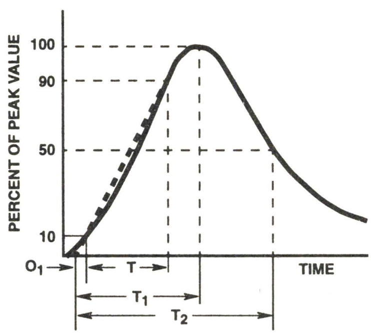


FIGURE 1. CURRENT, ENERGY AND POWER DERATING CURVE



O_1 = Virtual Origin of Wave
T = Time From 10% to 90% of Peak
T_1 = Virtual Front time = 1.25 • t
T_2 = Virtual Time to Half Value (Impulse Duration)
Example: For an 8/20μs Current Waveform:
8μs = T_1 = Virtual Front Time
20μs = T_2 = Virtual Time to Half Value

FIGURE 2. PEAK PULSE CURRENT TEST WAVEFORM

Transient V-I Characteristics Curve

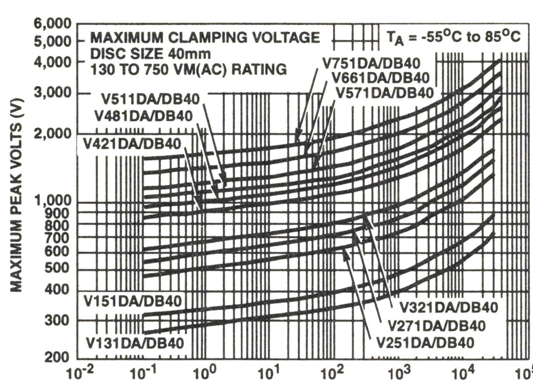


FIGURE 3. CLAMPING VOLTAGE FOR V131DA40, V131DB40 - V751DA40, V751DB40

Pulse Rating Curves

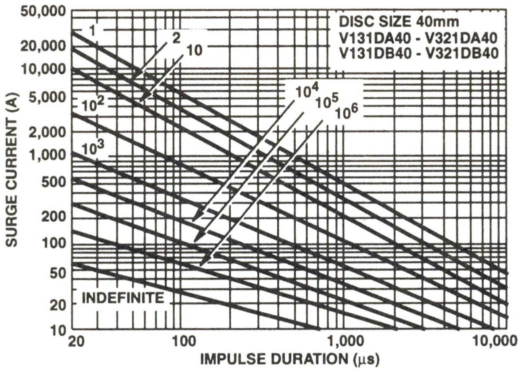


FIGURE 4. SURGE CURRENT RATING CURVES FOR V131DA40, V131DB40 - V321DA40, V321DB40

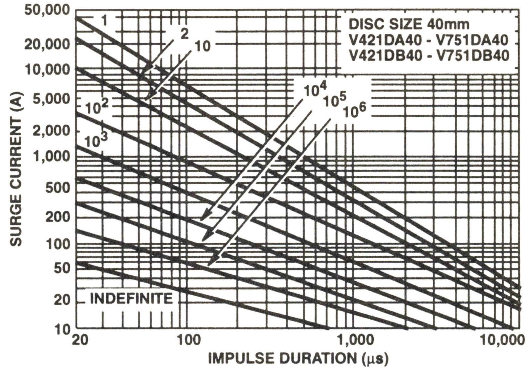
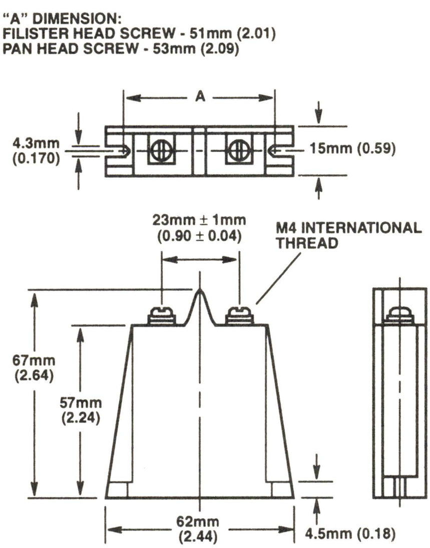


FIGURE 5. SURGE CURRENT RATING CURVES FOR V421DA40, V421DB40 - V751DA40

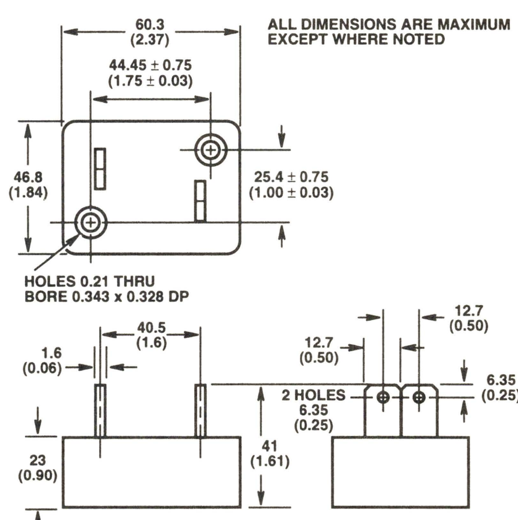
NOTE: If pulse ratings are exceeded, a shift of $V_{N(DC)}$ (at specified current) of more than ±10% could result. This type of shift, which normally results in a decrease of $V_{N(DC)}$, may result in the device not meeting the original published specifications, but it does not prevent the device from continuing to function, and to provide ample protection.

Mechanical Dimensions

DA SERIES



DB SERIES



Dimensions in millimeters and (inches).

HARRIS SEMICONDUCTOR

HA Series

January 1998

Industrial High Energy Metal-Oxide Varistors

Features

- **Recognized as "Transient Voltage Surge Suppressors", UL File #E75961 to Std. 1449**
- **Recognised as "Transient Voltage Surge Suppressors", CSA File #LR91788 to Standard C22.2 No. 1-M1981**
- **Wide Operating Voltage Range $V_{M(AC)RMS}$ . . . . 130V to 750V**
- **Two Disc Sizes Available. . . . . 32mm and 40mm**
- **High Energy Absorption Capability . . . . W_{TM} = 200J to 1050J**
- **High Peak Pulse Current Capability . . . . I_{TM} = 25,000A to 40,000A**
- **Rigid Terminals for Secure Mounting**
- **Available in Trimmed Version for Through Hole Board Mounting - Designation "HC"**
- **No Derating Up to 85°C Ambient**

Description

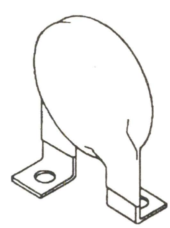
HA Series transient surge suppressors are industrial high energy metal-oxide varistors (MOVs). They are designed to provide secondary surge protection in the outdoor and service entrance environment (distribution panels) of buildings, and also in industrial applications for motor controls and power supplies used in the oil-drilling, mining, and transportation fields.

The design of the HA Series of metal oxide varistors provide rigid terminals for screw mounting. Also available in a clipped version for through hole board placement - designation "HC".

See Ratings and Specifications table for part number and brand information.

Packaging

HA SERIES



File Number **2973.4**

HA Series

Absolute Maximum Ratings For ratings of individual members of a series, see Device Ratings and Specifications chart

	HA SERIES	UNITS
Continuous:		
Steady State Applied Voltage:		
AC Voltage Range ($V_{M(AC)RMS}$)	130 to 750	V
DC Voltage Range ($V_{M(DC)}$)	175 to 970	V
Transient:		
Peak Pulse Current (I_{TM})		
For 8/20μs Current Wave (See Figure 2)	25,000 to 40,000	A
Single Pulse Energy Range		
For 10/1000μs Current Wave (W_{TM})	200 to 1050	J
Operating Ambient Temperature Range (T_A)	-55 to 85	^oC
Storage Temperature Range (T_{STG})	-55 to 125	^oC
Temperature Coefficient (αV) of Clamping Voltage (V_C) at Specified Test Current	<0.01	%/^oC
Hi-Pot Encapsulation (Isolation Voltage Capability) (Dielectric must withstand indicated DC voltage for one minute per MIL-STD 202, Method 301)	2500	V
Insulation Resistance	1000	MΩ

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Device Ratings and Specifications

HA Series varistors are listed under CSA File #LR91788 as a recognized component.

HA Series varistors are listed under U.L. File #E75961 as a recognized component.

PART NUMBER AND DEVICE BRANDING	MAXIMUM RATINGS (85^oC)				SPECIFICATIONS (25^oC)				
	CONTINUOUS		TRANSIENT						
	V_{RMS}	V_{DC}	ENERGY (2ms)	PEAK CURRENT (8/20μs)	VARISTOR VOLTAGE AT 1 mA DC TEST CURRENT			MAXIMUM CLAMPING VOLTAGE (V_C) AT 200A (8/20μs)	TYPICAL CAPACITANCE AT f = 1MHz
	$V_{M(AC)}$	$V_{M(DC)}$	W_{TM}	I_{TM}	MIN	$V_{N(DC)}$	MAX	V_C	C
	(V)	(V)	ENERGY	(A)	(V)	(V)	(V)	(V)	(pF)
V131HA32	130	175	200	25000	184	200	228	350	4700
V131HA40	130	175	270	30000	184	200	228	345	10000
V151HA32	150	200	220	25000	212	240	268	410	4000
V151HA40	150	200	300	30000	212	240	268	405	8000
V251HA32	250	330	330	25000	354	390	429	650	2500
V251HA40	250	330	370	40000	354	390	429	630	5000
V271HA32	275	369	360	25000	389	430	473	710	2200
V271HA40	275	369	400	40000	389	430	473	690	4500
V321HA32	320	420	390	25000	462	510	539	845	1900
V321HA40	320	420	460	40000	462	510	539	825	3800
V421HA32	420	560	400	25000	610	680	748	1120	1500
V421HA40	420	560	600	40000	610	680	748	1100	3000
V481HA32	480	640	450	25000	670	750	825	1290	1300
V481HA40	480	640	650	40000	670	750	825	1230	2700
V511HA32	510	675	500	25000	735	820	910	1355	1200
V511HA40	510	675	700	40000	735	820	910	1295	2500
V571HA32	575	730	550	25000	805	910	1000	1570	1100
V571HA40	575	730	770	40000	805	910	1000	1480	2200
V661HA32	660	850	600	25000	940	1050	1160	1820	1000
V661HA40	660	850	900	40000	940	1050	1160	1720	2000
V751HA32	750	970	700	25000	1080	1200	1320	2050	800
V751HA40	750	970	1050	40000	1080	1200	1320	2000	1800

Power Dissipation Ratings

Continuous power dissipation capability is not an applicable requirement for a suppressor, unless transients occur in rapid succession. Under this condition, the average power dissipation required is simply the energy (watt-seconds) per pulse times the number of pulses per second. The power so developed must be within the specifications shown on the Device Ratings and Specifications table for the specific device. Furthermore, the operating values need to be derated at high temperatures as shown in Figure 1. Because varistors can only dissipate a relatively small amount of average power they are, therefore, not suitable for repetitive applications that involve substantial amounts for average power dissipation.

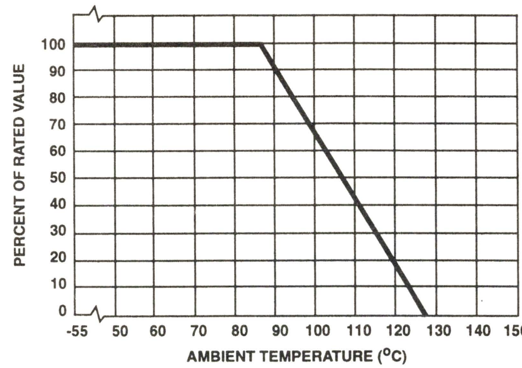
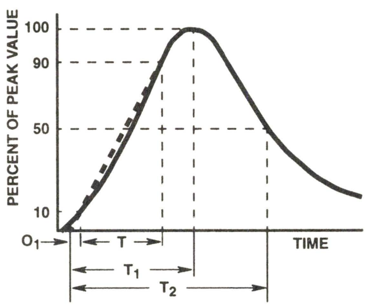


FIGURE 1. CURRENT, ENERGY AND POWER DERATING CURVE



O_1 = Virtual Origin of Wave
T = Time From 10% to 90% of Peak
T_1 = Virtual Front Time = 1.25 • t
T_2 = Virtual Time to Half Value (Impulse Duration)

Example: For an 8/20μs Current Waveform:
8μs = T_1 = Virtual Front Time
20μs = T_2 = Virtual Time to Half Value

FIGURE 2. PEAK PULSE CURRENT WAVEFORM

Transient V-I Characteristics Curves

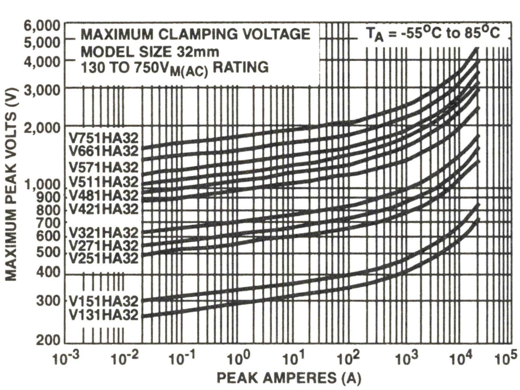


FIGURE 3. CLAMPING VOLTAGE FOR V131HA32 - V751HA32

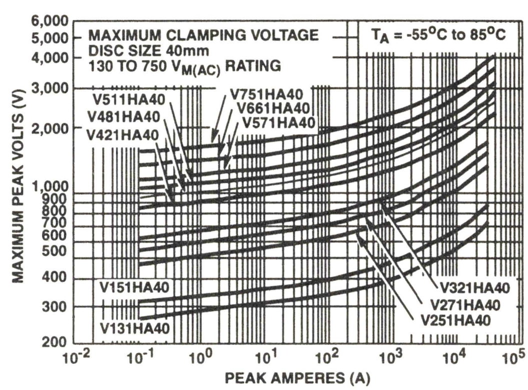


FIGURE 4. CLAMPING VOLTAGE FOR V131HA40 - V751HA40

Pulse Rating Curves

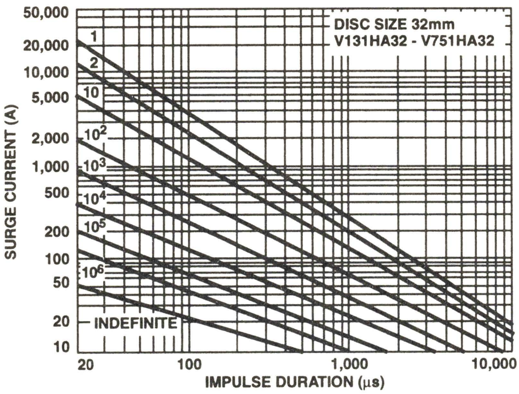


FIGURE 5. SURGE CURRENT RATING CURVES FOR V131HA32 - V751HA32

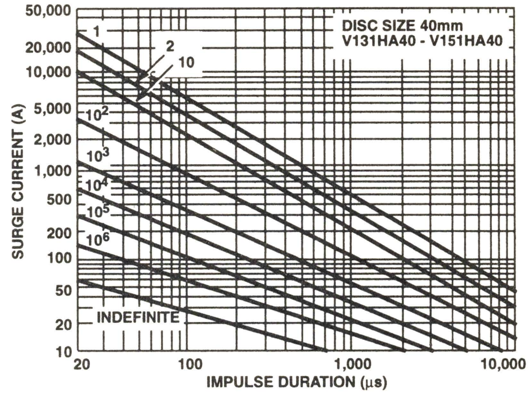


FIGURE 6. SURGE CURRENT RATING CURVES FOR V131HA40 - V151HA40

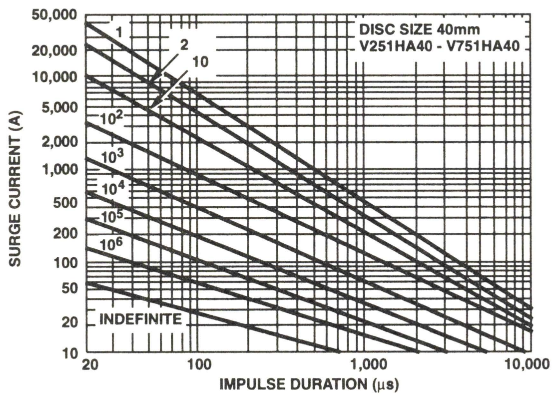
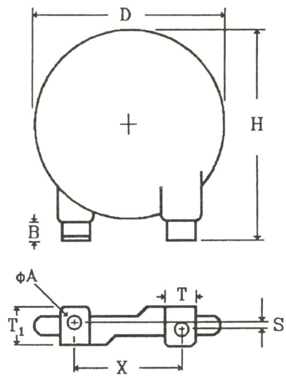


FIGURE 7. SURGE CURRENT RATING CURVES FOR V251HA40 - V751HA40

Mechanical Dimensions



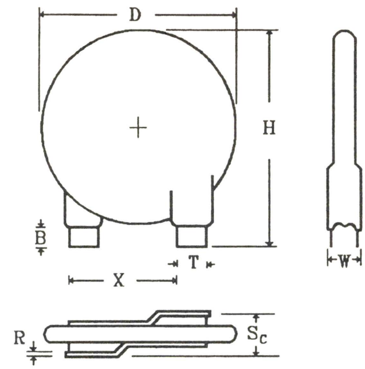


TABLE 1. HA SERIES OUTLINE SPECIFICATIONS (Dimensions in Millimeters)

	D	H	B	X	ØA	T	T1	S
	MAX	MAX	MIN	NOM	MAX	NOM	NOM	OFFSET
HA32	35.5	52.00	3.0	25	4.20	9.30	10.4	Depends on Device Voltage (See Table 2)
HA40	42.5	57.00	3.0	25	4.20	9.30	10.4	

TABLE 3. HC SERIES OUTLINE SPECIFICATIONS (Dimensions in Millimeters)

	D	H	B	X	T	R	S_C
	MAX	MAX	MIN	NOM	NOM	MAX	OFFSET
HC32	35.5	52.00	5.0	25	9.30	1.0	Depends on Device Voltage (See Table 4)
HC40	42.5	57.00	5.0	25	9.30	1.0	

TABLE 2. HA SERIES MAXIMUM THICKNESS AND TERMINAL OFFSETS (Dimensions in Millimeters)

VOLTAGE	THICKNESS "W"		DIMENSION "S" (±1mm)	
	HA32	HA40	HA32	HA40
V131 - V321	9.00	9.00	3.90	3.90
V421 - V511	11.00	11.00	2.60	2.60
V571 - V751	13.00	13.00	1.00	1.00

TABLE 4. HC SERIES MAXIMUM THICKNESS AND TERMINAL OFFSETS (Dimensions in Millimeters)

VOLTAGE	THICKNESS "W"		DIMENSION "S_C" (±1mm)	
	HC32	HC40	HC32	HC40
V131 - V321	9.00	9.00	6.00	6.00
V421 - V511	11.00	11.00	7.30	8.10
V571 - V751	13.00	13.00	8.90	10.00

Ordering Information

V XX X HA XX

V — **HARRIS VARISTOR**

XX — $V_{M(AC)}$ First Two Significant Digits

X — $V_{M(AC)}$ Decade Multiplier

HA — **SERIES DESIGNATOR** HA or HC

XX — **DISC SIZE (mm)**

HARRIS SEMICONDUCTOR

CA Series

Industrial High Energy Metal-Oxide Disc Varistors

January 1998

Features

- **Provided In Disc Form For Unique Packaging By Customer**
- **Solderable Electrode Finish Options**
- **Pressure Contacts and/or Disc Stacking May be Utilized**
- **Standard Disc Sizes 32mm, 40mm, and 60mm Diameter**
- **Available Edge Passivation Insulation**
- **Wide Operating Voltage Range $V_{M(AC)RMS}$ 130V to 2800V**
- **High Peak Pulse Current Range I_{TM} 20,000A to 70,000A**
- **Very High Energy Capability W_{TM} . . . . 200J to 10,000J**
- **No Derating Up to 85°C Ambient**

Description

The CA Series of transient surge suppressors are industrial high-energy disc varistors (MOVs) intended for special applications requiring unique electrical contact or packaging methods provided by the customer. The electrode finish of these devices is solderable and can also be used with pressure contacts. Discs of the same diameter may be stacked.

This series of industrial disc varistors are available in three diameter sizes of 32, 40, and 60mm, with disc thicknesses ranging from 1.8mm minimum to 32mm maximum. They offer a wide voltage range of from 130 to 2800 $V_{M(AC)RMS}$.

For information on soldering considerations, refer to AN8820 "Recommendations for Soldering Terminal Leads to MOV Varistor Discs".

Packaging

CA SERIES

4

VARISTOR PRODUCTS

File Number **2187.4**

Absolute Maximum Ratings

For ratings of individual members of a series, see Device Ratings and Specifications chart

	CA SERIES	UNITS
Continuous:		
Steady State Applied Voltage:		
AC Voltage Range ($V_{M(AC)RMS}$)	130 to 2800	V
DC Voltage Range ($V_{M(DC)}$)	175 to 3500	V
Transient:		
Peak Pulse Current (I_{TM})		
For 8/20µs Current Wave (See Figure 2)	20,000 to 70,000	A
Single Pulse Energy Range		
For 10/1000µs Current Wave (W_{TM})	200 to 10,000	J
Operating Ambient Temperature Range (T_A)	-55 to 85	^oC
Storage Temperature Range (T_{STG})	-55 to 125	^oC
Temperature Coefficient (αV) of Clamping Voltage (V_C) at Specified Test Current	<0.01	%/^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Device Ratings and Specifications

MODEL NUMBER	SIZE	MAXIMUM RATINGS (85°C)				SPECIFICATIONS (25°C)				
		CONTINUOUS		TRANSIENT						
		V_{RMS}	V_{DC}	ENERGY (2ms)	PEAK CURRENT (8/20µs)	VARISTOR VOLTAGE AT 1mA DC TEST CURRENT			MAX CLAMPING VOLT V_C AT 200A CURRENT (8/20µs)	TYPICAL CAPACI-TANCE
	SIZE	$V_{M(AC)}$	$V_{M(DC)}$	W_{TM}	I_{TM}	MIN	$V_{N(DC)}$	MAX	V_C	f = 1MHz
	(mm)	(V)	(V)	(J)	(A)	(V)	(V)	(V)	(V)	(pF)
V131CA32	32	130	175	200	20000	184	200	228	350	4700
V131CA40	40			270	30000				345	10000
V151CA32	32	150	200	220	20000	212	240	268	410	4000
V151CA40	40			300	30000				405	8000
V251CA32	32	250	330	330	20000	354	390	429	680	2500
V251CA40	40			370	30000				650	5000
V251CA60	60			880	50000				620	10000
V271CA32	32	275	369	360	20000	389	430	473	750	2200
V271CA40	40			400	30000				730	4500
V271CA60	60			950	50000				680	9000
V321CA32	32	320	420	390	20000	462	510	539	850	1900
V321CA40	40			460	30000				830	3800
V321CA60	60			1100	50000				760	7500
V421CA32	32	420	560	400	25000	610	680	748	1200	1500
V421CA40	40			600	40000				1130	3000
V421CA60	60			1500	70000				1060	6000
V481CA32	32	480	640	450	25000	670	750	825	1300	1300
V481CA40	40			650	40000				1240	2700
V481CA60	60			1600	70000				1160	5500
V511CA32	32	510	675	500	25000	735	820	910	1440	1200
V511CA40	40			700	40000				1350	2500
V511CA60	60			1800	70000				1300	5000
V571CA32	32	575	730	550	25000	805	910	1000	1600	1100
V571CA40	40			770	40000				1480	2200
V571CA60	60			2100	70000				1420	4500

Device Ratings and Specifications (Continued)

MODEL NUMBER	SIZE	MAXIMUM RATINGS (85°C)				SPECIFICATIONS (25°C)				
		CONTINUOUS		TRANSIENT		VARISTOR VOLTAGE AT 1mA DC TEST CURRENT			MAX CLAMPING VOLT V_C AT 200A CURRENT (8/20µs)	TYPICAL CAPACI-TANCE
		V_{RMS}	V_{DC}	ENERGY (2ms)	PEAK CURRENT (8/20µs)					
	SIZE	$V_{M(AC)}$	$V_{M(DC)}$	W_{TM}	I_{TM}	MIN	$V_{N(DC)}$	MAX	V_C	f = 1MHz
	(mm)	(V)	(V)	(J)	(A)	(V)	(V)	(V)	(V)	(pF)
V661CA32	32	660	850	600	25000	940	1050	1160	1820	1000
V661CA40	40			900	40000				1720	2000
V661CA60	60			2300	70000				1640	4000
V751CA32	32	750	970	700	25000	1080	1200	1320	2050	800
V751CA40	40			1050	40000				2000	1800
V751CA60	60			2600	70000				1880	3500
V881CA60	60	880	1150	3200	70000	1290	1500	1650	2340	2700
V112CA60	60	1100	1400	3200	70000	1620	1800	2060	2940	2200
V142CA60	60	1400	1750	5000	70000	2020	2200	2550	3600	1800
V172CA60	60	1700	2150	6000	70000	2500	2700	3030	4300	1500
V202CA60	60	2000	2500	7500	70000	2970	3300	3630	5200	1200
V242CA60	60	2400	3000	8600	70000	3510	3900	4290	6200	1000
V282CA60	60	2800	3500	10000	70000	4230	4700	5170	7400	800

NOTE: Average power dissipation of transients not exceed 1.5W, 2.0W and 2.5W for model 32mm, 40mm and 60mm, respectively.

Power Dissipation Ratings

Should transients occur in rapid succession, the average power dissipation result is the energy (watt-seconds) per pulse times the number of pulses per second. The power so developed must be within the specifications shown on the Device Ratings and Specifications table for the specific device. Furthermore, the operating values need to be derated at high temperatures as shown in Figure 1. Because varistors can only dissipate a relatively small amount of average power they are, therefore, not suitable for repetitive applications that involve substantial amounts of average power dissipation.

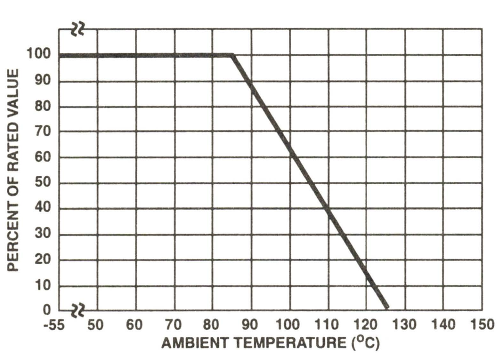
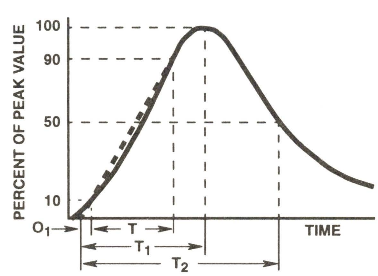


FIGURE 1. CURRENT, ENERGY AND POWER DERATING CURVE



O_1 = Virtual Origin of Wave

T = Time From 10% to 90% of Peak

T_1 = Virtual Front Time = 1.25 • t

T_2 = Virtual Time to Half Value (Impulse Duration)

Example: For an 8/20µs Current Waveform:

8µs = T_1 = Virtual Front Time

20µs = T_2 = Virtual Time to Half Value

FIGURE 2. PEAK PULSE CURRENT TEST WAVEFORM

Transient V-I Characteristics Curves

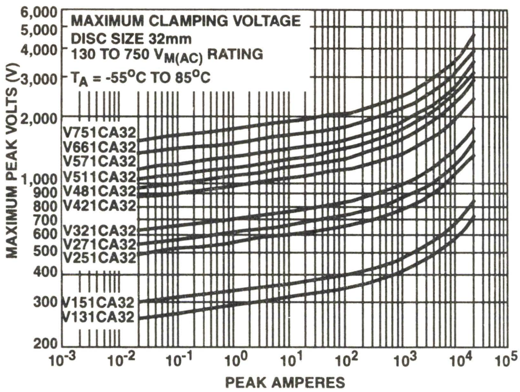


FIGURE 3. CLAMPING VOLTAGE FOR V131CA32 - C751CA32

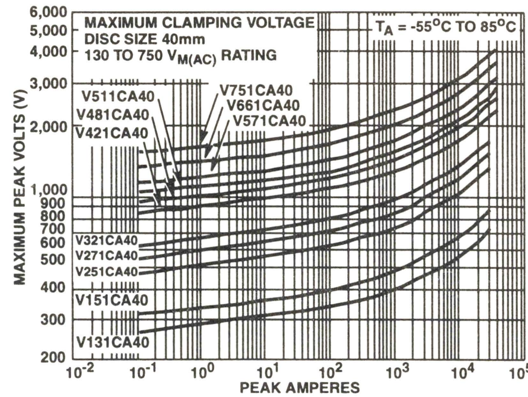


FIGURE 4. CLAMPING VOLTAGE FOR V131CA40 - V751CA40

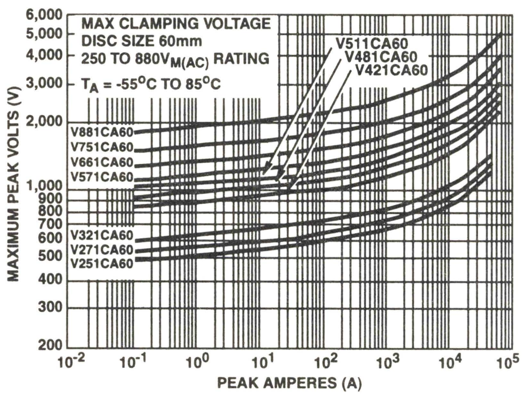


FIGURE 5. CLAMPING VOLTAGE FOR V251CA60 - V881CA60

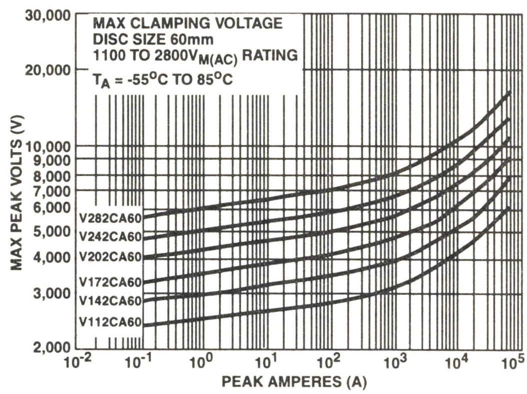


FIGURE 6. CLAMPING VOLTAGE FOR V112CA60 - V282CA60

Pulse Rating Curves

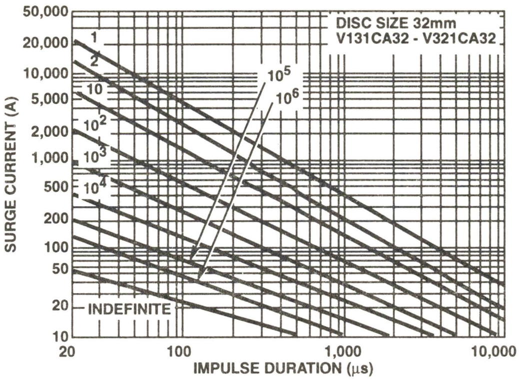


FIGURE 7. SURGE CURRENT RATING CURVES FOR V131CA32 - V321CA32

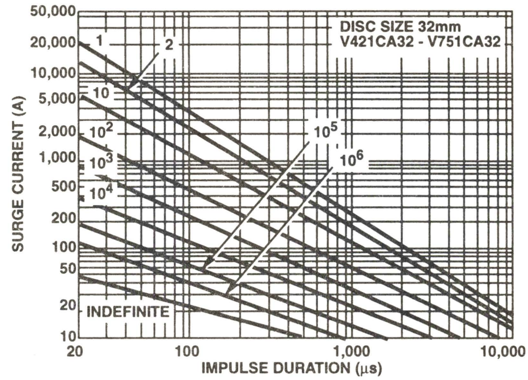


FIGURE 8. SURGE CURRENT RATING CURVES FOR V421CA32 - V751CA32

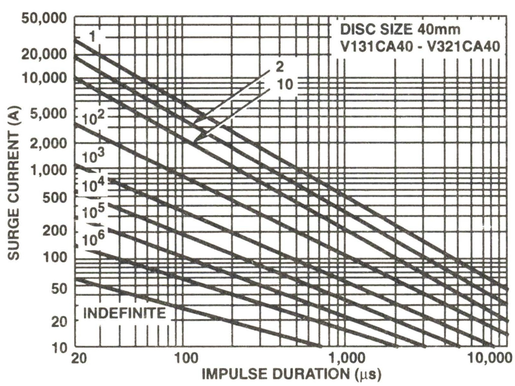


FIGURE 9. SURGE CURRENT RATING CURVES FOR V131CA40 - V321CA40

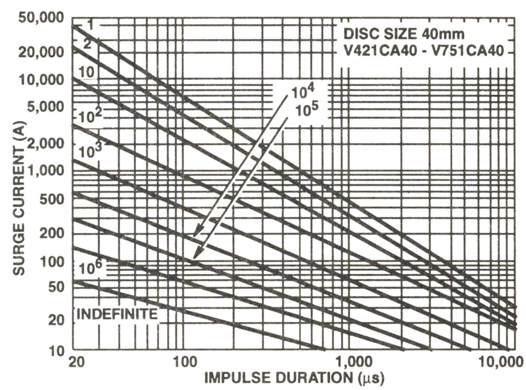


FIGURE 10. SURGE CURRENT RATING CURVES FOR V421CA40 - V751CA40

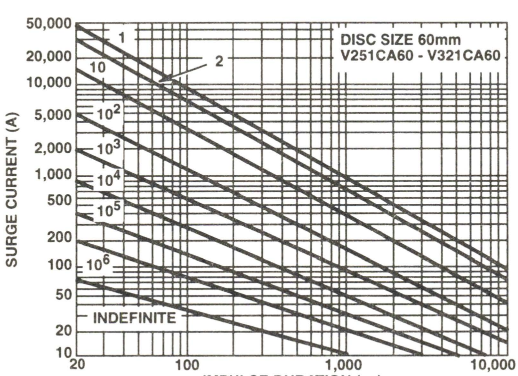


FIGURE 11. SURGE CURRENT RATING CURVES FOR V251CA60 - V321CA60

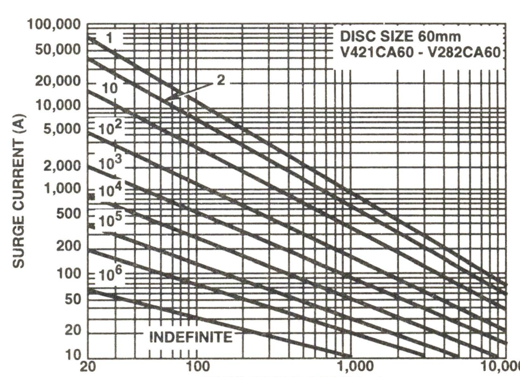
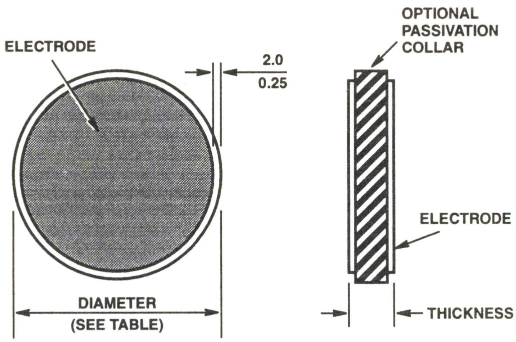


FIGURE 12. SURGE CURRENT RATING CURVES FOR V421CA60 - V282CA60

NOTE: If pulse ratings are exceeded, a shift of $V_{N(DC)}$ (at specified current) of more than ±10% could result. This type of shift, which normally results in a decrease of $V_{N(DC)}$, may result in the device not meeting the original published specifications, but does not prevent the device from continuing to function, and to provide ample protection.

Series Dimensions



MODEL SIZE	DISC DIAMETER			
	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
32	31.0	33.0	1.220	1.299
40	38.0	40.0	1.496	1.575
60	58.0	62.0	2.283	2.441

MODEL V_{RMS} $V_{M(AC)}$	THICKNESS (32mm DISC MODELS)				THICKNESS (40mm AND 60mm DISC MODELS)			
	MILLIMETERS		INCHES		MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
130†	1.8	2.4	0.071	0.094	2.5	3.4	0.098	0.134
150†	2.1	2.8	0.083	0.110	2.8	3.8	0.110	0.150
250	1.6	2.2	0.063	0.087	2.0	2.7	0.079	0.106
275	1.8	2.5	0.071	0.098	2.2	3.0	0.087	0.118
320	2.1	2.9	0.083	0.114	2.6	3.5	0.102	0.138
420	2.9	3.9	0.114	0.154	3.5	4.7	0.138	0.185
480	3.1	4.3	0.122	0.169	3.8	5.2	0.150	0.205
510	3.5	4.7	0.138	0.185	4.2	5.7	0.165	0.224
575	3.8	5.1	0.150	0.201	4.6	6.3	0.181	0.248
660	4.4	6.0	0.173	0.236	5.3	7.2	0.209	0.283
750	5.1	6.9	0.240	0.327	6.1	8.3	0.240	0.327
880††	-	-	-	-	7.3	10.3	0.287	0.406
1100††	-	-	-	-	9.2	13.0	0.362	0.512
1400††	-	-	-	-	11.5	16.0	0.453	0.630
1700††	-	-	-	-	14.0	19.0	0.551	0.748
2000††	-	-	-	-	17.0	22.5	0.669	0.886
2400††	-	-	-	-	20.0	27.0	0.787	1.063
2800††	-	-	-	-	24.0	32.0	0.945	1.260

† Available in 32mm and 40mm only.

†† Available in 60mm size only.

MODEL NUMBER	SIZE (mm)	TYPICAL DISC WEIGHT (GRAMS)
V131CA32	32	9
V131CA40	40	21
V151CA32	32	11
V151CA40	40	23
V251CA32	32	8
V251CA40	40	17
V251CA60	60	39
V271CA32	32	10
V271CA40	40	18
V271CA60	60	42
V321CA32	32	11
V321CA40	40	22
V321CA60	60	50
V421CA32	32	15
V421CA40	40	28
V421CA60	60	66
V481CA32	32	16
V481CA40	40	31
V481CA60	60	71
V511CA32	32	18
V511CA40	40	35
V511CA60	60	80
V571CA32	32	20
V571CA40	40	38
V571CA60	60	88
V661CA32	32	23
V661CA40	40	44
V661CA60	60	101
V751CA32	32	26
V751CA40	40	51
V751CA60	60	116
V881CA60	60	141
V112CA60	60	178
V142CA60	60	220
V172CA60	60	265
V202CA60	60	317
V242CA60	60	377
V282CA60	60	450

Passivation Layer

The standard CA Series is supplied with passivation layer around the outside perimeter of the disc forming an electrical insulator as detailed in the dimensional drawing. The CA Series is also available without a passivation layer for applications where the customer provides a suitable encapsulation or potting material as recommended below. (See Ordering Information.)

Encapsulated Recommendations

After lead attachment, the disc/lead assembly may be coated or encapsulated in a package to provide electrical insulation and isolation from environmental contamination as required by the application. Coating/Filler materials for containers may include silicones, polyurethanes, and some epoxy resins. Two examples of acceptable polyurethanes are Dexter Hysol (US7013, parts A and B) and Rhenatech (resin 4714, hardener 4900), or their equivalents. Materials containing halogens, sulphides, or alkalines are not recommended.

Electrode Metallization

The CA Series is available with either a sintered silver or an arc-sprayed copper-over-aluminum metallization for the electrode finish. In general, when discs are stacked to attain a specific operating voltage or energy capability, the copper finish is typically chosen. Likewise, the copper finish is used with high temperature lead attach soldering operations (wave solder). The silver metallization is typically used for solder reflow lead attach operations (I-R, Vapour-Phase).

The recommended temperature profile of a belt-fed convection oven is shown in Figure 13.

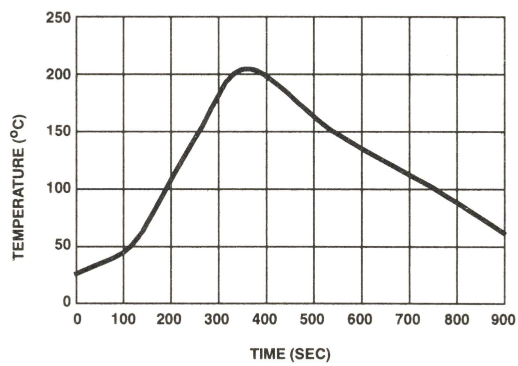


FIGURE 13. TYPICAL BELT OVEN TEMPERATURE PROFILE

Stacking and Contact Pressure Recommendations

When applications require the stacking of Harris CA discs or when electrical connection is made by pressure contacts, the minimum pressure applied to the disc electrode surface should be 2.2kGs (5 pounds). The maximum recommended pressure applied to the disc electrode is dependent upon diameter size and is given in the following table.

MODEL SIZE (mm)	MAXIMUM PRESSURE
32	$16N/CM^2$ ($23LBs/IN^2$)
40	$8N/CM^2$ ($11.5LBs/IN^2$)
60	$4N/CM^2$ ($5.7LBs/IN^2$)

Ordering Information

The CA Series offers optional electrode finish materials and a glass passivation edge option which must be designated. When ordering, the code letters suffix as shown in the following table must be selected and appended to the standard Model number.

NOTES:

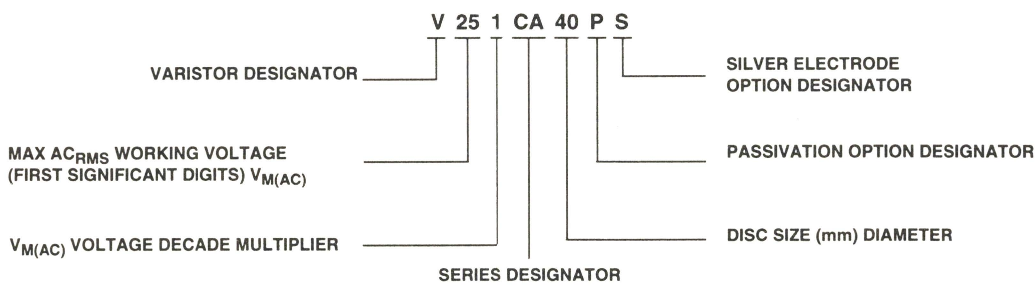
1. The 60mm disc types V112CA60 to V282CA60, inclusive, are only supplied with glass passivation and arc-sprayed copper finish electrodes. (That is, with the "PC" option suffix code.)
2. The 32mm size discs are only available with silver metallization.

Note also that the CA Series receives no branding on the disc itself.

ELECTRODE MATERIAL	NON-PASSIVATED DISC	PASSIVATED DISC
Arc-Sprayed Copper	NC	PC
Sintered Silver	NS	PS

Packaging and Shipping

The CA Series is supplied in bulk for shipment. Discs are packaged in compartmentized cartons to protect from scratching or edge-chipping during shipment.



NA Series

Industrial High Energy Metal-Oxide Square Disc Varistors

January 1998

Features

- Provided in Disc Form for Unique Packaging by Customer
- Solderable Electrode Finish
- Pressure Contacts and/or Disc Stacking may be Utilized
- Wide Operating Voltage Range
  $V_{M(AC)RMS}$ . . . . 130V to 750V
- Peak Pulse Current Capability I_{TM} 40,000A
- High Energy Capability W_{TM}. . . . . 270J to 1050J
- No Derating Up to 85°C Ambient

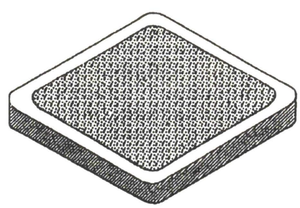
Description

The NA Series of transient surge suppressors are varistors (MOVs) in square disc form, intended for special industrial high-energy applications requiring unique electrical contact or packaging methods provided by the customer. The electrode finish of these devices is solderable and can also be used with pressure contacts. Discs may also be stacked.

The NA Series varistor is a square 34mm device, with thicknesses ranging from 1.8mm minimum for the 130V device to 8.3mm maximum for the 750V device. For information on mounting considerations refer to Application Note AN8820.

Packaging

NA SERIES



Absolute Maximum Ratings For ratings of individual members of a series, see Device Ratings and Specifications chart

	NA SERIES	UNITS
Continuous:		
Steady State Applied Voltage:		
AC Voltage Range ($V_{M(AC)RMS}$)	130 to 750	V
DC Voltage Range ($V_{M(DC)}$)	175 to 970	V
Transient:		
Peak Pulse Current (I_{TM})		
For 8/20μs Current Wave (See Figure 2)	40,000	A
Single Pulse Energy Range		
For 10/1000μs Current Wave (W_{TM})	270 to 1050	J
Operating Ambient Temperature Range (T_A)	-55 to 85	^oC
Storage Temperature Range (T_{STG})	-55 to 125	^oC
Temperature Coefficient (αV) of Clamping Voltage (V_C) at Specified Test Current	<0.01	%/^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Device Ratings and Specifications

MODEL NUMBER	SIZE	MAXIMUM RATINGS (85°C)				SPECIFICATIONS (25°C)				
		CONTINUOUS		TRANSIENT		VARISTOR VOLTAGE AT 1 mA DC TEST CURRENT			MAXIMUM CLAMPING VOLTAGE (Vc) AT 200A (8/20μs)	TYPICAL CAPACITANCE
		V_{RMS}	V_{DC}	ENERGY (2ms)	PEAK CURRENT (8/20μs)					
		$V_{M(AC)}$	$V_{M(DC)}$	W_{TM}	I_{TM}	MIN	$V_{N(DC)}$	MAX	V_C	f = 1MHz
	(mm)	(V)	(V)	(V)	(A)	(V)	(V)	(V)	(V)	(pF)
V131NA34	34	130	175	270	30,000	184	200	228	345	10,000
V151NA34	34	150	200	300	30,000	212	240	268	405	8,000
V251NA34	34	250	330	370	40,000	354	390	429	650	5,000
V271NA34	34	275	369	400	40,000	389	430	473	730	4,500
V321NA34	34	320	420	460	40,000	462	510	539	830	3,800
V421NA34	34	420	560	600	40,000	610	680	748	1,130	3,000
V481NA34	34	480	640	650	40,000	670	750	825	1,240	2,700
V511NA34	34	510	675	700	40,000	735	820	910	1,350	2,500
V571NA34	34	575	730	770	40,000	805	910	1000	1,480	2,200
V661NA34	34	660	850	900	40,000	940	1050	1160	1,720	2,000
V751NA34	34	750	970	1050	40,000	1080	1200	1320	2,000	1,800

Average power dissipation of transients not to exceed 2.0W.

Power Dissipation Ratings

Continuous power dissipation capability is not an applicable requirement for a suppressor, unless transients occur in rapid succession. Under this condition, the average power dissipation required is simply the energy (watt-seconds) per pulse times the number of pulses per second. The power so developed must be within the specifications shown on the Device Ratings and Specifications table for the specific device.

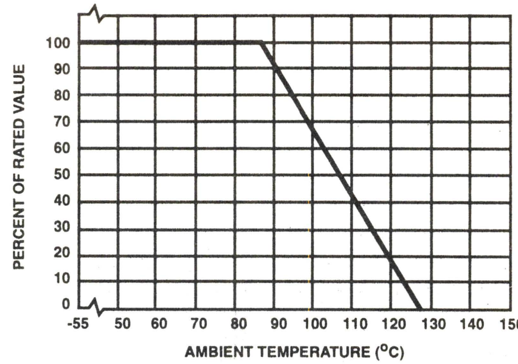
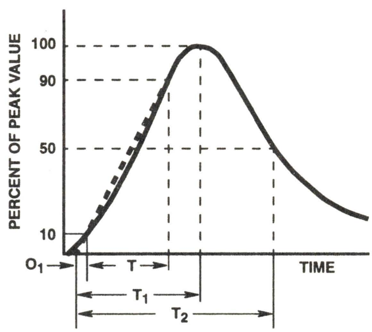


FIGURE 1. CURRENT, ENERGY AND POWER DERATING CURVE



O_1 = Virtual Origin of Wave
T = Time From 10% to 90% of Peak
T_1 = Virtual Front time = 1.25 • t
T_2 = Virtual Time to Half Value (Impulse Duration)
Example: For an 8/20µs Current Waveform:
8µs = T_1 = Virtual Front Time
20µs = T_2 = Virtual Time to Half Value

FIGURE 2. PEAK PULSE CURRENT TEST WAVEFORM

Transient V-I Characteristics Curves

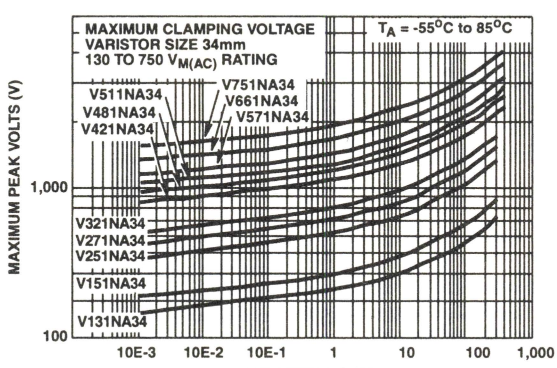


FIGURE 3. CLAMPING VOLTAGE FOR V131NA34 - V751NA34

Pulse Rating Curves

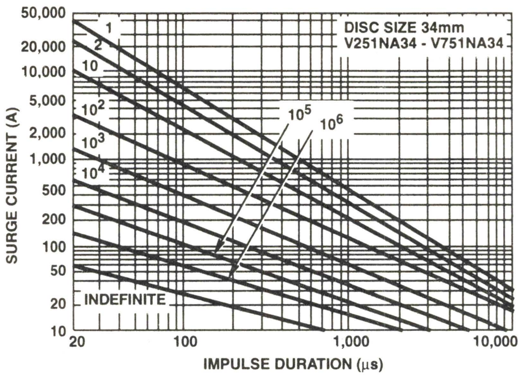


FIGURE 4. SURGE CURRENT RATING CURVES FOR V251NA34 - V751NA34

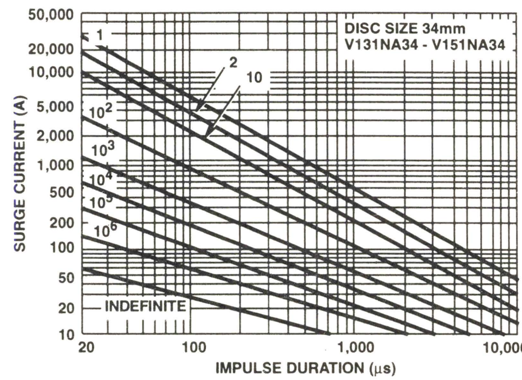
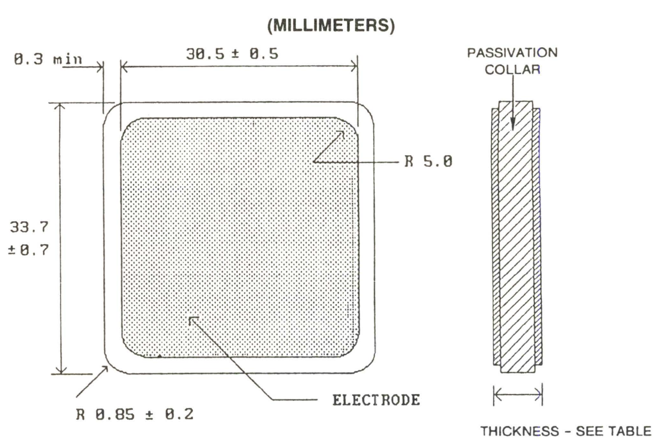


FIGURE 5. SURGE CURRENT RATING CURVES FOR V131NA34, V151NA34

NOTE: If pulse ratings are exceeded, a shift of $V_{N(DC)}$ (at specified current) of more than ±10% could result. This type of shift, which normally results in a decrease of $V_{N(DC)}$, may result in the device not meeting the original published specifications, but it does not prevent the device from continuing to function, and to provide ample protection.

Mechanical Dimensions



MODEL NUMBER	NA SERIES VARISTOR THICKNESS			
	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
V131NA34	1.40	2.30	0.055	0.090
V151NA34	1.70	2.80	0.067	0.011
V251NA34	2.00	2.70	0.079	0.106
V271NA34	2.20	3.00	0.087	0.118
V321NA34	2.60	3.50	0.102	0.138
V421NA34	3.50	4.70	0.138	0.185
V481NA34	3.80	5.20	0.150	0.205
V511NA34	4.20	5.70	0.165	0.225
V571NA34	4.60	6.30	0.181	0.248
V661NA34	5.30	7.20	0.209	0.284
V751NA34	6.10	8.30	0.240	0.327

NOTE: Parts available encapsulated with soldered tabs, to standard design or customer specific requirements.

Passivation Layer

The standard NA Series is supplied with passivation layer around the outside perimeter of the disc forming an electrical insulator as detailed in the dimensional drawing.

Encapsulated Recommendations

After lead attachment, the disc/lead assembly may be coated or encapsulated in a package to provide electrical insulation and isolation from environmental contamination as required by the application. Coating/Filler materials for containers may include silicones, polyurethanes, and some epoxy resins. Two examples of acceptable polyurethanes are Dexter Hysol (US7013, parts A and B) and Rhenatech (resin 4714, hardener 4900), or their equivalents. Materials containing halogens, sulphides, or alkalines are not recommended.

Electrode Metallization

The NA Series is supplied with a sintered silver metallization for the electrode finish. The silver metallization is typically used for solder reflow lead attach operations (I-R, Vapour-Phase).

The recommended temperature profile of a belt-fed convection oven is shown in Figure 6.

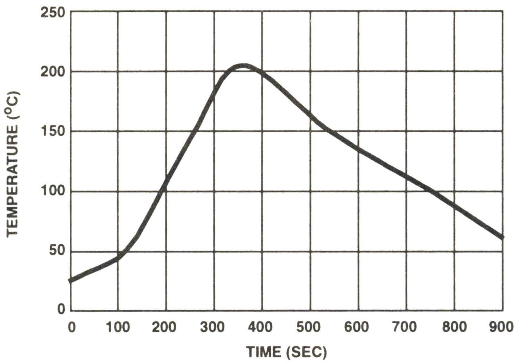


FIGURE 6. TYPICAL BELT OVEN TEMPERATURE PROFILE

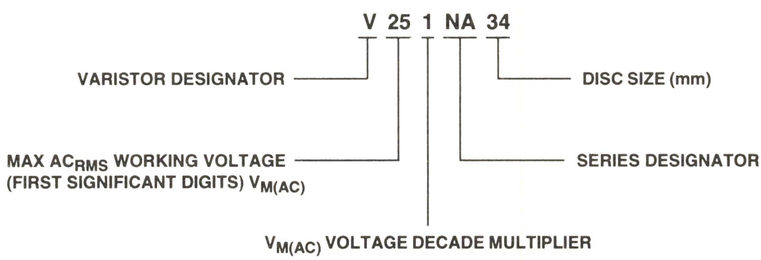
Stacking and Contact Pressure Recommendations

When applications require the stacking of Harris NA discs or when electrical connection is made by pressure contacts, the minimum pressure applied to the disc electrode surface should be 2.2kGs (5 pounds). The maximum recommended pressure applied to the disc electrode is $16N/CM^2$ ($23LBs/IN^2$).

Packaging and Shipping

The NA Series is supplied in bulk for shipment. Discs are packaged in compartmentized cartons to protect from scratching or edge-chipping during shipment.

Ordering Information



HARRIS SEMICONDUCTOR

CH Series

January 1998

Surface Mount Metal-Oxide Varistors

Features

- Recognized as “Transient Voltage Surge Suppressors”, UL File #E75961 to Std. 1449
- Recognized as “Protectors for Data Communication and Fire Alarm Circuits”, UL File #E135010 to Std. 497B
- Leadless, Surface Mount Chip in 5 x 8mm Size
- Voltage Ratings $V_{M(AC)RMS}$ . . . . 10V to 275V
- Supplied in Tape and Reel or Bulk Pack
- No Derating up to 125°C Ambient

Description

CH series transient surge suppressors are small, metal-oxide varistors (MOVs) manufactured in leadless chip form. They are intended for use in a variety of applications from low voltage DC to off-line board-level protection.

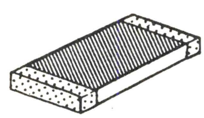
These devices, which have significantly lower profiles than traditional radial-lead varistors, permit designers to reduce the size and weight and increase the reliability of their equipment designs.

CH series varistors are available in a voltage range from 14V to 275V $V_{M(AC)RMS}$, and energy ratings up to 23J.

See the Harris Multilayer Suppressor Series also.

Packaging

CH SERIES



Absolute Maximum Ratings For ratings of individual members of a series, see Device Ratings and Specifications chart

	CH SERIES	UNITS
Continuous:		
Steady State Applied Voltage:		V
AC Voltage Range ($V_{M(AC)RMS}$)	10 to 275	V
DC Voltage Range ($V_{M(DC)}$)	14 to 369	V
Transient:		
Peak Pulse Current (I_{TM})		
For 8/20μs Current Wave (See Figure 2)	250 to 500	A
Single Pulse Energy Range		
For 10/1000μs Current Wave (W_{TM})	0.8 to 23	J
Operating Ambient Temperature Range (T_A)	-55 to 125	°C
Storage Temperature Range (T_{STG})	-55 to 150	°C
Temperature Coefficient (αV) of Clamping Voltage (V_C) at Specified Test Current	<0.01	%/°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Device Ratings and Specifications

V180 - V240 CH Varistors are listed under UL file #E75961 as a recognized component.
Series CH Varistors are listed under UL file #E135010 as a recognized component.

PART NUMBER	MAXIMUM RATINGS (125°C)				SPECIFICATIONS (25°C)					
	CONTINUOUS		TRANSIENT		VARISTOR VOLTAGE AT 1mA DC TEST CURRENT			MAX CLAMPING VOLT V_C AT TEST CURRENT (8/20μs)		TYPICAL CAPACI-TANCE
	V_{RMS}	V_{DC}	ENERGY (10/1000μs)	PEAK CURRENT (8/20μs)						
	$V_{M(AC)}$	$V_{M(DC)}$	W_{TM}	I_{TM}	MIN	$V_{N(DC)}$	MAX	V_C	I_P	f = 1MHz
	(V)	(V)	(J)	(A)	(V)	(V)	(V)	(V)	(A)	(pF)
V22CH8	14	18 (Note 3)	10.0 (Note 2)	250	18.7	22.0	26.0	47	5	1600
V27CH8	17	22	1.0	250	23.0	27.0	31.1	57	5	1300
V33CH8	20	26	1.2	250	29.5	33.0	36.5	68	5	1100
V39CH8	25	31	1.5	250	35.0	39.0	43.0	79	5	900
V47CH8	30	38	1.8	250	42.0	47.0	52.0	92	5	800
V56CH8	35	45	2.3	250	50.0	56.0	62.0	107	5	700
V120CH8	75	102	6.0	500	108.0	120.0	132.0	200	10	300
V150CH8	95	127	8.0	500	135.0	150.0	165.0	250	10	250
V180CH8	115	153	10.0	500	162.0	180.0	198.0	295	10	200
V200CH8	130	175	11.0	500	184.0	200.0	228.0	340	10	180
V220CH8	140	180	12.0	500	198.0	220.0	242.0	360	10	160
V240CH8	150	200	13.0	500	212.0	240.0	268.0	395	10	150
V360CH8	230	300	20.0	500	324.0	360.0	396.0	595	10	100
V390CH8	250	330	21.0	500	354.0	390.0	429.0	650	10	90
V430CH8	275	369	23.0	500	389.0	430.0	473.0	710	10	80

NOTES:

1. Power dissipation of transients not to exceed 0.25W.
2. Energy rating for impulse duration of 30ms minimum to one half of peak current value.
3. Also rated to withstand 24V for 5 minutes.

Power Dissipation Ratings

Continuous power dissipation capability is not an applicable design requirement for a suppressor, unless transients occur in rapid succession. Under this condition, the average power dissipation required is simply the energy (watt-seconds) per pulse times the number of pulses per second. The power so developed must be within the specifications shown on the Device Ratings and Specifications table for the specific device. Furthermore, the operating values need to be derated at high temperatures as shown in Figure 1. Because varistors can only dissipate a relatively small amount of average power they are, therefore, not suitable for repetitive applications that involve substantial amounts of average power dissipation.

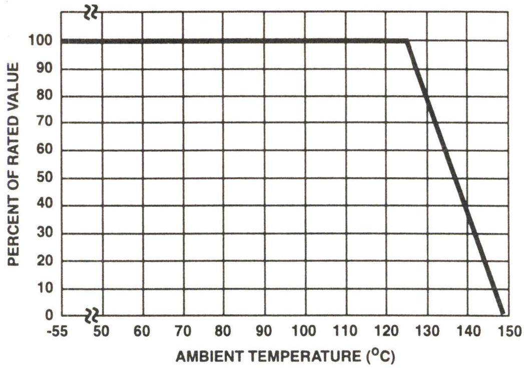
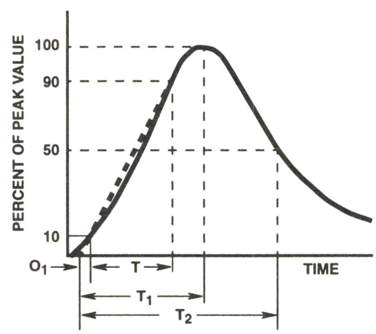


FIGURE 1. CURRENT, ENERGY AND POWER DERATING CURVE



O_1 = Virtual Origin of Wave
T = Time From 10% to 90% of Peak
T_1 = Virtual Front time = 1.25 • t
T_2 = Virtual Time to Half Value (Impulse Duration)
Example: For an 8/20µs Current Waveform:
8µs = T_1 = Virtual Front Time
20µs = T_2 = Virtual Time to Half Value

FIGURE 2. PEAK PULSE CURRENT TEST WAVEFORM

Transient V-I Characteristics Curves

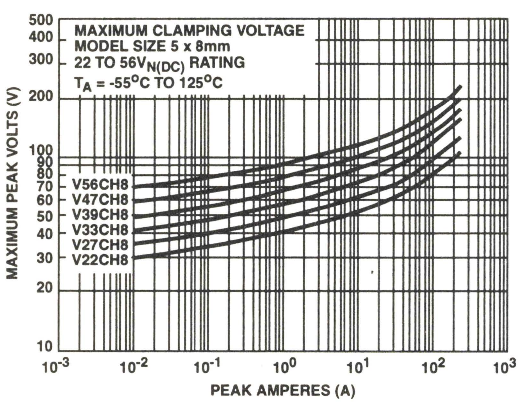


FIGURE 3. CLAMPING VOLTAGE FOR V18CH8 - V68CH8

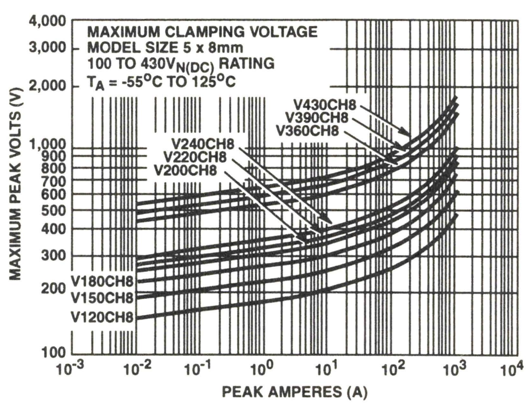


FIGURE 4. CLAMPING VOLTAGE FOR V82CH8 - V430CH8

Pulse Rating Curves

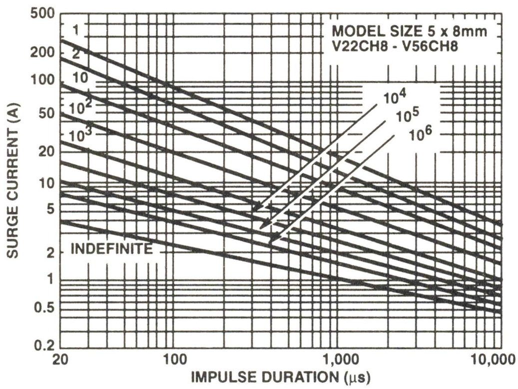


FIGURE 5. SURGE CURRENT RATING CURVES FOR V18CH8 - V68CH8

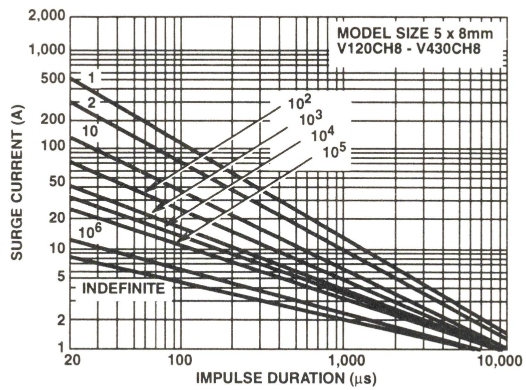
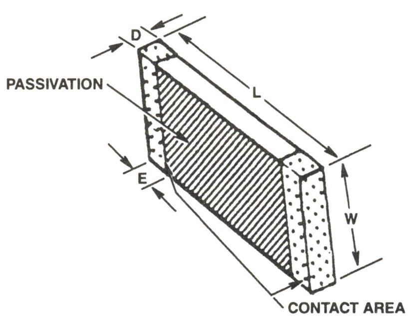


FIGURE 6. SURGE CURRENT RATING CURVES FOR V82CH8 - V430CH8

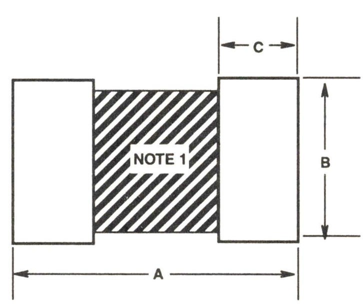
NOTE: If pulse ratings are exceeded, a shift of $V_{N(DC)}$ (at specified current) of more than ±10% could result. This type of shift, which normally results in a decrease of $V_{N(DC)}$, may result in the device not meeting the original published specifications, but it does not prevent the device from continuing to function, and to provide ample protection.

Mechanical Dimensions



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
D	-	0.080	-	2.03
E	0.016	0.050	0.41	1.27
L	0.311	0.335	7.90	8.51
W	0.185	0.207	4.70	5.26

Recommended Pad Outline



SYMBOL	INCHES	MILLIMETERS
A	0.402	10.21
B	0.216	5.50
C	0.087	2.21

NOTE: Avoid metal runs in this area. Soldering recommendations: Material - 62/36/2 Sn/Pb/Ag or equivalent. Temperature - 230°C max., 5 sec. max. Flux - R.M.A.

Ordering Information

Standard Packaging:

CH Series varistors are always shipped in tape and reel. The standard 13-inch reel utilized contains 4000 pieces.

Note also that the CH Series receives no branding on the chip itself.

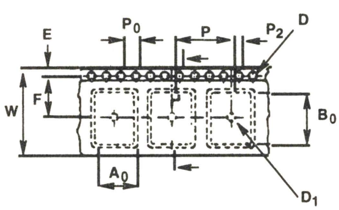
Special Packaging:

Option 1 - 7-inch reels containing 1000 pieces are available. To order 7-inch reels add a T suffix to the part number; e.g., V47CH8T.

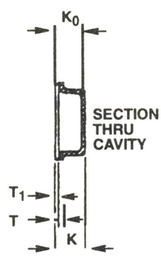
Option 2 - For small quantities (less than 100 pieces) the units are shipped bulk pack. To order, add a S suffix to the part number; e.g., V47CH8S.

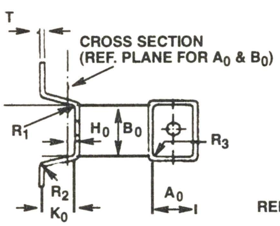
Tape and Reel Specifications

- Conforms to EIA-481, Revision A
- Can be Supplied to IEG Publication 286-3

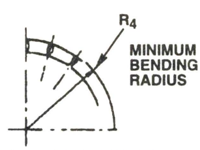


PLAN VIEW OF STRIP





CAVITY DETAILS



REELED RADIUS DETAILS

SYMBOL	PARAMETER	SIZE (mm)
B_0	Cavity Length	8.5 ± 0.1
A_0	Cavity Width	5.5 ± 0.1
K_0	Cavity Depth	2.0 Min.
H_0	Ref. Plane for A_0 and B_0	$0.3^{+0.10}_{-0.05}$
R_1, R_2, R_3	Tape Cavity Radii	0.5 Max.
T	Carrier Tape Thickness	1.0 Max.
T_1	Cover Tape Thickness	0.1 Max.
E	Sprocket Hole from Edge	1.75 ± 0.1
P_0	Sprocket Hole Pitch	4.0 ± 0.1
D	Sprocket Hole Diameter	$1.5^{+0.1}_{-0.0}$
P_2	Hole Centre to Component Centre	2.0 ± 0.15
R_4	Min. Bending Radius	40.0 Min.
D_1	Ejection Hole Dia.	1.5 Min.
K	Overall Thickness	3.0 Min.
P	Pitch Of Component	8.0 ± 0.1
F	Sprocket Hole to Ejection Hole	7.5 ± 0.1
W	Carrier Tape Width	16.0 ± 0.3

V 220 CH 8 X

- V — HARRIS VARISTOR TECHNOLOGY
- 220 — NOMINAL VARISTOR VOLTAGE
- CH — SERIES DESIGNATOR
- 8 — RELATIVE SIZE INDICATOR
- X — PACKAGING OPTIONS
  - No Letter: Standard 13 Inch Reel
  - T: 7 Inch Reel
  - S: Bulk Pack

HARRIS SEMICONDUCTOR

CP Series

January 1998

Tubular Metal-Oxide Varistors

Features

- Unique Coaxial Design and Mounting Arrangement in Tubular Form
- Designed to be Integrated Within Standard Connector Assemblies
- Wide Operating Voltage Range $V_{M(AC)RMS}$ . . 6V to 150V
- Can be Used with 16, 20, or 22 Gauge Standard Connector Pins
- No Derating up to 125°C Ambient

Description

The CP Series of transient voltage surge suppressors are metal-oxide varistors (MOVs) of tubular construction. These varistors are intended for mounting within a multipin connector assembly. This series is available in a wide range of voltage ratings from 6V to 150V $V_{M(AC)RMS}$. Their internal dimensions allow them to be used with 16, 20, or 22 gauge connector pins. The unique coaxial mounting arrangement of these tubular varistors allow them to become part of a transmission line itself. Added inductive lead effects are eliminated.

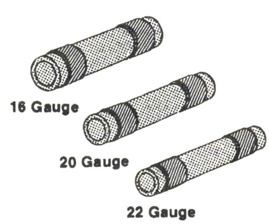
Varistor action takes place between the inside and outside diameters of the tube. Typically, data or signal lines make electrical connection to the inside of the tube. The outside tube surface is then connected to ground or common.

4

VARISTOR PRODUCTS

Packaging

CP SERIES



Absolute Maximum Ratings

For ratings of individual members of a series, see Device Ratings and Specifications chart

Continuous:		
Steady State Applied Voltage:		
AC Voltage Range ($V_{M(AC)RMS}$)	6 to 150	V
DC Voltage Range ($V_{M(DC)}$)	8 to 150	V
Transient:		
Peak Pulse Current (I_{TM})		
For 8/20µs Current Wave (See Figure 2)	250 to 500	A
Single Pulse Energy Range		
For 10/1000µs Current Wave (W_{TM})	1.5 to 5	J
Operating Ambient Temperature Range (T_A)	-55 to 125	^oC
Storage Temperature Range (T_{STG})	-55 to 150	^oC
Temperature Coefficient (αV) of Clamping Voltage (V_C) at Specified Test Current	<0.01	$\%/^oC$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Device Ratings and Specifications

		MAXIMUM RATINGS (125^oC)				SPECIFICATIONS (25^oC)						
		CONTINUOUS		TRANSIENT								
		V_{RMS}	V_{DC}	ENERGY (10/1000 µs)	PEAK CURRENT (8/20µs)	VARISTOR VOLTAGE AT 1mA DC TEST CURRENT			MAX. CLAMPING VOLTAGE V_C AT TEST CURRENT (8/20µs)		CAPACITANCE AT f = 1MHz	
MODEL NUMBER	PART SIZE	$V_{M(AC)}$	$V_{M(DC)}$	W_{TM}	I_{TM}	MIN	$V_{N(DC)}$	MAX	V_C	I_P	MIN	MAX
		(V)	(V)	(J)	(A)	(V)	(V)	(V)	(V)	(A)	(pF)	(pF)
V8CP22	22B	6.0	8.0	1.5	250	12.5	16.0	19.5	34.0	10	1600	2950
V14CP22	22B	10.0	14.0	1.5	250	18.5	22.0	25.5	42.0	10	1600	2950
V31CP22	22B	25.0	31.0	1.5	250	35.0	39.0	48.0	85.0	5	450	1950
V38CP22	22B	30.0	38.0	1.5	250	42.0	47.0	58.0	100.0	5	450	1950
V130CP22	22A	130.0	130.0	2.4	300	184.0	200.0	228.0	375.0	5	150	350
V150CP22	22A	150.0	150.0	2.4	300	212.0	240.0	268.0	430.0	5	100	300
V31CP20	20B	25.0	31.0	2.0	300	35.0	39.0	48.0	85.0	10	700	2200
V38CP20	20B	30.0	38.0	2.0	300	42.0	47.0	58.0	100.0	10	650	1950
V130CP20	20A	130.0	130.0	3.0	400	184.0	200.0	228.0	375.0	10	150	400
V150CP20	20A	150.0	150.0	3.0	400	212.0	240.0	268.0	430.0	10	100	350
V38CP16	16A	30.0	38.0	3.0	350	42.0	47.0	58.0	100.0	20	1000	2750
V130CP16	16A	130.0	130.0	5.0	500	184.0	200.0	228.0	375.0	20	250	700
V150CP16	16A	150.0	150.0	5.0	500	212.0	240.0	268.0	430.0	20	200	650

Average power dissipation of transients not to exceed 250mW, 300mW and 350mW for sizes 22AWG, 20AWG and 16AWG, respectively.

Device Leakage Current

MODEL NUMBER	PART SIZE	LEAKAGE CURRENT AT $V_{T(DC)}$ 25°C I_L TYP (μA)	25°C I_L MAX (μA)	125°C I_L TYP (μA)	125°C I_L MAX (μA)	$V_{T(DC)}$ (V)
V8CP22	22B	0.5	5.0	5.0	50	8
V14CP22	22B	0.5	5.0	5.0	50	14
V31CP22	22B	0.5	5.0	5.0	50	28
V38CP22	22B	0.5	5.0	5.0	50	36
V130CP22	22A	0.5	5.0	25.0	100	130
V150CP22	22A	0.5	5.0	25.0	100	150
V31CP20	20B	0.5	5.0	5.0	50	28
V38CP20	20B	0.5	5.0	5.0	50	36
V130CP20	20A	0.5	5.0	25.0	100	130
V150CP20	20A	0.5	5.0	25.0	100	150
V38CP16	16A	0.5	5.0	5.0	50	36
V130CP16	16A	0.5	5.0	25.0	100	130
V150CP16	16A	0.5	5.0	25.0	100	150

Power Dissipation Ratings

Continuous power dissipation capability is not an applicable design requirement for a suppressor, unless transients occur in rapid succession. Under this condition, the average power dissipation required is simply the energy (watt-seconds) per pulse times the number of pulses per second. The power so developed must be within the specifications shown on the Device Ratings and Specifications table for the specific device. Furthermore, the operating values need to be derated at high temperatures as shown in Figure 1. Because varistors can only dissipate a relatively small amount of average power they are, therefore, not suitable for repetitive applications that involve substantial amounts of average power dissipation.

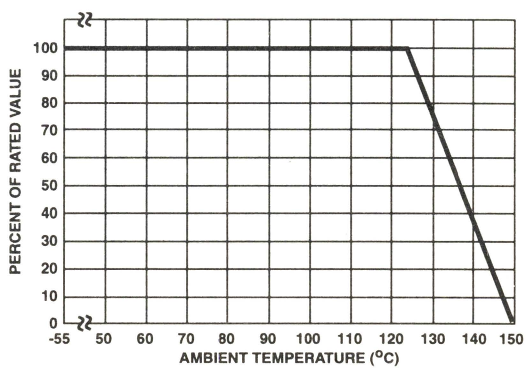
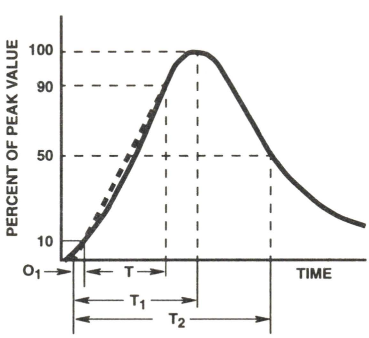


FIGURE 1. CURRENT, ENERGY AND POWER DERATING CURVE



O_1 = Virtual Origin of Wave
T = Time From 10% to 90% of Peak
T_1 = Virtual Front time = 1.25 • t
T_2 = Virtual Time to Half Value (Impulse Duration)
Example: For an 8/20μs Current Waveform:
8μs = T_1 = Virtual Front Time
20μs = T_2 = Virtual Time to Half Value

FIGURE 2. PEAK PULSE CURRENT TEST WAVEFORM

Transient V-I Characteristics Curves

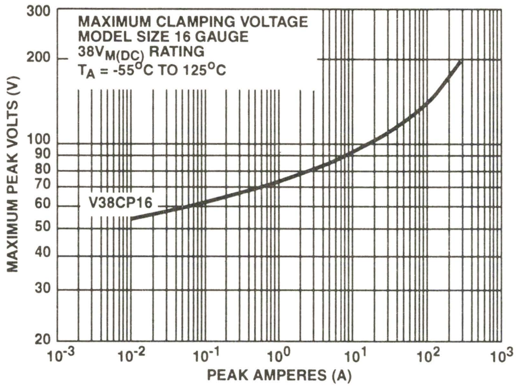


FIGURE 3. CLAMPING VOLTAGE FOR V38CP16

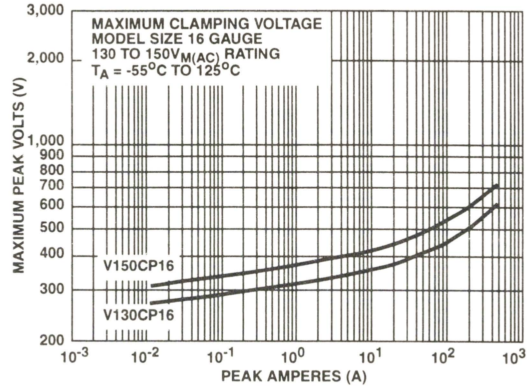


FIGURE 4. CLAMPING VOLTAGE FOR V130CP16 - V150CP16

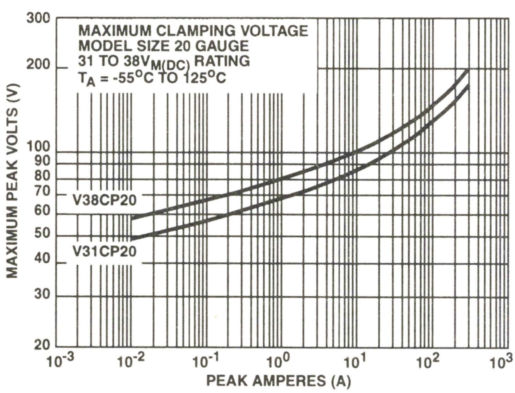


FIGURE 5. CLAMPING VOLTAGE FOR V31CP20 - C38CP20

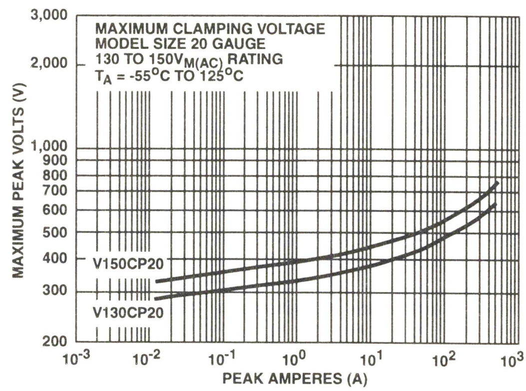


FIGURE 6. CLAMPING VOLTAGE FOR V130CP20 - V150CP20

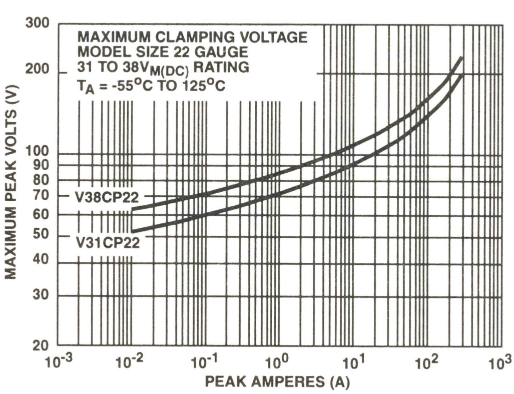


FIGURE 7. CLAMPING VOLTAGE FOR V31CP22 - V38CP22

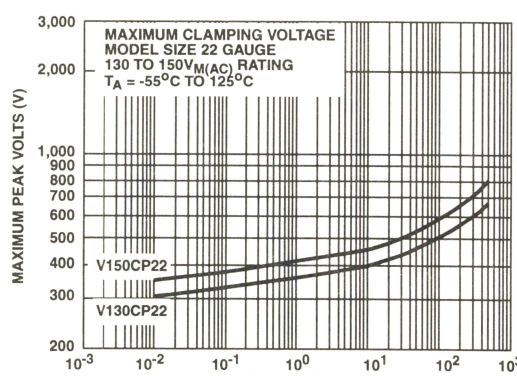


FIGURE 8. CLAMPING VOLTAGE FOR V130CP22 - V150CP22

Transient V-I Characteristics Curves (Continued)

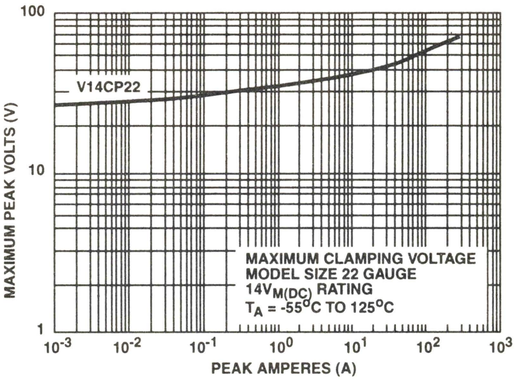


FIGURE 9. CLAMPING VOLTAGE FOR V14CP22

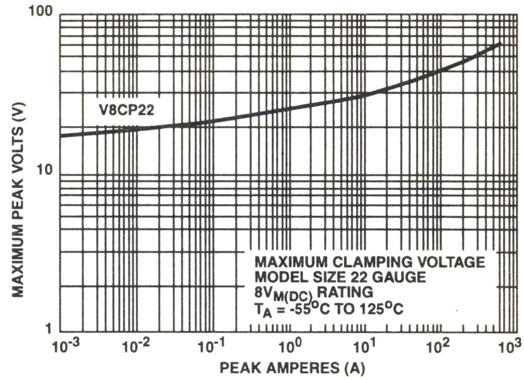


FIGURE 10. CLAMPING VOLTAGE FOR V8CP22

Pulse Rating Curves

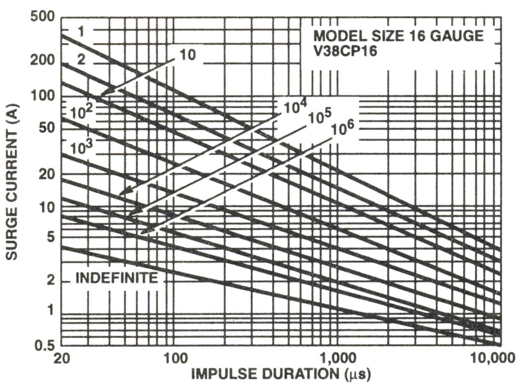


FIGURE 11. SURGE CURRENT RATING CURVES FOR V38CP16

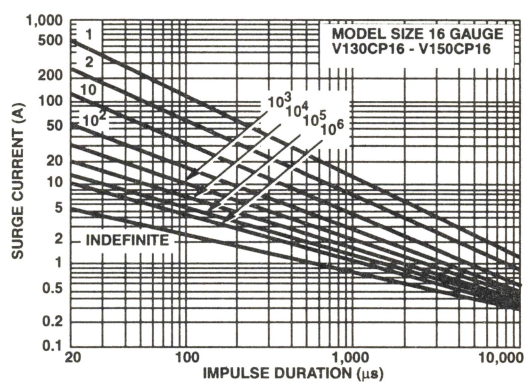


FIGURE 12. SURGE CURRENT RATING CURVES FOR V130CP16 - V150CP16

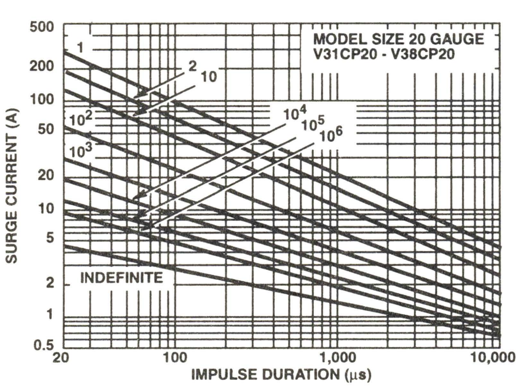


FIGURE 13. SURGE CURRENT RATING CURVES FOR V31CP20 - V38CP20

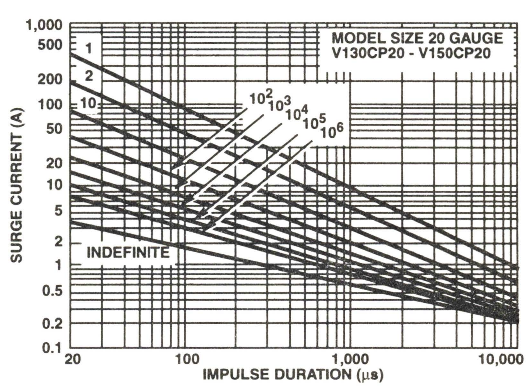


FIGURE 14. SURGE CURRENT RATING CURVES FOR V130CP20 - V150CP20

Pulse Rating Curves (Continued)

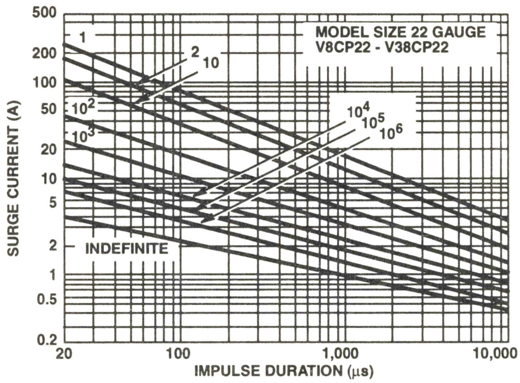


FIGURE 15. SURGE CURRENT RATING CURVES FOR V8CP22 - V38CP22

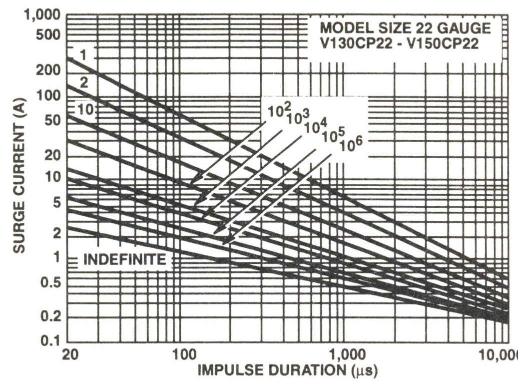
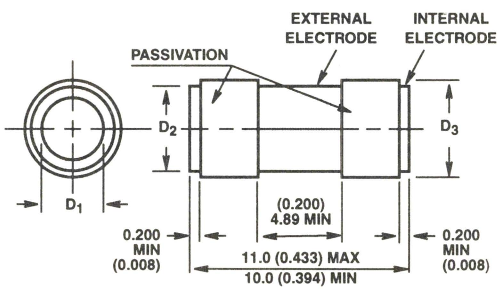


FIGURE 16. SURGE CURRENT RATING CURVES FOR V130CP22 - V150CP22

NOTE: If pulse ratings are exceeded, a shift of $V_{N(DC)}$ (at specified current) of more than ±10% could result. This type of shift, which normally results in a decrease of $V_{N(DC)}$, may result in the device not meeting the original published specifications, but it does not prevent the device from continuing to function, and to provide ample protection.

Mechanical Dimensions



PART SIZE	INTERNAL DIAMETER (D_1)		EXTERNAL DIAMETER (D_2)		PASSIVATION DIAMETER (D_3)	
	MIN	MAX	MIN	MAX	MIN	MAX
22A	0.86 (0.034)	1.02 (0.040)	1.73 (0.068)	1.88 (0.074)	1.83 (0.072)	1.98 (0.078)
22B	0.86 (0.034)	1.25 (0.049)	1.73 (0.068)	1.88 (0.074)	1.83 (0.072)	1.98 (0.078)
20A	1.09 (0.043)	1.25 (0.049)	2.08 (0.082)	2.39 (0.094)	2.18 (0.086)	2.54 (0.100)
20B	1.09 (0.043)	1.83 (0.072)	2.08 (0 .082)	2.39 (0.094)	2.18 (0.086)	2.54 (0.100)
16A	2.27 (0.090)	2.41 (0.095)	3.40 (0.134)	3.56 (0.140)	3.50 (0.138)	3.56 (0.144)

NOTE: Dimensions in millimeters and (inches)

Ordering Information

The CP Series is supplied in bulk pack. Note that this series receives no branding on the device itself.

V XXX CP XX

- V — HARRIS VARISTOR
- XXX — MAXIMUM DC WORKING VOLTAGE (One, Two or Three Digits)
- CP — SERIES DESIGNATOR
- XX — PIN GUAGE SIZE

CS Series

January 1998

Tubular Metal-Oxide Varistors

Features

- **Unique Coaxial Design and Mounting Arrangement in Tubular Form**
- **Designed to be Integrated Within Standard Connector Assemblies**
- **Low Voltage Operating Range $V_{M(DC)}$ . . . . . 8V to 38V**
- **Small Size, Less Than Half the Length of Harris CP Series**
- **No Derating Up to 125°C Ambient**
- **Designed for Use with 22 Guage Standard Connector Pins**

Description

The CS series of transient voltage surge suppressors are metal-oxide varistors (MOVs) of tubular construction. They are designed to provide transient surge protection integrated within a connector/filter for applications in aerospace, automotive, computer and associated industries. These varistors are available in a wide range of voltage rating from $8V_{DC}$ to $38V_{DC}$.

The CS series of suppressors are of similar package construction to the Harris CP series, but differ in size, ratings and characteristics. They offer the advantage of small size and light weight; key benefits in connector assemblies. The unique coaxial mounting arrangement of the CS series allows them to become an integral part of a transmission line. Added inductive lead effects are eliminated.

Varistor action takes place between the inside and outside diameters of the tube. Typically, data or signal lines make electrical connection to the inside of the tube. The outside tube surface is then connected to ground or common.

Ordering Information

The CS Series is supplied in bulk pack. Note that this series receives no branding on the device itself.

V XX CP XX

- **V** — **HARRIS VARISTOR**
- **XX** — **MAXIMUM DC WORKING VOLTAGE** (One or Two Digits)
- **CP** — **SERIES DESIGNATOR**
- **XX** — **PIN GUAGE SIZE**

Packaging

CS SERIES

Absolute Maximum Ratings

For ratings of individual members of a series, see Device Ratings and Specifications chart

	CS SERIES	UNITS
Continuous:		
Steady State Applied Voltage:		
DC Voltage Range ($V_{M(DC)}$)	8 to 38	V
Transient:		
Peak Pulse Current (I_{TM})		
For 8/20µs Current Wave (See Figure 2)	80 to 100	A
Single Pulse Energy Range (W_{TM})		
For 10/1000µs Current Wave	0.5	J
Operating Ambient Temperature Range (T_A)	-55 to 125	^oC
Storage Temperature Range (T_{STG})	-55 to 150	^oC
Temperature Coefficient (αV) of Clamping Voltage (V_C) at Specified Test Current	<0.01	%/^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Device Ratings and Specifications

PART NUMBER	PART SIZE	MAXIMUM RATINGS (125°C)			SPECIFICATIONS (25°C)				
		CONTINUOUS	TRANSIENT		VARISTOR VOLTAGE AT 1mA DC TEST CURRENT		MAXIMUM CLAMPING VOLTAGE V_C AT 10A (8/20µs)	CAPACITANCE AT f = 1MHz	
		V_{DC}	ENERGY (10/1000µs)	PEAK CURRENT (8/20µs)	$V_{N(DC)}$			C	
		$V_{M(DC)}$	W_{TM}	I_{TM}	MIN	MAX	V_C	MIN	MAX
		(V)	(V)	(A)	(V)		(V)	(pF)	
V8CS22	22B	8	0.5	80	13.5	19.5	36	830	1550
V14CS22	22B	14	0.5	80	18.5	25.5	44	675	1250
V18CS22	22B	18	0.5	80	22.5	27.9	47	600	1200
V22CS22	22B	22	0.5	100	27.5	34.5	57	540	1050
V26CS22	22B	26	0.5	100	29.5	36.5	68	510	960
V31CS22	22B	31	0.5	100	35.0	48.0	85	450	880
V38CS22	22B	38	0.5	100	42.0	58.0	100	350	770

NOTE: Average power dissipation of transients not to exceed 200mW

Device Leakage Current

PART NUMBER	LEAKAGE CURRENT AT $V_{M(DC)}$			
	25°C		125°C	
	I_L TYP	I_L MAX	I_L TYP	I_L MAX
	(µA)	(µA)	(µA)	(µA)
V8CS22	0.5	5.0	5.0	50
V14CS22	0.5	5.0	5.0	50
V18CS22	0.5	5.0	5.0	50
V22CS22	0.5	5.0	5.0	50
V26CS22	0.5	5.0	5.0	50
V31CS22	0.5	5.0	5.0	50
V38CS22	0.5	5.0	5.0	50

Power Dissipation Ratings

Continuous power dissipation capability is not an applicable requirement for a suppressor, unless transients occur in rapid succession. Under this condition, the average power dissipation required is simply the energy (watt-seconds) per pulse times the number of pulses per second. The power so developed must be within the specifications shown on the Device Ratings and Specifications table for the specific device. Furthermore, the operating values need to be derated at high temperatures as shown in Figure 1. Because varistors can only dissipate a relatively small amount of average power they are, therefore, not suitable for repetitive applications that involve substantial amounts for average power dissipation.

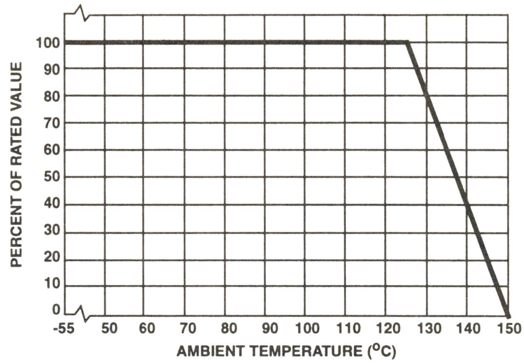
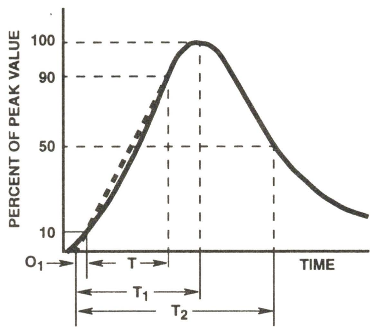


FIGURE 1. CURRENT, ENERGY AND POWER DERATING CURVE



O_1 = Virtual Origin of Wave
T = Time From 10% to 90% of Peak
T_1 = Virtual Front time = 1.25 • t
T_2 = Virtual Time to Half Value (Impulse Duration)

Example: For an 8/20µs Current Waveform:
8µs = T_1 = Virtual Front Time
20µs = T_2 = Virtual Time to Half Value

FIGURE 2. PEAK PULSE CURRENT TEST WAVEFORM

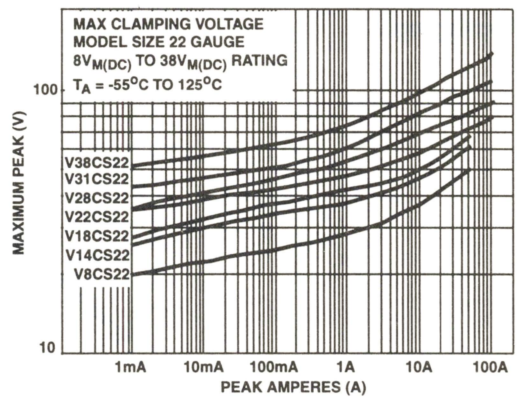
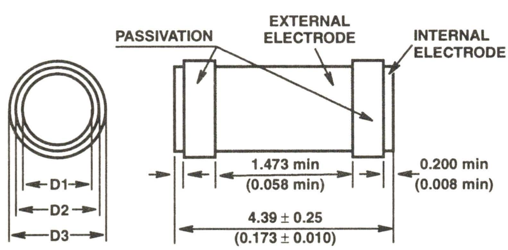


FIGURE 3. CLAMPING VOLTAGE FOR V8CS22 - V38CS22

Mechanical Dimensions



"CS" DIMENSION OUTLINE

DIMENSIONS

PART SIZE	INTERNAL DIAMETER (D1)		EXTERNAL DIAMETER (D2)		PASSIVATION DIAMETER (D3)	
	MIN	MAX	MIN	MAX	MIN	MAX
22B	0.86 (0.034)	1.25 (0.049)	1.73 (0.068)	1.88 (0.074)	1.83 (0.072)	1.98 (0.078)

NOTE: Dimensions in millimeters and (inches)

NOTE:

1. The CS series of connector pin varistors may also be obtained in gauge sizes 16A, 20A, 20B, and 22A AWG, and with continuous operating voltages of up to 100 volts dc. For information on availability of different voltages and sizes, please contact Harris Semiconductor Power Marketing.

4
VARISTOR PRODUCTS

HARRIS SEMICONDUCTOR

MA Series

January 1998

Axial Lead Metal-Oxide Varistors

Features

- 3mm Diameter Disc Size
- Small Axial Lead Package
- Wide Operating Voltage Range
  $V_{M(AC)RMS}$ .... 9V to 264V
  $V_{M(DC)}$ .... 13V to 365V
- Available in Tape and Reel or Bulk Packaging
- No Derating Up to 85°C Ambient

Description

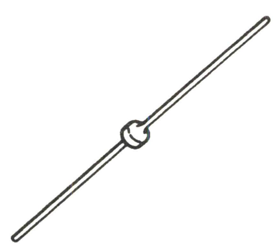
The MA Series of transient surge suppressors are axial-lead metal-oxide varistors (MOVs) for use in a wide variety of board level industrial and commercial electronic equipment. They are intended to protect components and signal/data lines from low energy transients where the small axial lead package is required.

The MA Series is offered with standard (S suffix) or tightened (B suffix) clamping voltage.

See MA Series Device Ratings and Specifications table for part number and brand information.

Packaging

MA SERIES



File Number **2191.4**

Absolute Maximum Ratings
For ratings of individual members of a series, see Device Ratings and Specifications chart

Continuous:		
Steady State Applied Voltage:		
AC Voltage Range ($V_{M(AC)RMS}$)	9 to 264	V
DC Voltage Range ($V_{M(DC)}$)	13 to 365	V
Transient:		
Peak Pulse Current (I_{TM})		
For 8/20µs Current Wave (See Figure 2)	40 to 100	A
Single Pulse Energy Range		
For 10/1000µs Current Wave (W_{TM})	0.06 to 1.7	J
Operating Ambient Temperature Range (T_A)	-55 to 85	°C
Storage Temperature Range (T_{STG})	-55 to 125	°C
Temperature Coefficient (αV) of Clamping Voltage (V_C) at Specified Test Current	<0.01	%/°C
Hi-Pot Encapsulation (Isolation Voltage Capability) (Dielectric must withstand indicated DC voltage for one minute per MIL-STD 202, Method 301)	1000	V
Insulation Resistance	1000	MΩ

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Device Ratings and Specifications

PART NUMBER	BRAND	MAXIMUM RATINGS (85°C) CONTINUOUS V_{RMS} $V_{M(AC)}$ (V)	V_{DC} $V_{M(DC)}$ (V)	TRANSIENT ENERGY (10/1000µs) W_{TM} (J)	PEAK CURRENT (8/20µs) I_{TM} (A)	SPECIFICATIONS (25°C) VARISTOR VOLTAGE AT 1mA DC TEST CURRENT MIN (V)	$V_{N(DC)}$ (V)	MAX (V)	MAX CLAMPING VOLTAGE V_C AT 2.0A (8/20µs) V_C (V)	TYPICAL CAPACITANCE f = 1MHz (pF)
V18MA1A	18A	9	13	0.06	40	14	18	23	49	550
V18MA1B	18B	10	14	0.07	40	15	18	21	44	550
V18MA1S	18S	10	14	0.06	40	15	18	21	49	550
V22MA1A	22A	10	15	0.09	40	16	22	28	55	410
V22MA1B	22B	14	18	0.10	40	19	22	26	51	410
V22MA1S	22S	14	18	0.09	40	19	22	26	55	410
V27MA1A	27A	13	19	0.10	40	21	27	34	67	370
V27MA1B	27B	17	22	0.11	40	24	27	31	59	370
V27MA1S	27S	17	22	0.10	40	24	27	31	67	370
V33MA1A	33A	18	23	0.13	40	26	33	40	73	300
V33MA1B	33B	20	26	0.15	40	29.5	33	36.5	67	300
V33MA1S	33S	20	26	0.14	40	29.5	33	36.5	73	300
V39MA2A	39A	22	28	0.16	40	31	39	47	86	250
V39MA2B	39B	25	31	0.18	40	35	39	43	79	250
V39MA2S	39S	25	31	0.17	40	35	39	43	86	250
V47MA2A	47A	27	34	0.19	40	37	47	57	99	210
V47MA2B	47B	30	38	0.21	40	42	47	52	90	210
V47MA2S	47S	30	38	0.19	40	42	47	52	99	210
V56MA2A	56A	32	40	0.23	40	44	56	68	117	180
V56MA2B	56B	35	45	0.25	40	50	56	62	108	180
V56MA2S	56S	35	45	0.23	40	50	56	62	117	180
V68MA3A	68A	38	48	0.26	40	54	68	82	138	150
V68MA3B	68B	40	56	0.30	40	61	68	75	127	150
V68MA3S	68S	40	56	0.27	40	61	68	75	138	150

Device Ratings and Specifications (Continued)

PART NUMBER	BRAND	MAXIMUM RATINGS (85°C)				SPECIFICATIONS (25°C)				
		CONTINUOUS		TRANSIENT		VARISTOR VOLTAGE AT 1mA DC TEST CURRENT			MAX CLAMPING VOLTAGE V_C AT 2.0A (8/20µs)	TYPICAL CAPACITANCE
		V_{RMS}	V_{DC}	ENERGY (10/1000µs)	PEAK CURRENT (8/20µs)					
		$V_{M(AC)}$	$V_{M(DC)}$	W_{TM}	I_{TM}	MIN	$V_{N(DC)}$	MAX	V_C	f = 1MHz
		(V)	(V)	(J)	(A)	(V)	(V)	(V)	(V)	(pF)
V82MA3A	82A	45	60	0.33	40	65	82	99	163	120
V82MA3B	82B	50	66	0.37	40	73	82	91	150	120
V82MA3S	82S	50	66	0.34	40	73	82	91	163	120
V100MA4A	100	57	72	0.40	40	80	100	120	200	100
V100MA4B	101	60	81	0.45	40	90	100	110	185	100
V100MA4S	102	60	81	0.42	40	90	100	110	200	100
V120MA1A	120	72	97	0.40	100	102	120	138	220	40
V120MA2B	121	75	101	0.50	100	108	120	132	205	40
V120MA2S	122	75	101	0.46	100	108	120	132	220	40
V150MA1A	150	88	121	0.50	100	127	150	173	255	32
V150MA2B	151	92	127	0.60	100	135	150	165	240	32
V180MA1A	180	105	144	0.60	100	153	180	207	310	27
V180MA3B	181	110	152	0.70	100	162	180	198	290	27
V220MA2A	220	132	181	0.80	100	187	220	253	380	21
V220MA4B	221	138	191	0.90	100	198	220	242	360	21
V270MA2A	270	163	224	0.90	100	229	270	311	460	17
V270MA4B	271	171	235	1.00	100	243	270	297	440	17
V330MA2A	330	188	257	1.00	100	280	330	380	570	14
V330MA5B	331	200	274	1.10	100	297	330	363	540	14
V390MA3A	390	234	322	1.20	100	331	390	449	670	12
V390MA6B	391	242	334	1.30	100	351	390	429	640	12
V430MA3A	430	253	349	1.50	100	365	430	495	740	11
V430MA7B	431	264	365	1.70	100	387	430	473	700	11

NOTE: Average power dissipation of transients not to exceed 200mW.

Power Dissipation Ratings

Continuous power dissipation capability is not an applicable design requirement for a suppressor, unless transients occur in rapid succession. Under this condition, the average power dissipation required is simply the energy (watt-seconds) per pulse times the number of pulses per second. The power so developed must be within the specifications shown on the Device Ratings and Specifications table for the specific device. Furthermore, the operating values need to be derated at high temperatures as shown in Figure 1. Because varistors can only dissipate a relatively small amount of average power they are, therefore, not suitable for repetitive applications that involve substantial amounts of average power dissipation.

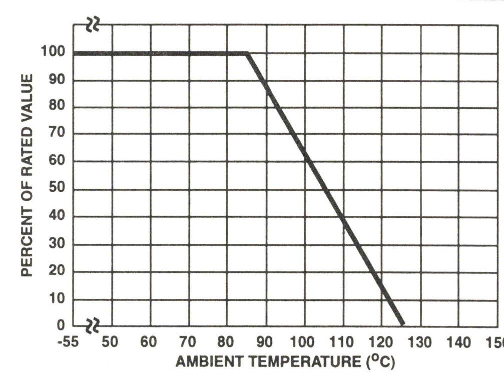
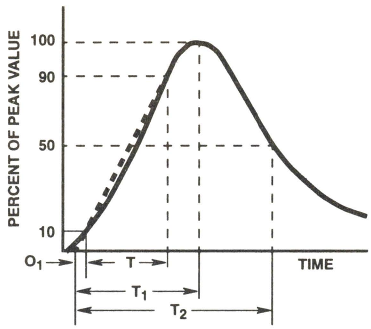


FIGURE 1. CURRENT, ENERGY AND POWER DERATING CURVE



O_1 = Virtual Origin of Wave
T = Time From 10% to 90% of Peak
T_1 = Virtual Front time = 1.25 • t
T_2 = Virtual Time to Half Value (Impulse Duration)
Example: For an 8/20μs Current Waveform:
8μs = T_1 = Virtual Front Time
20μs = T_2 = Virtual Time to Half Value

FIGURE 2. PEAK PULSE CURRENT TEST WAVEFORM

Transient V-I Characteristics Curves

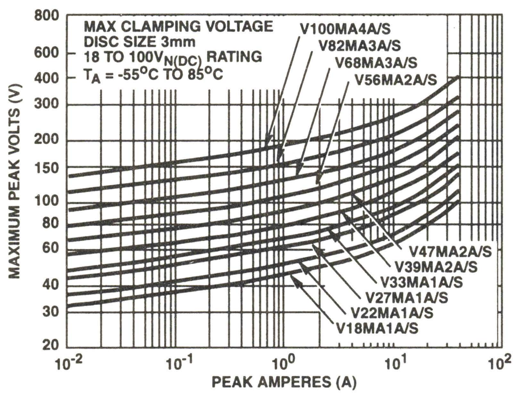


FIGURE 3. CLAMPING VOLTAGE FOR V18MA1A/S - V100MA4A/S

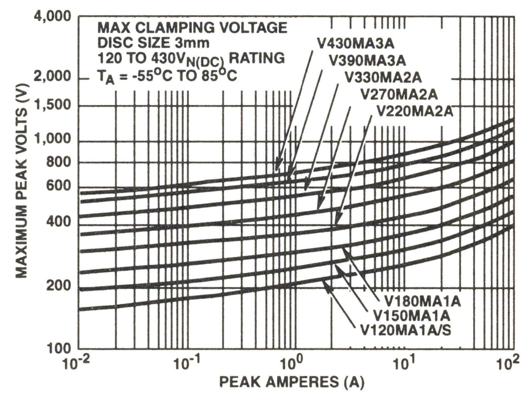


FIGURE 4. CLAMPING VOLTAGE FOR V120MA1A/S - V430MA3A

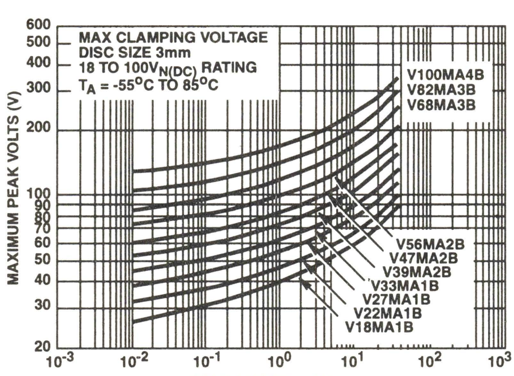


FIGURE 5. CLAMPING VOLTAGE FOR V18MA1B - V100MA4B

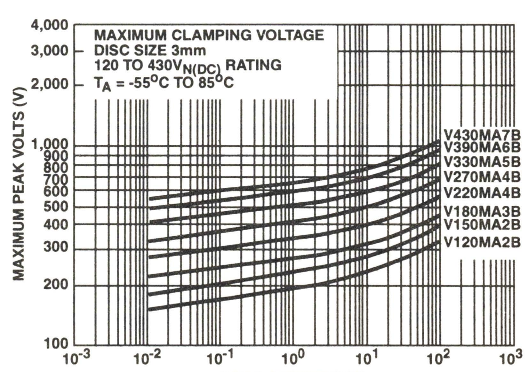


FIGURE 6. CLAMPING VOLTAGE FOR V120MA2B - V430MA7B

Pulse Rating Curves

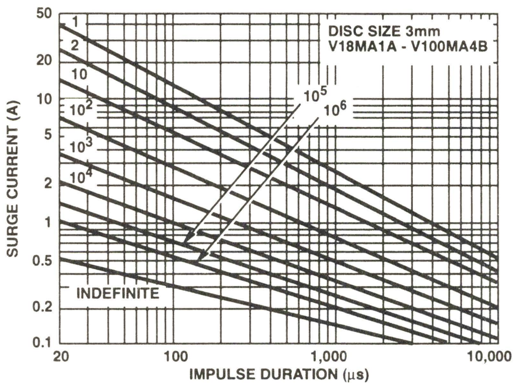


FIGURE 7. SURGE CURRENT RATING CURVES FOR V18MA SERIES - V100MA SERIES

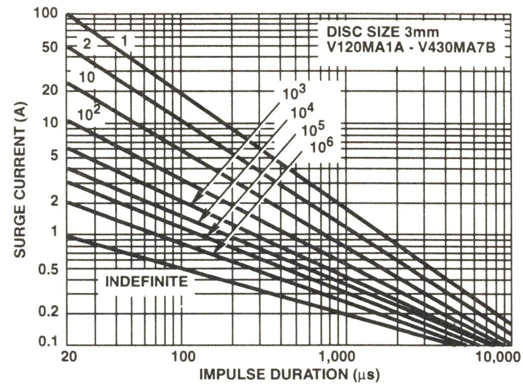
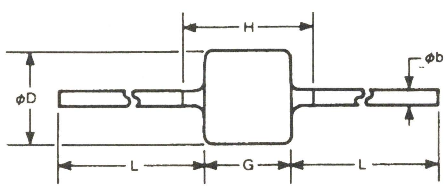


FIGURE 8. SURGE CURRENT RATING CURVES FOR V120MA SERIES - V430MA SERIES

NOTE: If pulse ratings are exceeded, a shift of $V_{N(DC)}$ (at specified current) of more than ±10% could result. This type of shift, which normally results in a decrease of $V_{N(DC)}$, may result in the device not meeting the original published specifications, but it does not prevent the device from continuing to function, and to provide ample protection.

Mechanical Dimensions



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
Øb	0.024	0.026	0.61	0.66
ØD	0.135	0.177	3.43	4.5
G	0.098	0.177	3.43	4.5
H	0.118	0.236	3.0	6.0
L	1.130	1.220	28.70	31.0
Typical Weight = 25g				

Ordering Information

V XXX MA XX

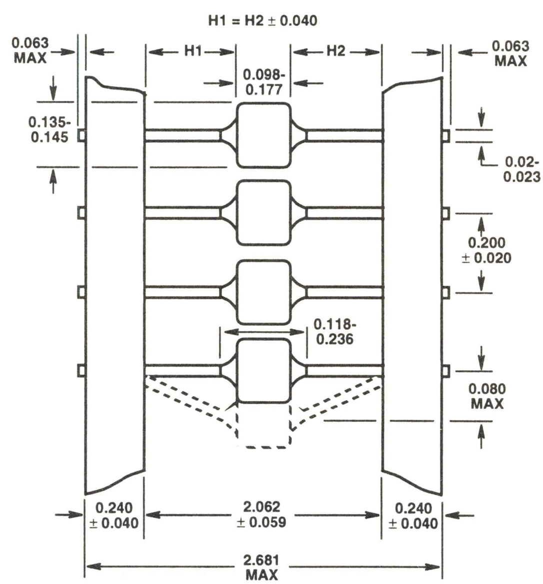
HARRIS VARISTOR

VARISTOR VOLTAGE
(V_N at 1mA)

SERIES DESIGNATOR
Bulk
Use "MT" for Tape and Reel

ENERGY/CLAMPING VOLTAGE VARIANT

Tape and Reel Specification



- Conforms to EIA Standard RS-296E

PA Series

January 1998

Base Mount Metal-Oxide Varistors

Features

- **Recognized as "Transient Voltage Surge Suppressors", UL File #E75961 to Std. 1449**
- **Recognized as "Transient Voltage Surge Suppressors", CSA File #LR91788 to Std. C22.2 No. 1-M1981**
- **Wide Operating Voltage Range $V_{M(AC)RMS}$ . . . . 130V to 660V**
- **Creep and Strike Distance Capability Meets Rigid NEMA Standards**
- **Base Mount Construction Forms One Electrical Connection**
- **Quick Connect Tab Terminal**
- **No Derating Up to 85°C Ambient**

Description

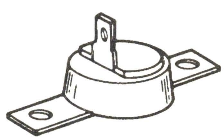
The PA Series of transient surge suppressors are metal-oxide varistors (MOVs) featuring a rigid base mount package construction, and are useful in applications which are subject to vibration.

These UL and CSA recognized varistors are available in a wide range of operating voltages, from 130V to 660V $V_{M(AC)RMS}$. The base-mount package has a quick-connect tab terminal that provides a fast, secure lead attach. The mounting base forms the second electrical connection, usually chassis ground. Meeting rigid NEMA standards, PA series varistors have a creep and strike distance capability that minimizes breakdown along the package surface.

See PA Series Device Ratings and Specifications table for part number and brand information.

Packaging

PA SERIES



Absolute Maximum Ratings

For ratings of individual members of a series, see Device Ratings and Specifications chart

	PA SERIES	UNITS
Continuous:		
Steady State Applied Voltage:		
AC Voltage Range ($V_{M(AC)RMS}$)	130 to 660	V
DC Voltage Range ($V_{M(DC)}$)	175 to 850	V
Transient:		
Peak Pulse Current (I_{TM})		
For 8/20μs Current Wave (See Figure 2)	6500	A
Single Pulse Energy Range		
For 10/1000μs Current Wave (W_{TM})	70 to 250	J
Operating Ambient Temperature Range (T_A)	-55 to 85	^oC
Storage Temperature Range (T_{STG})	-55 to 125	^oC
Temperature Coefficient (αV) of Clamping Voltage (V_C) at Specified Test Current	<0.01	%/^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Device Ratings and Specifications

Series PA Varistors are listed under UL file #E75961 and under CSA file #LR91788, as a UL recognized component.

PART NUMBER AND DEVICE BRANDING	MAXIMUM RATINGS (85°C)				SPECIFICATIONS (25°C)					
	CONTINUOUS		TRANSIENT							
	V_{RMS}	V_{DC}	ENERGY (10/1000μs)	PEAK CURRENT (8/20μs)	VARISTOR VOLTAGE AT 1mA DC TEST CURRENT			MAX CLAMPING VOLT V_C AT TEST CURRENT (8/20μs)		TYPICAL CAPACI-TANCE
	$V_{M(AC)}$	$V_{M(DC)}$	W_{TM}	I_{TM}	MIN	$V_{N(DC)}$	MAX	V_C	I_P	f = 1MHz
	(V)	(V)	(J)	(A)	(V)	(V)	(V)	(V)	(A)	(pF)
V130PA20A	130	175	70	6500	184	200	243	360	100	1900
V130PA20C	130	175	70	6500	184	200	220	325	100	1900
V150PA20A	150	200	80	6500	212	240	284	420	100	1600
V150PA20C	150	200	80	6500	212	240	243	360	100	1600
V250PA40A	250	330	130	6500	354	390	453	675	100	1000
V250PA40C	250	330	130	6500	354	390	413	620	100	1000
V275PA40A	275	369	140	6500	389	430	494	740	100	900
V275PA40C	275	369	140	6500	389	430	453	680	100	900
V320PA40A	320	420	160	6500	462	510	565	850	100	750
V320PA40C	320	420	160	6500	462	510	540	800	100	750
V420PA40A	420	560	170	6500	610	680	790	1160	100	600
V420PA40C	420	560	170	6500	610	680	690	1050	100	600
V480PA80A	480	640	180	6500	670	750	860	1280	100	550
V480PA80C	480	640	180	6500	670	750	790	1160	100	550
V510PA80A	510	675	190	6500	735	820	963	1410	100	500
V510PA80C	510	675	190	6500	735	820	860	1280	100	500
V575PA80A	575	730	220	6500	805	910	1050	1560	100	450
V575PA80C	575	730	220	6500	805	910	960	1410	100	450
V660PA100A	660	850	250	6500	940	1050	1210	1820	100	400
V660PA100C	660	850	250	6500	940	1050	1100	1650	100	400

NOTE: Average power dissipation of transients not to exceed 1W.

Power Dissipation Ratings

Continuous power dissipation capability is not an applicable design requirement for a suppressor, unless transients occur in rapid succession. Under this condition, the average power dissipation required is simply the energy (watt-seconds) per pulse times the number of pulses per second. The power so developed must be within the specifications shown on the Device Ratings and Specifications table for the specific device. Furthermore, the operating values need to be derated at high temperatures as shown in Figure 1. Because varistors can only dissipate a relatively small amount of average power they are, therefore, not suitable for repetitive applications that involve substantial amounts of average power dissipation.

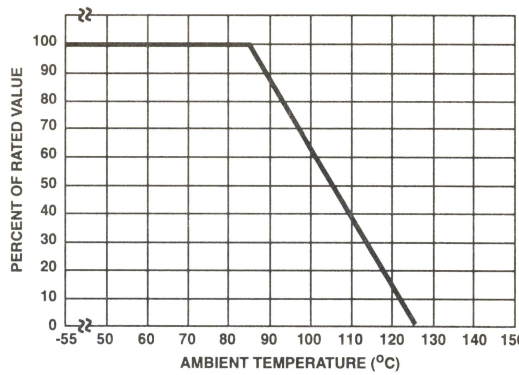
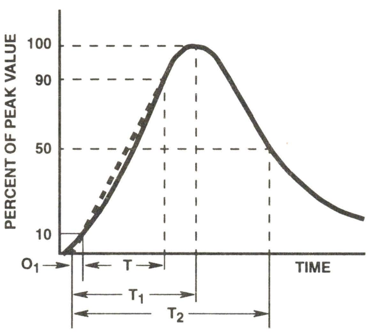


FIGURE 1. CURRENT, ENERGY AND POWER DERATING CURVE



O_1 = Virtual Origin of Wave
T = Time From 10% to 90% of Peak
T_1 = Virtual Front time = 1.25 • t
T_2 = Virtual Time to Half Value (Impulse Duration)
Example: For an 8/20µs Current Waveform:
8µs = T_1 = Virtual Front Time
20µs = T_2 = Virtual Time to Half Value

FIGURE 2. PEAK PULSE CURRENT TEST WAVEFORM

Transient V-I Characteristics Curves

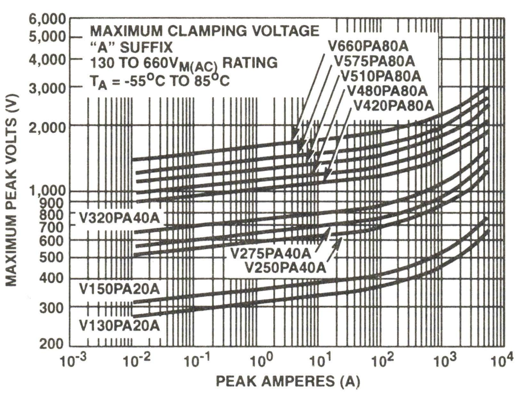


FIGURE 3. CLAMPING VOLTAGE FOR V130PA20A - V660PA100A

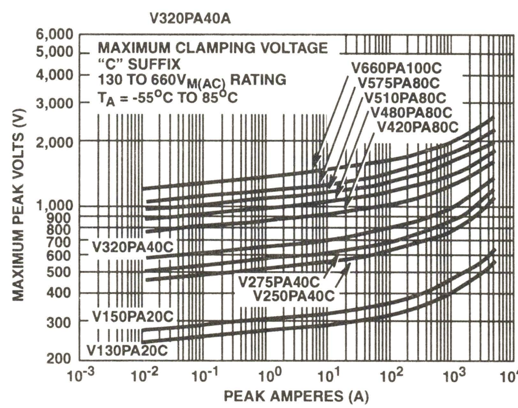


FIGURE 4. CLAMPING VOLTAGE FOR V130PA20C - V660PA100C

Pulse Rating Curves

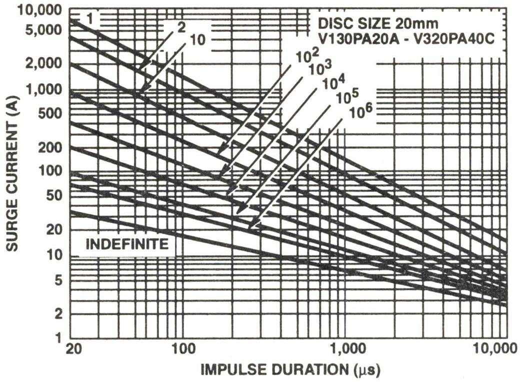


FIGURE 5. SURGE CURRENT RATING CURVES FOR V130PA20A - V320PA40C

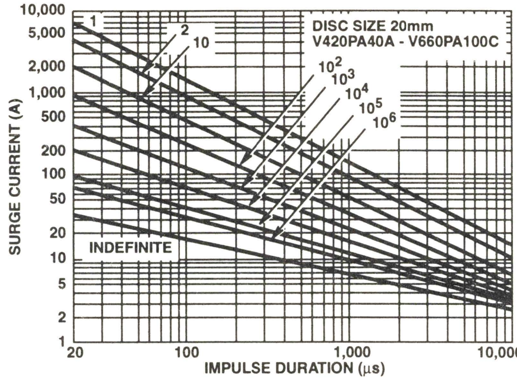
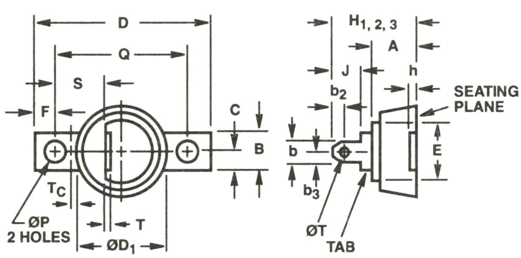


FIGURE 6. SURGE CURRENT RATING CURVES FOR V420PA40A - V660PA100C

NOTE: If pulse ratings are exceeded, a shift of $V_{N(DC)}$ (at specified current) of more than ±10% could result. This type of shift, which normally results in a decrease of $V_{N(DC)}$, may result in the device not meeting the original published specifications, but it does not prevent the device from continuing to function, and to provide transient protection.

Mechanical Dimensions



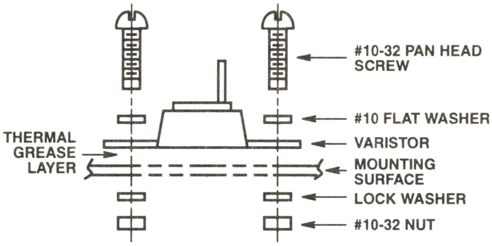
NOTES:

1. Tab is designed to fit 1/4" quick-connect terminal.
2. Case temperature is measured at T_C on top surface of base plate.
3. H_1 (130-150V_{RMS} devices)
   H_2 (250-320V_{RMS} devices)
   H_3 (420-660V_{RMS} devices)
4. Electrical connection: top terminal and base plate.
5. Typical weight: 30g

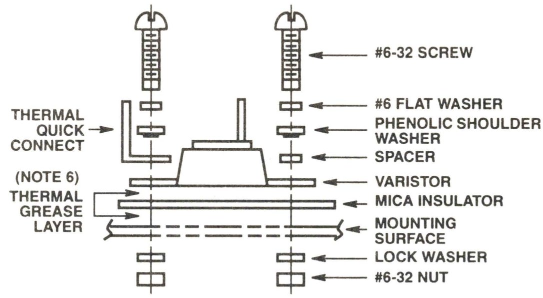
SYMBOL	MILLIMETERS			INCHES			NOTES
	MIN	NOM	MAX	MIN	NOM	MAX	
A	-	-	14.3	-	-	0.570	-
b	-	-	6.6	-	-	0.260	1
b2	3.94	4.06	4.18	0.155	0.160	0.165	-
b3	3.05	3.17	3.29	0.120	0.125	0.130	-
B	-	-	12.9	-	-	0.510	-
C	-	-	6.6	-	-	0.260	-
D	-	-	66.3	-	-	2.610	-
ØD1	-	-	33.5	-	-	1.320	-
E	-	11.2	-	-	0.440	-	-
F	7.50	7.62	7.75	0.295	0.300	0.305	-
h	-	0.8	1.0	-	0.030	0.040	-
H_1	-	-	25.6	-	-	1.010	3
H_2	-	-	28.3	-	-	1.120	3
H_3	-	-	32.8	-	-	1.290	3
J	-	-	8.1	-	-	0.320	-
ØP	5.6	-	6.0	0.220	-	0.240	-
Q	50.6	50.8	51.0	1.990	2.000	2.010	-
S	18.4	19.2	20.0	0.72	0.75	0.78	-
T	-	-	1.0	-	-	0.040	-
ØT	2.8	-	-	0.110	-	-	-
T_C	-	3.2	-	-	0.126	-	2

Suggested Hardware and Mounting Arrangements

TYPICAL NON-ISOLATED MOUNTING



TYPICAL ISOLATED MOUNTING



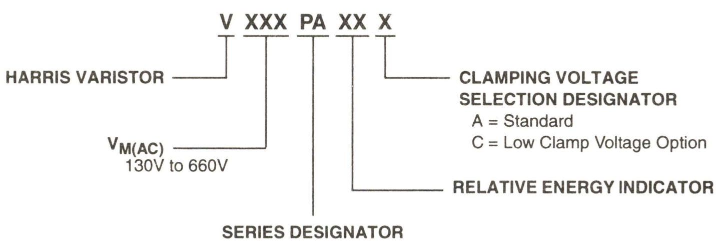
NOTE:

6. GE G623, Dow Corning, DC3, 4, 340, or 640 Thermal Grease recommended for best heat transfer.

1,000V Isolation Kit containing the following parts can be ordered by part #A7811055.

1. MICA insulation 1"/3.1"/0.005" thick	2. Phenolic shoulder washer	2. #6-32/$^3/_4$ screw	2. #6 internal tooth lock washer
1. $^1/_4$" quick-connect terminal	1. Spacer	2. #6-32 nut	2. #6 flat washer

Ordering Information



HARRIS SEMICONDUCTOR

RA Series

January 1998

Low Profile Metal-Oxide Varistors

Features

- **Recognized as "Transient Voltage Surge Suppressors", UL File #E75961 to Std. 1449**
- **Recognized as "Transient Voltage Surge Suppressors", CSA File #LR91788 to Std. C22.2 No. 1-M1981**
- **Recognized as "Across-The-Line Components", UL File #E56529 to Standard 1414**
- **Recognized as "Protectors for Data Communication and Fire Alarm Circuits", UL File #E135010 to Standard 497B**
- **Low Profile Outline with Precise Seating Plane**
- **No Derating up to 125°C Ambient**
- **Wide Operating Voltage Range**
  - $V_{M(AC)RMS}$ .... 4V to 275V
  - $V_{M(DC)}$ .... 5.5V to 369V
- **High Energy Absorption Capability W_{TM} .. up to 140J**
- **3 Model Sizes Available....... RA8, RA16, and RA22**
- **In-Line Leads**

Description

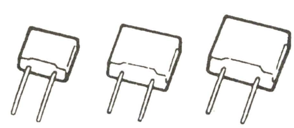
The RA Series transient surge suppressors are varistors (MOVs) supplied in a low-profile box that features a precise seating plane to increase mechanical stability for secure circuit-board mounting. This feature makes these devices suitable for industrial applications critical to vibration. Their construction permits operation up to 125°C (ambient) without derating.

The RA series are available in voltage ratings up to 275V $V_{M(AC)RMS}$, and energy levels up to 140J. These varistors are used in automotive, motor-control, telecommunication, and military applications.

See RA Series Device Ratings and Specifications table for part number and brand information.

Packaging

RA SERIES



Absolute Maximum Ratings

For ratings of individual members of a series, see Device Ratings and Specifications chart

	RA8 SERIES	RA16 SERIES	RA22 SERIES	UNITS
Continuous:				
Steady State Applied Voltage:				
AC Voltage Range ($V_{M(AC)RMS}$)	4 to 275	10 to 275	4 to 275	V
DC Voltage Range ($V_{M(DC)}$)	5.5 to 369	14 to 369	18 to 369	V
Transient:				
Peak Pulse Current (I_{TM})				
For 8/20µs Current Wave (See Figure 2)	100 to 1200	1000 to 4500	2000 to 6500	A
Single Pulse Energy Range (Note 1)				
For 10/1000µs Current Wave (W_{TM})	0.4 to 23	3.5 to 75	70 to 160	J
Operating Ambient Temperature Range (T_A)	-55 to 125	-55 to 125	-55 to 125	^oC
Storage Temperature Range (T_{STG})	-55 to 150	-55 to 150	-55 to 150	^oC
Temperature Coefficient (αV) of Clamping Voltage (V_C) at Specified Test Current	<0.01	<0.01	<0.01	%/^oC
Hi-Pot Encapsulation (Isolation Voltage Capability) (Dielectric must withstand indicated DC voltage for one minute per MIL-STD 202, Method 301)	5000	5000	5000	V
Insulation Resistance	1000	1000	1000	MΩ

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Device Ratings and Specifications (Note 1)

PART NUMBER	BRAND	MAXIMUM RATINGS (125°C)				SPECIFICATIONS (25°C)					
		CONTINUOUS		TRANSIENT		VARISTOR VOLTAGE AT 1mA DC TEST CURRENT			MAX CLAMPING VOLTAGE V_C AT TEST CURRENT (8/20µs)		TYPICAL CAPACI-TANCE
		V_{RMS}	V_{DC}	ENERGY (10/1000µs)	PEAK CURRENT (8/20µs)						
		$V_{M(AC)}$	$V_{M(DC)}$	W_{TM}	I_{TM}	MIN	$V_{N(DC)}$	MAX	V_C	I_P	f = 1MHz
		(V)	(V)	(J)	(A)	(V)	(V)	(V)	(V)	(A)	(pF)
RA8 SERIES	Series RA8 Varistors of 130VRMS or greater are listed under UL File No. E75961 as a recognized component. CSA approved File No. LR91788										
V8RA8	8R	4	5.5	0.4	150	6	8.2	11.2	22	5	3000
V12RA8	12R	6	8	0.6	150	9	12	16	34	5	2500
V18RA8	18R	10	14	0.8	250	14.4	18	21.6	42	5	2000
V22RA8	22R	14	18 (Note 3)	10 (Note 2)	250	18.7	22	26	47	5	1600
V27RA8	27R	17	22	1.0	250	23	27	31.1	57	5	1300
V33RA8	33R	20	26	1.2	250	29.5	33	36.5	68	5	1100
V39RA8	39R	25	31	1.5	250	35	39	43	79	5	900
V47RA8	47R	30	38	1.8	250	42	47	52	92	5	800
V56RA8	56R	35	45	2.3	250	50	56	62	107	5	700
V68RA8	68R	40	56	3.0	250	61	68	75	127	5	600
V82RA8	82R	50	66	4.0	1200	74	82	91	135	10	500
V100RA8	100R	60	81	5.0	1200	90	100	110	165	10	400
V120RA8	120R	75	102	6.0	1200	108	120	132	205	10	300
V150RA8	150R	95	127	8.0	1200	135	150	165	250	10	250
V180RA8	180R	115	153	10.0	1200	162	180	198	295	10	200
V200RA8	200R	130	175	11.0	1200	184	200	228	340	10	180
V220RA8	220R	140	180	12.0	1200	198	220	242	360	10	160
V240RA8	240R	150	200	13.0	1200	212	240	268	395	10	150
V270RA8	270R	175	225	15.0	1200	247	270	303	455	10	130

Device Ratings and Specifications (Note 1) (Continued)

		MAXIMUM RATINGS (125°C)				SPECIFICATIONS (25°C)					
		CONTINUOUS		TRANSIENT		VARISTOR VOLTAGE AT 1mA DC TEST CURRENT			MAX CLAMPING VOLTAGE V_C AT TEST CURRENT (8/20μs)		TYPICAL CAPACITANCE
		V_{RMS}	V_{DC}	ENERGY (10/1000μs)	PEAK CURRENT (8/20μs)						
PART NUMBER	BRAND	$V_{M(AC)}$ (V)	$V_{M(DC)}$ (V)	W_{TM} (J)	I_{TM} (A)	MIN (V)	$V_{N(DC)}$ (V)	MAX (V)	V_C (V)	I_P (A)	f = 1MHz (pF)
V360RA8	360R	230	300	20.0	1200	324	360	396	595	10	100
V390RA8	390R	250	330	21.0	1200	354	390	429	650	10	90
V430RA8	430R	275	369	23.0	1200	389	430	473	710	10	80
RA16 SERIES Varistors of 130VRMS or greater are listed under UL File No. E75961 as a recognized component. CSA approved File No. LR91788.											
V18RA16	18R16	10	14	3.5	1000	14.4	18	21.6	39	10	11000
V22RA16	22R16	14	18 (Note 3)	50 (Note 2)	1000	18.7	22	26	43	10	9000
V27RA16	27R16	17	22	5.0	1000	23	27	31.1	53	10	7000
V33RA16	33R16	20	26	6.0	1000	29.5	33	36.5	64	10	6000
V39RA16	39R16	25	31	7.2	1000	35	39	43	76	10	5000
V47RA16	47R16	30	38	8.8	1000	42	47	52	89	10	4500
V56RA16	56R16	35	45	10.0	1000	50	56	62	103	10	3900
V68RA16	68R16	40	56	13.0	1000	61	68	75	123	10	3300
V82RA16	82R16	50	66	15.0	4500	74	82	91	145	50	2500
V100RA16	100R16	60	81	20.0	4500	90	100	110	175	50	2000
V120RA16	120R16	75	102	22.0	4500	108	120	132	205	50	1700
V150RA16	150R16	95	127	30.0	4500	135	150	165	255	50	1400
V180RA16	180R16	115	153	35.0	4500	162	180	198	300	50	1100
V200RA16	200R16	130	175	38.0	4500	184	200	228	340	50	1000
V220RA16	220R16	140	180	42.0	4500	198	220	242	360	50	900
V240RA16	240R16	150	200	45.0	4500	212	240	268	395	50	800
V270RA16	270R16	175	225	55.0	4500	247	270	303	455	50	700
V360RA16	360R16	230	300	70.0	4500	324	360	396	595	50	550
V390RA16	390R16	250	330	72.0	4500	354	390	429	650	50	500
V430RA16	430R16	275	369	75.0	4500	389	430	473	710	50	450
RA22 SERIES Varistors of 130VRMS or greater are listed under UL File No. E75961 as a recognized component. CSA approved File No. LR91788.											
V24RA22	24R22	14	18 (Note 3)	100.0 (Note 2)	2000	19.2	24 (Note 4)	26	43	20	18000
V36RA22	36R22	23	31	160.0 (Note 2)	2000	32	36 (Note 4)	40	63	20	12000
V200RA22	200R22	130	175	70.0	6500	184	200	228	340	100	1900
V240RA22	240R22	150	200	80.0	6500	212	240	268	395	100	1600
V270RA22	270R22	175	225	90.0	6500	247	270	303	455	100	1400
V390RA22	390R22	250	330	130.0	6500	354	390	429	650	100	1000
V430RA22	430R22	275	369	140.0	6500	389	430	473	710	100	900

NOTES:

1. Average power dissipation of transients not to exceed 0.25W for RA8 Series, 0.60W for RA16 Series, or 1.0W for RA22 Series.
2. Energy ratings for impulse duration of 30ms minimum to one half of peak current value.
3. Also rated to withstand 24V for 5 minutes.
4. 10mA DC Test Current.

Power Dissipation Ratings

Continuous power dissipation capability is not an applicable design requirement for a suppressor, unless transients occur in rapid succession. Under this condition, the average power dissipation required is simply the energy (watt-seconds) per pulse times the number of pulses per second. The power so developed must be within the specifications shown on the Device Ratings and Specifications table for the specific device. Furthermore, the operating values need to be derated at high temperatures as shown in Figure 1. Because varistors can only dissipate a relatively small amount of average power they are, therefore, not suitable for repetitive applications that involve substantial amounts of average power dissipation.

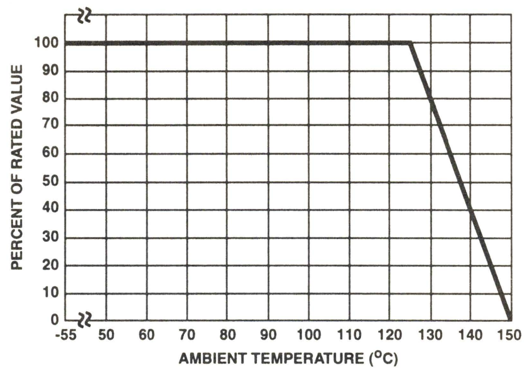
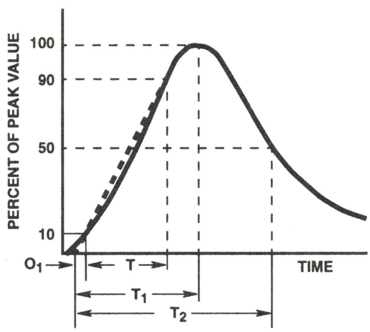


FIGURE 1. CURRENT, ENERGY AND POWER DERATING CURVE



O_1 = Virtual Origin of Wave
T = Time From 10% to 90% of Peak
T_1 = Virtual Front time = 1.25 • t
T_2 = Virtual Time to Half Value (Impulse Duration)
Example: For an 8/20μs Current Waveform:
8μs = T_1 = Virtual Front Time
20μs = T_2 = Virtual Time to Half Value

FIGURE 2. PEAK PULSE CURRENT TEST WAVEFORM

Transient V-I Characteristics Curves

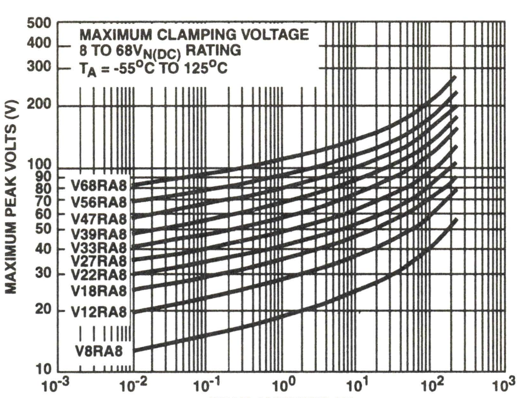


FIGURE 3. CLAMPING VOLTAGE FOR V8RA8 - V68RA8

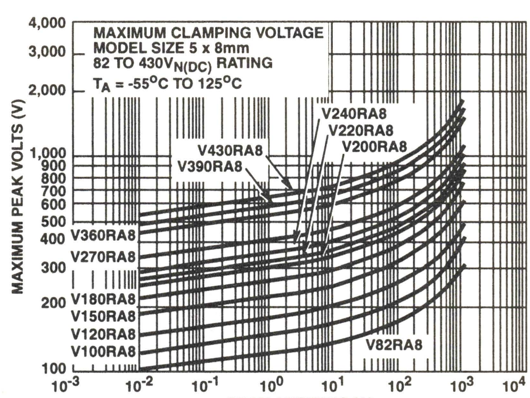


FIGURE 4. CLAMPING VOLTAGE FOR V82RA8 - V430RA8

Transient V-I Characteristics Curves (Continued)

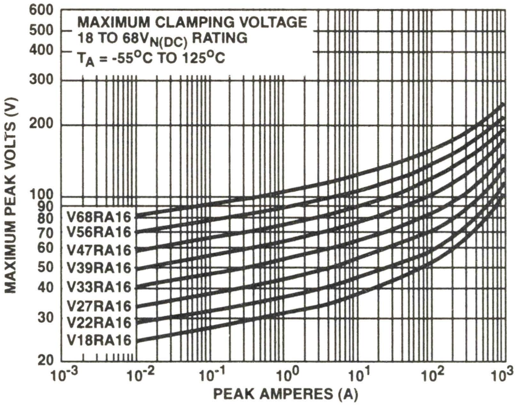


FIGURE 5. CLAMPING VOLTAGE FOR V18RA16 - V68RA16

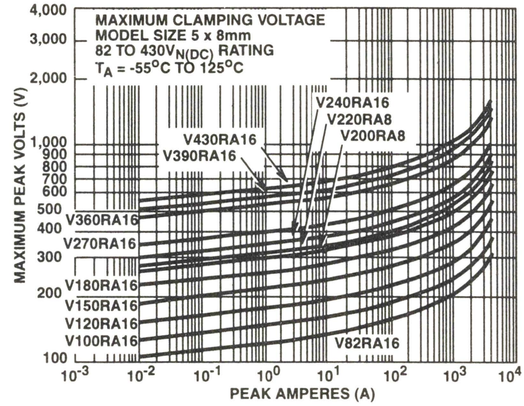


FIGURE 6. CLAMPING VOLTAGE FOR V82RA16 - V430RA16

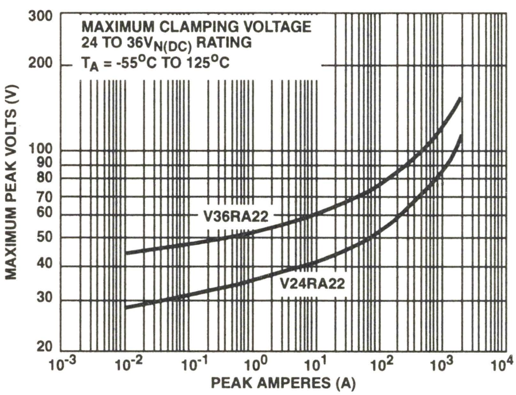


FIGURE 7. CLAMPING VOLTAGE FOR V24RA22 - V36RA22

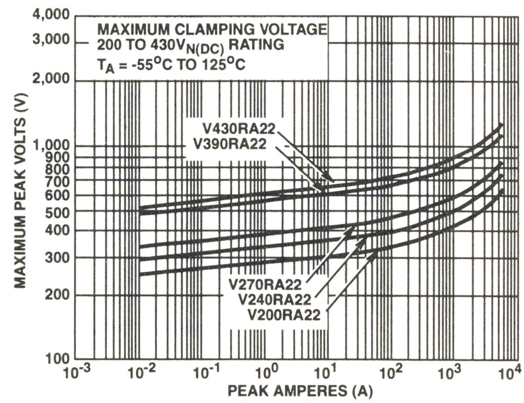


FIGURE 8. CLAMPING VOLTAGE FOR V200RA22 - V430RA22

Pulse Rating Curves

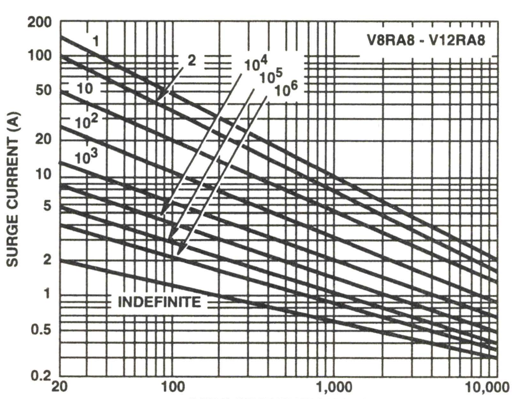


FIGURE 9. SURGE CURRENT RATING CURVES FOR V8RA8 - V12RA8

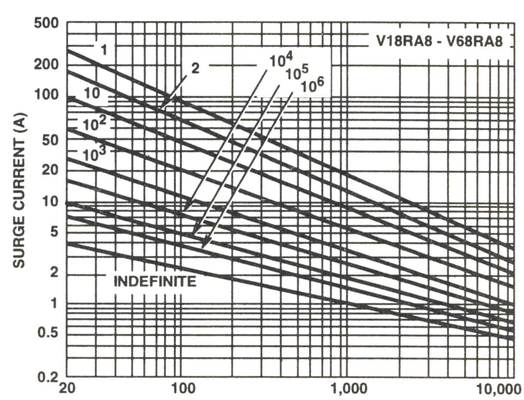


FIGURE 10. SURGE CURRENT RATING CURVES FOR V18RA8 - V68RA8

Pulse Rating Curves (Continued)

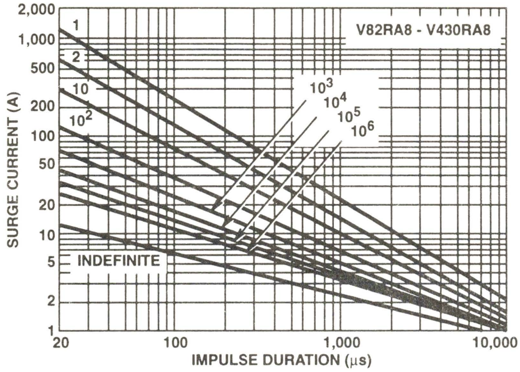


FIGURE 11. SURGE CURRENT RATING CURVES FOR V82RA8 - V430RA8

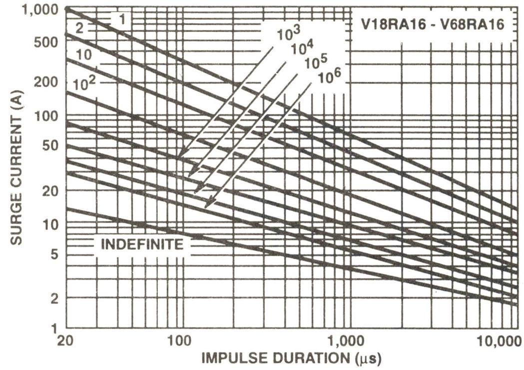


FIGURE 12. SURGE CURRENT RATING CURVES FOR V18RA16 - V68RA16

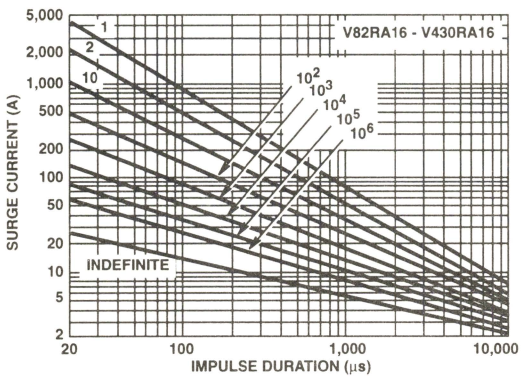


FIGURE 13. SURGE CURRENT RATING CURVES FOR V82RA16 - V430RA16

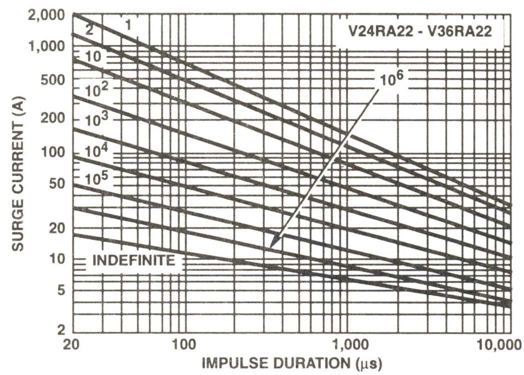


FIGURE 14. SURGE CURRENT RATING CURVES FOR V24RA22 - V36RA22

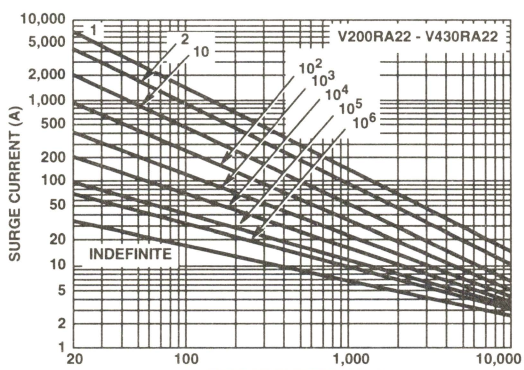


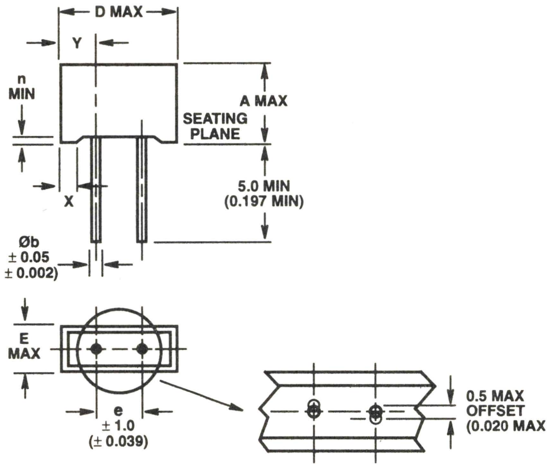
FIGURE 15. SURGE CURRENT RATING CURVES FOR V200RA22 - V430RA22

NOTE: If pulse ratings are exceeded, a shift of $V_{N(DC)}$ (at specified current) of more than ±10% could result. This type of shift, which normally results in a decrease of $V_{N(DC)}$, may result in the device not meeting the original published specifications, but it does not prevent the device from continuing to function, and to provide ample protection.

4

VARISTOR PRODUCTS

Mechanical Dimensions



SYMBOL	RA8 SERIES	RA16 SERIES	RA22 SERIES
A MAX	8.85 (0.348)	15.1 (0.594)	19.1 (0.752)
D MAX	11.45 (0.450)	19.7 (0.776)	25.5 (1.004)
e	5 (0.197)	7.5 (0.295)	7.5 (0.295)
E MAX	5.2 (0.205)	6.3 (0.248)	6.3 (0.248)
n MAX	0.7 (0.027)	0.7 (0.027)	0.7 (0.027)
Øb	0.635 (0.025)	0.81 (0.032)	0.81 (0.032)
WEIGHT TYP	1 Gram	3.4 Grams	4.4 Grams
X	2.2 (0.087)	2.2 (0.087)	4.4 (0.173)
Y	3.1 ± 0.5 (0.122 ± 0.02)	6 ± 1 (0.236 ± 0.04)	8.9 ± 1 (0.35 ± 0.04)

NOTES:

1. Dimensions in mm, dimensions in inches in parentheses.
2. Inches for reference only.

Ordering Information

The RA Series is supplied in bulk pack.

V 200 RA 16

- V — Harris Varistor Technology
- 200 — Nominal Varistor Voltage
- RA — Series Designator
- 16 — Relative Device Size Indicator

TVS 5

MULTILAYER PRODUCTS

Multilayer Products Overview

As with most electronic components, devices for Transient Voltage Suppression have evolved to meet specific customer needs and market demands. This is no more evident than with the Harris Multilayer Suppressor technology. This product family combines the required electrical performance with the leadless chip, surface mount package. These devices provide the designer with a means to ensure circuit reliability in a form factor necessary to meet the space constraints of today's densely packaged electronic products.

Multilayer Suppressors address a specific part of the transient voltage spectrum - the circuit board level environment where, although lower in energy, transients from ESD, inductive load switching, and even lightning surge remnants would otherwise reach sensitive integrated circuits. Each event can relate to a product's **E**lectro**M**agnetic **C**ompatibility (**EMC**), or its immunity to these transients that could cause damage or malfunction. The importance of EMC is evident as it is the subject of numerous recent international testing standards and legislation mandating compliance in many countries.

Harris offers three distinct versions of Multilayer Suppressors - The ML Series which supports the broadest application range, the MLE Series intended for ESD while providing filter functions, and the AUML Series characterized for the specific transients found in automotive electronic systems.

Market Segment examples for Multilayers are given in the table below and a number of pertinent Application Notes are provided in Section 11.

Transient Voltage Suppressor Device Selection Guide

MARKET SEGMENT	TYPICAL APPLICATIONS AND CIRCUITS EXAMPLES	DEVICE FAMILY OR SERIES	DATA BOOK SECTION	TECHNOLOGY	SURFACE MOUNT PRODUCT?
Low Voltage, Board Level Products	• Hand-Held/Portable Devices • EDP • Computer • I/O Port and Interfaces • Controllers • Instrumentation • Remote Sensors • Medical Electronics, etc.	CH	4	MOV	✔
		MA, ZA, RA	4	MOV	
		ML, MLE	**5**	**Multilayer Suppressor**	✔
		SP72X	6	SCR/Diode Array	✔ †
AC Line, TVSS Products	• UPS • AC Panels • AC Power Taps • TVSS Devices • AC Appliance/Controls • Power Meters • Power Supplies • Circuit Breakers • Consumer Electronics	UltraMOV™, "C" III, LA, HA, RA	4	MOV	
		CH	4	MOV	✔
		GDT	7	Gas Discharge Tube	
Automotive Electronics	• ABS • EEC • Instrument Cluster • Air Bag • Window Control • Wiper Modules • Multiplex Bus • EFI	CH	4	MOV	✔
		ZA	4	MOV	
		AUML, ML	**5**	**Multilayer Suppressor**	✔
		SP72X	6	SCR/Diode Array	✔ †
Telecommunications Products	• Cellular/Cordless Phone • Modems • Secondary Phone Line Protectors • Data Line Connectors • Repeaters • Line Cards	CH	4	MOV	✔
		CP, CS, ZA	4	MOV	
		ML, MLE	**5**	**Multilayer Suppressor**	✔
		SP72X	6	SCR/Diode Array	✔ †
		GDT	7	Gas Discharge Tube	
		Surgector	8	Thyristor/Zener	
Industrial, High Energy AC Products	• High Current Relays • Solenoids • Motor Drives • AC Distribution Panels • Robotics • Large Motors	DA/DB, BA/BB, CA, HA, NA, PA	4	MOV	
		GDT	7	Gas Discharge Tube	
Arrester Products	• Lightning Arrester Assemblies for High Voltage AC Power Distribution Lines and Utility Transformers	AS	9	MOV	

† Available in both surface mount and through-hole packages.

ML Series

Multilayer Surface Mount Transient Voltage Surge Suppressors

February 1998

Features

- Leadless 0603, 0805, 1206 and 1210 Chip Sizes
- Multilayer Ceramic Construction Technology
- -55°C to 125°C Operating Temperature Range
- Wide Operating Voltage Range $V_{M(DC)}$ = 3.5V to 120V
- Rated for Surge Current (8 x 20)
- Rated for Energy (10 x 1000)
- Inherent Bidirectional Clamping
- No Plastic or Epoxy Packaging Assures Better than 94V-0 Flammability Rating
- Standard Low Capacitance Types Available
- Available with Nickel/Tin End Terminations

Applications

- Suppression of Inductive Switching or Other Transient Events Such as EFT and Surge Voltage at the Circuit Board Level
- ESD Protection for Components Sensitive to IEC 1000-4-2, MIL-STD-883C Method 3015.7, and Other Industry Specifications (See Also the MLE Series)
- Provides On-Board Transient Voltage Protection for ICs and Transistors
- Used to Help Achieve Electromagnetic Compliance of End Products
- Replace Larger Surface Mount TVS Zeners in Many Applications

Description

The ML Series is a family of Transient Voltage Surge Suppression devices based on the Harris Multilayer fabrication technology. These components are designed to suppress a variety of transient events, including those specified by the IEC or other standards used for Electromagnetic Compliance (EMC). The ML Series is typically applied to protect integrated circuits and other components at the circuit board level.

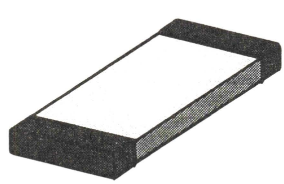
The wide operating voltage and energy range make the ML Series suitable for numerous applications on power supply, control and signal lines.

The ML Series is manufactured from semiconducting ceramics providing bidirectional voltage clamping and is supplied in leadless, surface mount form, compatible with modern reflow and wave soldering procedures.

Harris manufactures other Multilayer Series products. See the MLE Series data sheet (Harris AnswerFAX, 407-724-7800, doc #2463) for ESD applications. See the AUML Series for automotive applications (AnswerFAX doc #3387).

Packaging

ML SERIES (LEADLESS CHIP)



Absolute Maximum Ratings For ratings of individual members of a series, see device ratings and specifications table.

	ML SERIES	UNITS
Continuous:		
Steady State Applied Voltage:		
DC Voltage Range ($V_{M(DC)}$)	3.5 to 68	V
AC Voltage Range ($V_{M(AC)RMS}$)	2.5 to 50	V
Transient:		
Non-Repetitive Surge Current, 8/20μs Waveform, (I_{TM})	30 to 250	A
Non-Repetitive Surge Energy, 10/1000μs Waveform, (W_{TM})	0.1 to 1.2	J
Operating Ambient Temperature Range (T_A)	-55 to 125	^oC
Storage Temperature Range (T_{STG})	-55 to 150	^oC
Temperature Coefficient (αV) of Clamping Voltage (V_C) at Specified Test Current	<0.01	%/^oC

Device Ratings and Specifications

PART NUMBER	MAXIMUM RATINGS (125°C)					SPECIFICATIONS (25°C)		
	MAXIMUM CONTINUOUS WORKING VOLTAGE		MAXIMUM NON-REPETITIVE SURGE CURRENT (8/20μs)	MAXIMUM NON-REPETITIVE SURGE ENERGY (10/1000μs)	MAXIMUM CLAMPING VOLTAGE AT 10A (OR AS NOTED) (8/20μs)	NOMINAL VOLTAGE AT 1mA DC TEST CURRENT		TYPICAL CAPACITANCE AT f = 1MHz
	$V_{M(DC)}$	$V_{M(AC)}$	I_{TM}	W_{TM}	V_C	$V_{N(DC)}$ MIN	$V_{N(DC)}$ MAX	C
	(V)	(V)	(A)	(J)	(V)	(V)	(V)	(pF)
V3.5MLA0603	3.5	2.5	30	0.1	10 at 2A	3.7	7.0	1100
V3.5MLA0805	3.5	2.5	120	0.3	10 at 5A	3.7	7.0	2200
V3.5MLA0805L	3.5	2.5	40	0.1	10 at 2A	3.7	7.0	1200
V3.5MLA1206	3.5	2.5	100	0.3	14	3.7	7.0	6000
V5.5MLA0603	5.5	4.0	30	0.1	15.5 at 2A	7.1	9.3	660
V5.5MLA0805	5.5	4.0	120	0.3	15.5 at 5A	7.1	9.3	1600
V5.5MLA0805L	5.5	4.0	40	0.1	15.5 at 2A	7.1	9.3	860
V5.5MLA1206	5.5	4.0	150	0.4	15.5	7.1	9.3	4500
V9MLA0603	9.0	6.5	30	0.1	23 at 2A	11.0	16.0	420
V9MLA0805L	9.0	6.5	40	0.1	20 at 2A	11	14	450
V12MLA0805L	12	9.0	40	0.1	25 at 2A	14	18.5	350
V14MLA0603	14	10	30	0.1	30 at 2A	15.9	20.3	150
V14MLA0805	14	10	120	0.3	30 at 5A	15.9	20.3	480
V14MLA0805L	14	10	40	0.1	30 at 2A	15.9	20.3	270
V14MLA1206	14	10	150	0.4	30	15.9	20.3	1600

Device Ratings and Specifications (Continued)

PART NUMBER	MAXIMUM RATINGS (125°C)					SPECIFICATIONS (25°C)		
	MAXIMUM CONTINUOUS WORKING VOLTAGE		MAXIMUM NON-REPETITIVE SURGE CURRENT (8/20µs)	MAXIMUM NON-REPETITIVE SURGE ENERGY (10/1000µs)	MAXIMUM CLAMPING VOLTAGE AT 10A (OR AS NOTED) (8/20µs)	NOMINAL VOLTAGE AT 1mA DC TEST CURRENT		TYPICAL CAPACITANCE AT f = 1MHz
	$V_{M(DC)}$	$V_{M(AC)}$	I_{TM}	W_{TM}	V_C	$V_{N(DC)}$ MIN	$V_{N(DC)}$ MAX	C
	(V)	(V)	(A)	(J)	(V)	(V)	(V)	(pF)
V18MLA0603	18	14	30	0.1	40 at 2A	22	28.0	125
V18MLA0805	18	14	120	0.3	40 at 5A	22	28.0	450
V18MLA0805L	18	14	40	0.1	40 at 2A	22	28.0	250
V18MLA1206	18	14	150	0.4	40	22	28.0	1100
V18MLA1210	18	14	500	2.5	40	22	28.0	1250
V26MLA0603	26	20	30	0.1	58 at 2A	31	38	90
V26MLA0805	26	20	100	0.3	58 at 5A	29.5	38.5	190
V26MLA0805L	26	20	40	0.1	58 at 2A	29.5	38.5	115
V26MLA1206	26	20	150	0.6	56	29.5	38.5	900
V26MLA1210	26	20	300	1.2	54	29.5	38.5	1000
V30MLA0603	30	25	30	0.1	65 at 2A	37	46	75
V30MLA0805L	30	25	30	0.1	65 at 2A	37	46	80
V30MLA1210	30	25	280	1.2	62	35	43	1575
V30MLA1210L	30	25	220	0.9	62	35	43	1530
V33MLA1206	33	26	180	0.8	72	38	49	550
V42MLA1206	42	30	180	0.8	86	46	60	550
V48MLA1210	48	40	250	1.2	100	54.5	66.5	450
V48MLA1210L	48	40	220	0.9	100	54.5	66.5	430
V56MLA1206	56	40	180	1.0	110	61	77	150
V60MLA1210	60	50	250	1.5	120	67	83	375
V68MLA1206	68	50	180	1.0	130	76	90	150
V85MLA1210	85	67	250	2.5	160	95	115	225
V120MLA1210	120	107	125	2.0	230	135	165	65

NOTES:

1. L suffix is a low capacitance and energy version. Contact Sales for custom capacitance requirements.
2. Typical leakage at 25°C < 25µA, maximum leakage 50µA at $V_{M(DC)}$.
3. Average power dissipation of transients for 0603, 0805, 1206 and 1210 sizes not to exceed 0.05, 0.10W, 0.10W and 0.15W, respectively.

Power Dissipation Ratings

When transients occur in rapid succession the average power dissipation is the energy (watt-seconds) per pulse times the number of pulses per second. The power so developed must be within the specifications shown on the Device Ratings and Characteristics table for the specific device. Certain parameter ratings must be derated at high temperatures as shown in Figure 1.

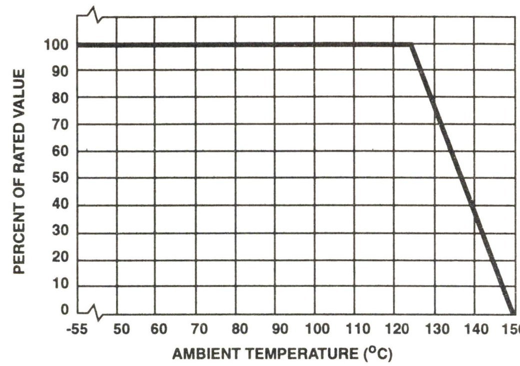
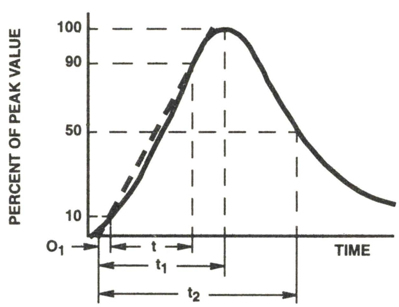


FIGURE 1. CURRENT, ENERGY AND POWER DERATING CURVE



O_1 = VIRTUAL ORIGIN OF WAVE
t = TIME FROM 10% TO 90% OF PEAK
t_1 = VIRTUAL FRONT TIME = 1.25 x t
t_2 = VIRTUAL TIME TO HALF VALUE (IMPULSE DURATION)

EXAMPLE:
FOR AN 8/20μs CURRENT WAVEFORM:
8μs = t_1 = VIRTUAL FRONT TIME
20μs = t_2 = VIRTUAL TIME TO HALF VALUE

FIGURE 2. PEAK PULSE CURRENT TEST WAVEFORM

Maximum Transient V-I Characteristic Curves

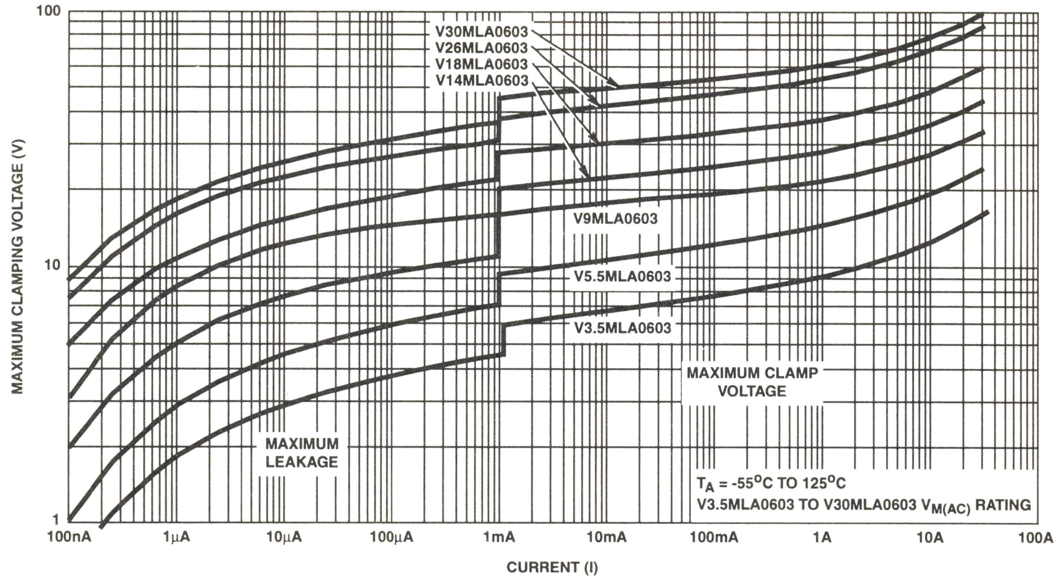


FIGURE 3. V3.5MLA0603 TO V30MLA0603 MAXIMUM V-I CHARACTERISTIC CURVES

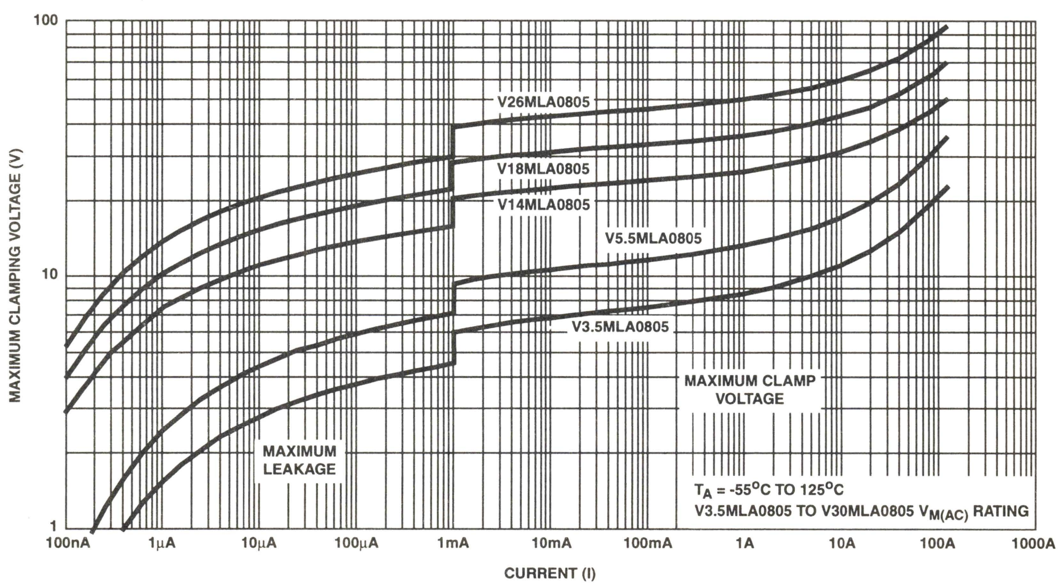


FIGURE 4. V3.5MLA0805 TO V26MLA0805 MAXIMUM V-I CHARACTERISTIC CURVES

Maximum Transient V-I Characteristic Curves (Continued)

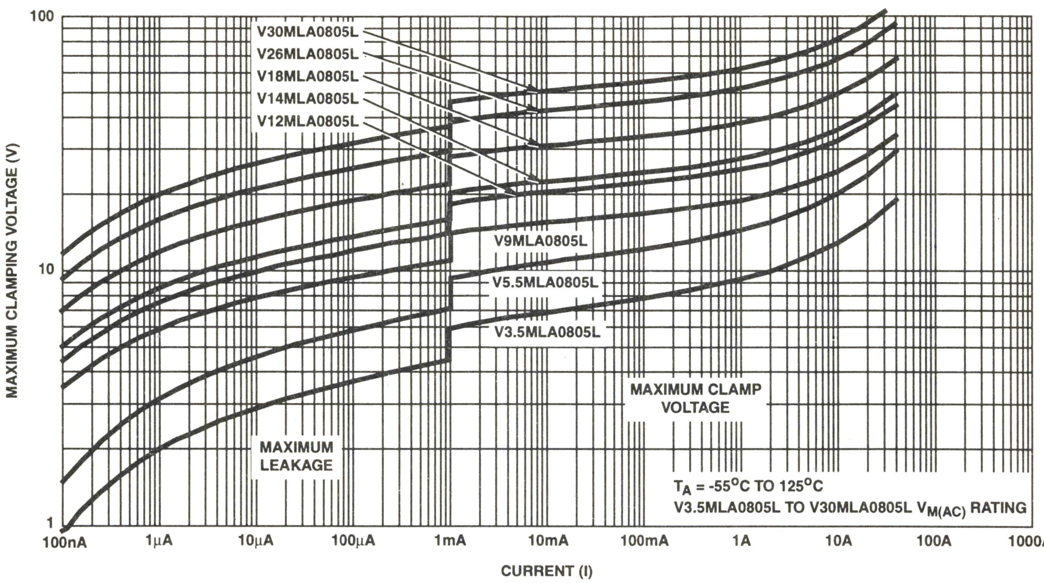


FIGURE 5. V3.5MLA0805L TO V30MLA0805L MAXIMUM V-I CHARACTERISTIC CURVES

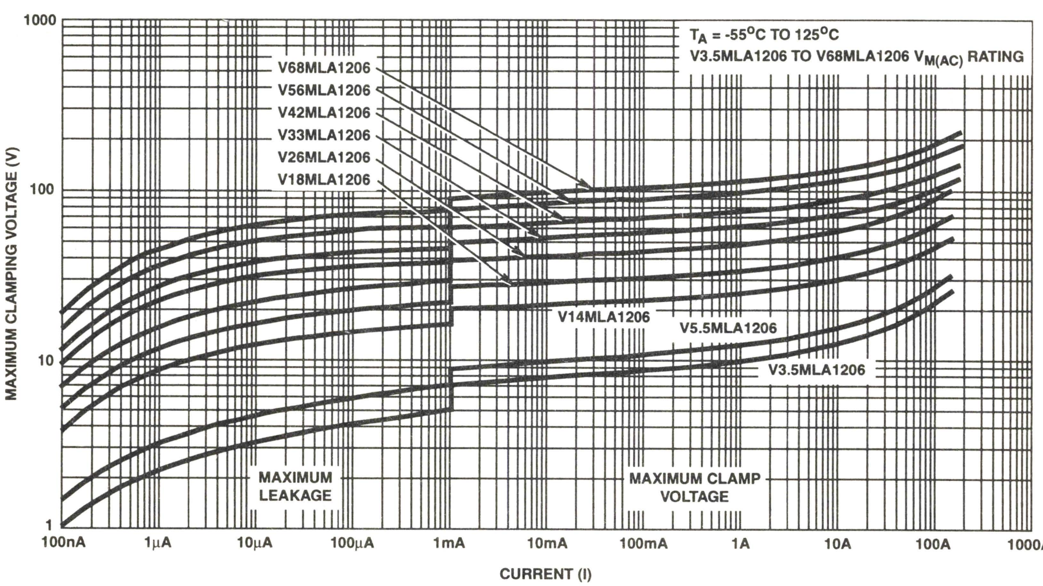


FIGURE 6. V3.5MLA1206 TO V68MLA1206 MAXIMUM V-I CHARACTERISTIC CURVES

Maximum Transient V-I Characteristic Curves (Continued)

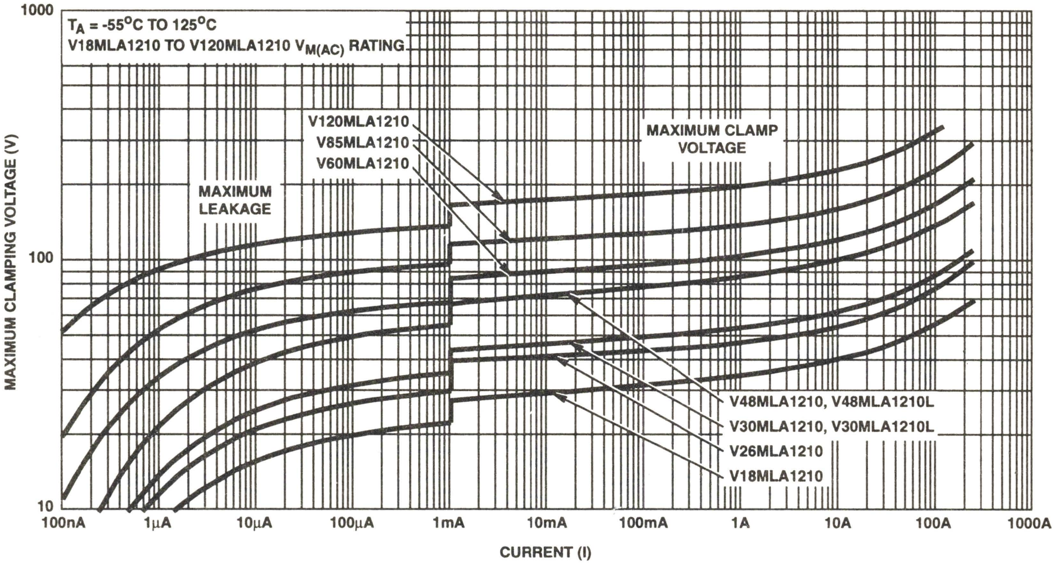


FIGURE 7. V18MLA1210 TO V120MLA1210 MAXIMUM V-I CHARACTERISTIC CURVES

Device Characteristics

At low current levels, the V-I curve of the multilayer transient voltage suppressor approaches a linear (ohmic) relationship and shows a temperature dependent affect (Figure 8). At or below the maximum working voltage, the suppressor is in a high resistance mode (approaching $10^6\Omega$ at its maximum rated working voltage). Leakage currents at maximum rated voltage are below 50μA, typically 25μA.

When clamping transients at and above the 10mA range, the multilayer suppressor approaches a 1Ω -10Ω characteristic. Here, the multilayer becomes virtually temperature independent (Figure 9).

Speed of Response

The Multilayer Suppressor is a leadless device. Its response time is not limited by the parasitic lead inductances found in other surface mount packaging. The response time of the Zinc Oxide dielectric material is less than 1 nanosecond and the ML can clamp very fast dV/dT events such as ESD. Additionally, in "real world" applications, the associated circuit wiring is often the greatest factor effecting speed of response. Therefore, transient suppressor placement within a circuit can be considered important in certain instances.

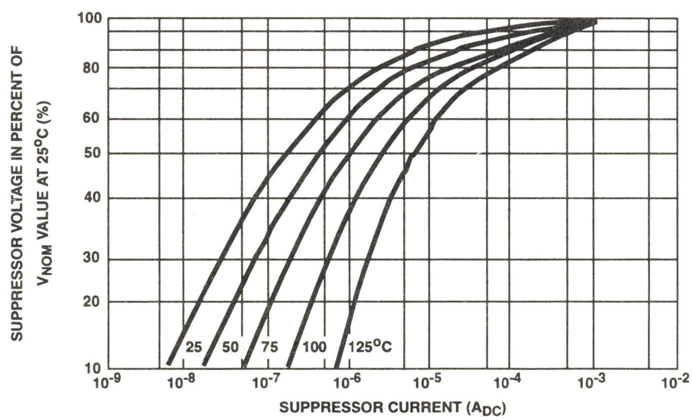


FIGURE 8. TYPICAL TEMPERATURE DEPENDENCE OF THE CHARACTERISTIC CURVE IN THE LEAKAGE REGION

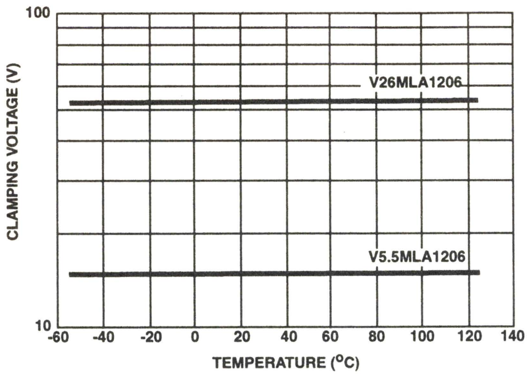


FIGURE 9. CLAMPING VOLTAGE OVER TEMPERATURE (V_C AT 10A)

Energy Absorption/Peak Current Capability

Energy dissipated within the ML is calculated by multiplying the clamping voltage, transient current and transient duration. An important advantage of the multilayer is its interdigitated electrode construction within the mass of dielectric material. This results in excellent current distribution and the peak temperature per energy absorbed is very low. The matrix of semiconducting grains combine to absorb and distribute transient energy (heat) (Figure 10). This dramatically reduces peak temperature, thermal stresses and enhances device reliability.

As a measure of the device capability in energy handling and peak current, the V26MLA1206A part was tested with multiple pulses at its peak current rating (150A, 8/20µs). At the end of the test, 10,000 pulses later, the device voltage characteristics are still well within specification (Figure 11).

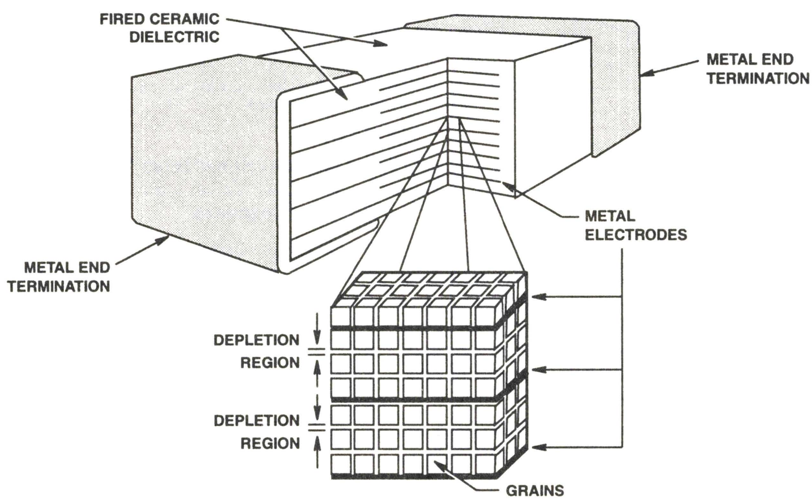


FIGURE 10. MULTILAYER INTERNAL CONSTRUCTION

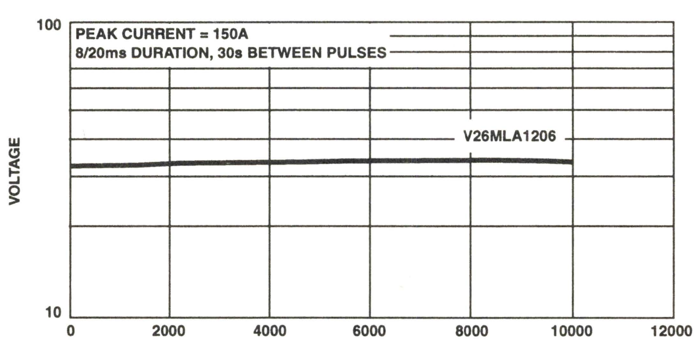


FIGURE 11. REPETITIVE PULSE CAPABILITY

Soldering Recommendations

The principal techniques used for the soldering of components in surface mount technology are Infra Red (IR) Reflow, Vapor Phase Reflow and Wave Soldering. When wave soldering, the ML suppressor is attached to the substrate by means of an adhesive. The assembly is then placed on a conveyor and run through the soldering process. With IR and Vapor Phase Reflow the device is placed in a solder paste on the substrate. As the solder paste is heated it reflows, and solders the unit to the board.

With the ML suppressor, the recommended solder is a 62/36/2 (Sn/Pb/Ag), 60/40 (Sn/Pb), or 63/37 (Sn/Pb). Harris also recommends an RMA solder flux. Wave soldering operation is the most strenuous of the processes. To avoid the possibility of generating stresses due to thermal shock, a preheat stage in the soldering process is recommended, and the peak temperature of the solder process should be rigidly controlled.

When using a reflow process, care should be taken to ensure that the ML chip is not subjected to a thermal gradient steeper than 4 degrees per second; the ideal gradient being 2 degrees per second. During the soldering process, preheating to within 100 degrees of the solders peak temperature is essential to minimize thermal shock. Examples of the soldering conditions for the ML series of suppressors are given in the tables below.

Once the soldering process has been completed, it is still necessary to ensure that any further thermal shocks are avoided. One possible cause of thermal shock is hot printed circuit boards being removed from the solder process and subjected to cleaning solvents at room temperature. The boards must be allowed to cool to less than 50°C before cleaning.

Termination Options

Harris offers three types of termination finish on the Multilayer product series:

1. Silver/Platinum (standard)
2. Silver/Palladium (optional)
3. Nickel/Tin (optional)

(The ordering information section describes how to designate them.)

The Nickel/Tin plated termination can provide certain solder process application benefits such as:

- A better match to Tin/Lead solders resulting in improved solder wetting and solder fillet height (typically 70% of component height).
- An enhanced resistance to solder leaching permits greater flexibility/latitude in the design and control of solder processes. (See the temperature-time graph below.)
- An alternative material when silver end terminations are restricted.

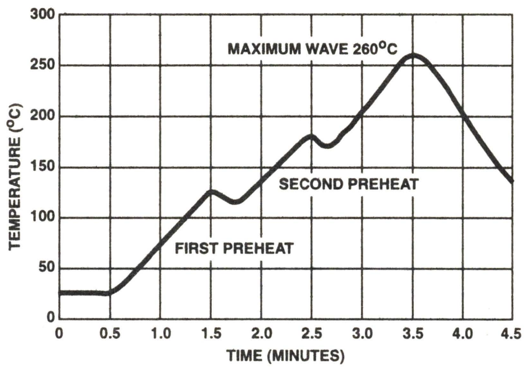


FIGURE 12. WAVE SOLDER PROFILE

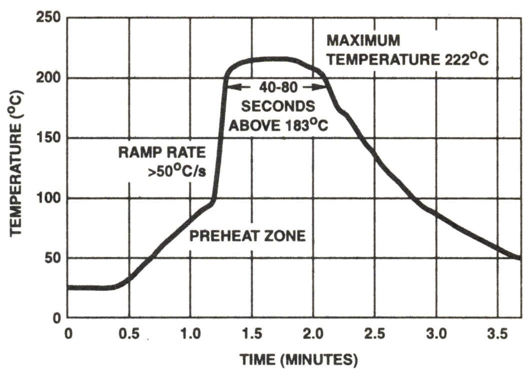


FIGURE 13. VAPOR PHASE SOLDER PROFILE

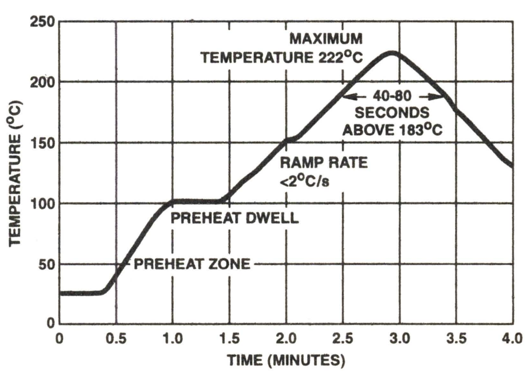


FIGURE 14. REFLOW SOLDER PROFILE

Solder Process Time Advantages for Nickel/Tin Terminated Multilayer Suppressors

Certain surface mount soldering processes require long duration or multiple soldering cycles for top and bottom side assemblies and/or for reworking rejected product. In these instances, devices with a Nickel/Tin finish offer greater dwell time, for example, when end termination leaching is of concern. The Solder Temperature-Time Curve shown can be used as a guideline when designing process variables and rework operations and illustrates the greater latitude afforded with this material.

Since end termination leaching is a function of the cumulative molten dwell time, then the molten time duration allowed at subsequent operations is reduced by the percentage of time used by the initial operation. Using the curve for the applicable material,

$$\frac{\text{Total Time at Initial Temp - Actual Time at Initial Temp}}{\text{Total Time at Initial Temp}}$$

$$\times \text{Total Time Permitted at the Subsequent Temp}$$

For example, if the initial process is for 20 seconds at 220°C and the next process is at 260°C, then the maximum time allowed at 260°C is:

For Nickel/Tin Termination:

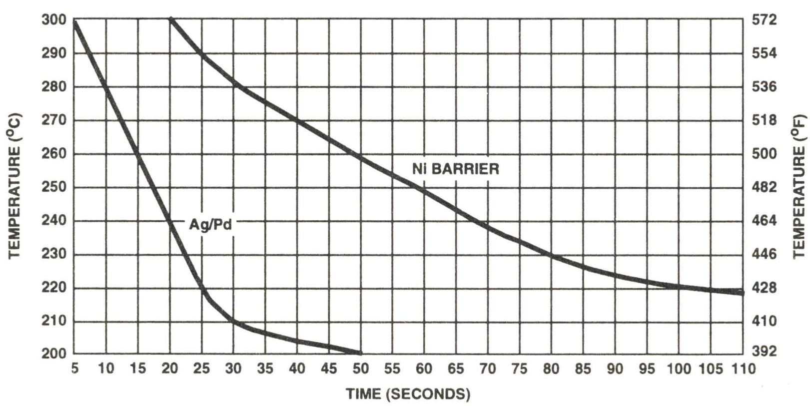
$$\frac{100-20}{100} \times 48 = 38.4 \text{ seconds}$$

For Ag/Pd Termination:

$$\frac{25-20}{25} \times 15 = 3.0 \text{ seconds}$$

Also, if the initial soldering process is for 10 seconds at 280°C, the Nickel/Tin termination can withstand a further 20 seconds at 280°C or an equivalent percentage of time at a subsequent temperature. For example, If the next soldering process is at 230°C, the total time allowed at this temperature is:

$$\frac{30-10}{30} \times 80 = 53 \text{ seconds}$$

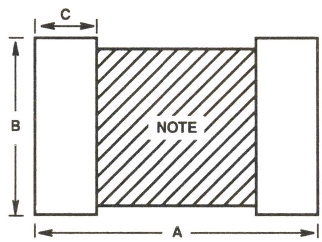


NOTES:

4. Comparative Temperature-Time data for Silver/Palladium and Nickel/Tin terminated Multilayer Suppressors.
5. The curves indicate the point at which 5% leaching of the termination will occur after immersion in a static solder bath for an 0805 size device.
6. Static solder bath = Sn/Pb (63/67). RMA no clean flux.

FIGURE 15. SOLDER TEMPERATURE-TIME CURVE

Recommended Pad Outline



NOTE: Avoid metal runs in this area.

SYMBOL	PAD SIZE							
	FOR 1210 SIZE DEVICE		FOR 1206 SIZE DEVICE		FOR 0805 SIZE DEVICE		FOR 0603 SIZE DEVICE	
	IN	MM	IN	MM	IN	MM	IN	MM
A	0.219	5.53	0.203	5.15	0.144	3.65	0.11	2.8
B	0.147	3.73	0.103	2.62	0.084	2.13	0.064	1.62
C	0.073	1.85	0.065	1.65	0.058	1.48	0.044	1.12

Explanation of Terms

Rated DC Voltage ($V_{M(DC)}$)

This is the maximum continuous DC voltage which may be applied up to the maximum operating temperature of the device. The rated DC operating voltage (working voltage) is also used as the reference point for leakage current. This voltage is always less than the breakdown voltage of the device.

Rated AC Voltage ($V_{M(AC)RMS}$)

This is the maximum continuous sinusoidal rms voltage which may be applied. This voltage may be applied at any temperature up to the maximum operating temperature of the device.

Maximum Non-Repetitive Surge Current (I_{TM})

This is the maximum peak current which may be applied for an 8/20µs impulse, with rated line voltage also applied, without causing device failure. The pulse can be applied to the device in either polarity with the same confidence factor. See Figure 2 for waveform description.

Maximum Non-Repetitive Surge Energy (W_{TM})

This is the maximum rated transient energy which may be dissipated for a single current pulse at a specified impulse duration (10/1000µs), with the rated DC or RMS voltage applied, without causing device failure.

Leakage (I_L) at Rated DC Voltage

In the nonconducting mode, the device is at a very high impedance (approaching $10^6\Omega$ at its maximum rated voltage) and appears essentially as an open circuit in the system. The leakage current drawn at this level is very low, as specified in the Device Ratings table.

Nominal Voltage ($V_{N(DC)}$)

This is the voltage at which the device changes from the off (standby state) to the on (clamping state) and enters its conduction mode of operation. The voltage value is usually characterized at the 1mA point and has a specified minimum and maximum voltage range.

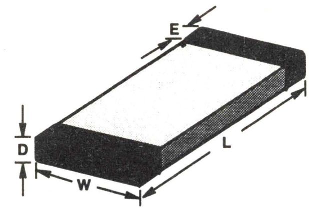
Clamping Voltage (V_C)

This is the peak voltage appearing across the suppressor when measured at conditions of specified pulse current and specified waveform.

Capacitance (C)

This is the capacitance of the device at a specified frequency (1MHz) and bias ($1V_{P-P}$)

Mechanical Dimensions

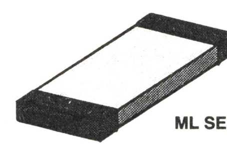


SYMBOL	CHIP SIZE							
	1210		1206		0805		0603	
	IN	MM	IN	MM	IN	MM	IN	MM
D Max.	0.113	2.87	0.071	1.80	0.043	1.1	0.035	0.9
E	0.02 ±0.01	0.50 ±0.25	0.02 ±0.01	0.50 ±0.25	0.01 to 0.029	0.25 to 0.75	0.015 ±0.008	0.4 ±0.2
L	0.125 ±0.012	3.20 ±0.30	0.125 ±0.012	3.20 ±0.03	0.079 ±0.008	2.01 ±0.2	0.063 ±0.006	1.6 ±0.15
W	0.10 ±0.012	2.54 ±0.30	0.06 ±0.011	1.60 ±0.28	0.049 ±0.008	1.25 ±0.2	0.032 ±0.006	0.8 ±0.15

Ordering Information

VXXML TYPES

V 18 ML X 1206 X X X



DEVICE FAMILY
Harris TVSS Device

MAXIMUM DC WORKING VOLTAGE

MULTILAYER DESIGNATOR

PERFORMANCE DESIGNATOR
A: Standard
E: ESD (See MLE Data Sheet)

DEVICE SIZE:
i.e., 120 mil x 60 mil

CAPACITANCE OPTION
No Letter: Standard
L: Low Capacitance Version (Where available - see device ratings for standard versions)

END TERMINATION OPTION
No Letter: Ag/P_t (Standard)
W: Ag/P_d
N: Ni/Sn

PACKING OPTIONS
A: <100 pc Bulk Pak
H: 7in (178mm) Diameter Reel (Note)
T: 13in (330mm) Diameter Reel (Note)

NOTE: See quantity table.

Standard Shipping Quantities

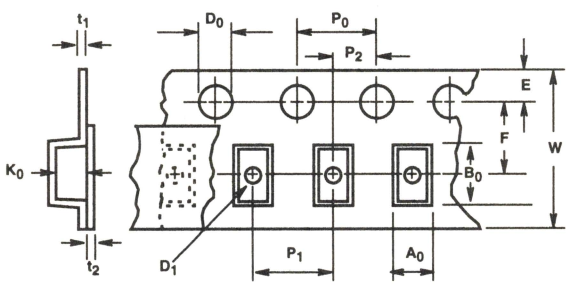
DEVICE SIZE	"13" INCH REEL ("T" OPTION)	"7" INCH REEL ("H" OPTION)	BULK PACK ("A" OPTION)
1210	8,000	2,000	100
1206	10,000	2,500	100
0805	10,000	2,500	100
0603	10,000	2,500	100

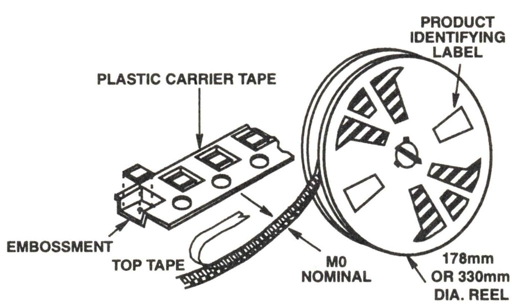
Tape and Reel Specifications

- **Conforms to EIA - 481, Revision A**
- **Can be Supplied to IEC Publication 286 - 3**

SYMBOL	DESCRIPTION	MILLIMETERS
A_0	Width of Cavity	Dependent on Chip Size to Minimize Rotation.
B_0	Length of Cavity	Dependent on Chip Size to Minimize Rotation.
K_0	Depth of Cavity	Dependent on Chip Size to Minimize Rotation.
W	Width of Tape	8 ±0.2
F	Distance Between Drive Hole Centers and Cavity Centers	3.5 ±0.5
E	Distance Between Drive Hole Centers and Tape Edge	1.75 ±0.1
P_1	Distance Between Cavity Center	4 ±0.1
P_2	Axial Distance Between Drive Hole Centers and Cavity Centers	2 ±0.1
P_0	Axial Distance Between Drive Hole Centers	4 ±0.1
D_0	Drive Hole Diameter	1.55 ±0.05
D_1	Diameter of Cavity Piercing	1.05 ±0.05
t_1	Embossed Tape Thickness	0.3 max
t_2	Top Tape Thickness	0.1 max

NOTE: Dimensions in millimeters.





5

MULTILAYER PRODUCTS

HARRIS SEMICONDUCTOR

MLE Series

Multilayer Surface Mount ESD Suppressor/Filter

January 1998

Features

- Rated for ESD (IEC-1000-4-2)
- Characterized for Impedance and Capacitance
- -55^{o}C to 125^{o}C Operating Temperature Range
- Leadless 0603, 0805, and 1206 Chip Sizes
- Operating Voltage up to 18$V_{M(DC)}$
- Multilayer Ceramic Construction Technology
- Available with Nickel/Tin End Terminations

Applications

- Protection of Components and Circuits Sensitive to ESD Transients Occurring on Power Supply, Control and Signal Lines
- Suppression of ESD Events Such as Specified in IEC-1000-4-2 or MIL-STD-883C Method-3015.7, for Electromagnetic Compliance (EMC)
- Used in Mobile Communications, Computer/EDP Products, Medical Products, Hand Held/Portable Devices, Industrial Equipment, Including Diagnostic Port Protection and I/O Interfaces

Description

The MLE Series is a family of Transient Voltage Suppression devices based on the Harris Multilayer fabrication technology. These components are designed to suppress ESD events, including those specified in IEC1000-4-2 or other standards used for Electromagnetic Compliance testing. The MLE Series is typically applied to protect integrated circuits and other components at the circuit board level operating at 18VDC, or less.

Additionally, the fabrication method and materials of these devices result in capacitance characteristics suitable for high frequency attenuation/low-pass filter circuit functions, thereby, providing suppression and filtering in a single device.

The MLE Series is manufactured from semiconducting ceramics, providing bidirectional voltage clamping and is supplied in leadless, surface mount form compatible with modern reflow and wave soldering procedures.

Harris manufactures other Multilayer Series products. See the ML Series data sheet (Harris AnswerFAX, 407-724-7800, doc. #2461) for higher energy/peak current transient applications. See the AUML Series for automotive applications (AnswerFAX doc. #3387).

Packaging

MLE SERIES (LEADLESS CHIP)

Absolute Maximum Ratings For ratings of individual members of a series, see device ratings and specifications table.

	MLE SERIES	UNITS
Continuous:		
Steady State Applied Voltage:		
DC Voltage Range ($V_{M(DC)}$)	≤18	V
Operating Ambient Temperature Range (T_A)	-55 to 125	^oC
Storage Temperature Range (T_{STG})	-55 to 150	^oC

Device Ratings and Specifications

PART NUMBER	MAX CONTINUOUS WORKING VOLTAGE -55°C TO 125°C (NOTE 1) $V_{M(DC)}$ (V)	NOMINAL VOLTAGE V_{NOM} AT 1mA DC MIN (V)	MAX (V)	PERFORMANCE SPECIFICATIONS (25°C) (NOTE 2) TYPICAL ESD CLAMP VOLTAGE (8kV CONTACT NOTE 3) PEAK (V)	(15kV AIR NOTE 4) PEAK (V)	(NOTE 5) TYPICAL CAPACITANCE AT 1MHz (pF)	MAXIMUM LEAKAGE $I_{L\ MAX}$ (μA)	AT APPLIED VOLTAGE V_{DC}
V18MLE0603	18	22	28	<140	<85	<100	0.1	3.5
							0.3	5.5
							5.0	15
							25	18
V18MLE0805	18	22	28	<95	<75	<500	0.2	3.5
							0.5	5.5
							5.0	15
							25	18
V18MLE1206	18	22	28	<75	<65	<1700	0.5	3.5
							1.0	5.5
							5.0	15
							25	18

NOTES:

1. For applications of $18V_{DC}$ or less. Higher voltages available, contact Sales.
2. Tested with IEC-1000-4-2 Human Body Model (HBM) discharge test circuit.
3. Direct discharge to device terminals (IEC preferred test method).
4. Corona discharge through air (represents actual ESD event).
5. Capacitance may be customized, contact Sales.

Typical Performance Curves

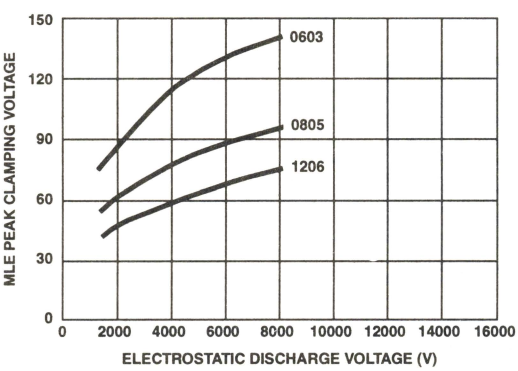


FIGURE 1. CLAMPING CHARACTERISTIC FOR CONTACT METHOD ESD PER IEC-1000-4-2, RANGE 0.5kV TO 8.0kV

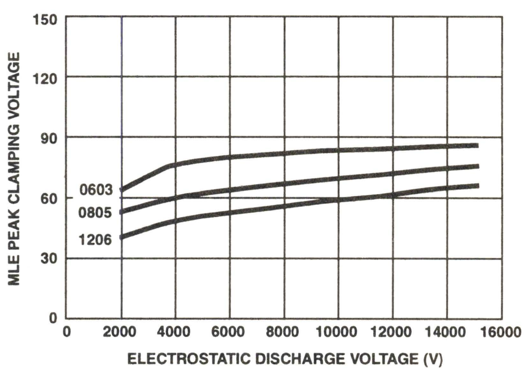


FIGURE 2. CLAMPING CHARACTERISTIC FOR AIR DISCHARGE METHOD ESD PER IEC1000-4-2, RANGE 2kV TO 15kV

Typical Performance Curves (Continued)

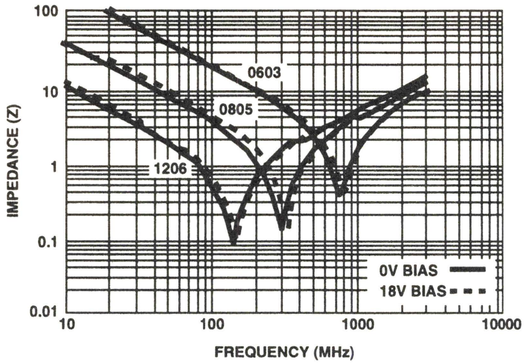


FIGURE 3. IMPEDANCE (Z) vs FREQUENCY TYPICAL CHARACTERISTIC WITH 0V AND 18V_{DC} BIAS

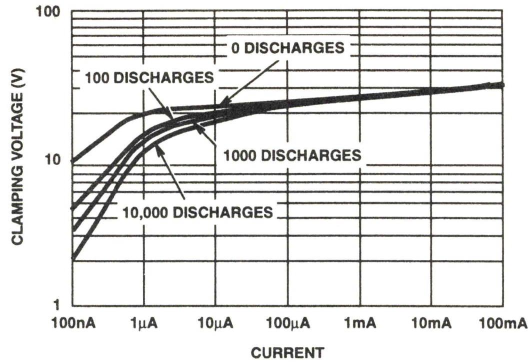


FIGURE 4. V18MLE0805 LEAKAGE CHARACTERISTIC STABILITY AFTER 10,000 x 8kV CONTACT ESD IMPULSES

NOTE: Figure 4 is an example of device clamping characteristics in the Standby (or "Leakage") current region of operation. It is intended to illustrate the stability of the device after the application of multiple, 8kV ESD CONTACT discharges per IEC 1000-4-2. Note that the discharges were applied in one polarity only and the measurements were made in that same polarity.

Multilayer Internal Construction

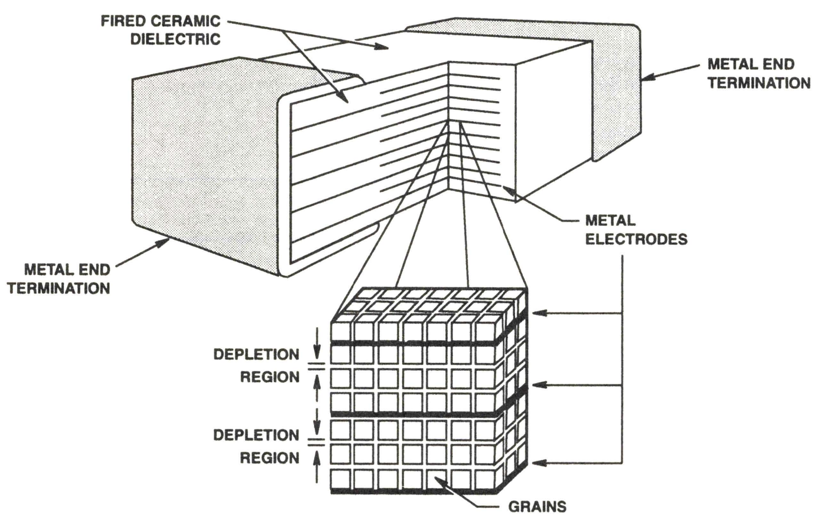


FIGURE 5. DIAGRAM OF INTERDIGITATED METAL ELECTRODES WITHIN THE CERAMIC DIELECTRIC MATERIAL AND REPRESENTATION OF GRAIN STRUCTURE WITHIN EACH LAYER

Soldering Recommendations

The principal techniques used for the soldering of components in surface mount technology are Infra Red (IR) Reflow, Vapour Phase Reflow, and Wave Soldering. When wave soldering, the MLE suppressor is attached to the circuit board by means of an adhesive. The assembly is then placed on a conveyor and run through the soldering process to contact the wave. With IR and Vapour Phase Reflow, the device is placed in a solder paste on the substrate. As the solder paste is heated, it reflows and solders the unit to the board.

With the MLE suppressor, the recommended solder is a 62/36/2 (Sn/Pb/Ag), 60/40 (Sn/Pb), or 63/37 (Sn/Pb). Harris also recommends an RMA solder flux.

Wave soldering is the most strenuous of the processes. To avoid the possibility of generating stresses due to thermal shock, a preheat stage in the soldering process is recommended, and the peak temperature of the solder process should be rigidly controlled.

When using a reflow process, care should be taken to ensure that the MLE chip is not subjected to a thermal gradient steeper than 4 degrees per second; the ideal gradient being 2 degrees per second. During the soldering process, preheating to within 100 degrees of the solders peak temperature is essential to minimize thermal shock. Examples of the soldering conditions for the MLE series of suppressors are given in the tables below.

Once the soldering process has been completed, it is still necessary to ensure that any further thermal shocks are avoided. One possible cause of thermal shock is hot printed circuit boards being removed from the solder process and subjected to cleaning solvents at room temperature. The boards must be allowed to gradually cool to less than 50°C before cleaning.

Termination Options

Harris offers three types of termination finish on the Multilayer product series:

1. Silver/Platinum (standard)
2. Silver/Palladium (optional)
3. Nickel/Tin (optional)

(The ordering information section describes how to designate them.)

The Nickel/Tin plated termination can provide certain solder process application benefits such as:

- A better match to Tin/Lead solders resulting in improved solder wetting and solder fillet height (typically 70% of component height).
- An enhanced resistance to solder leaching permits greater flexibility/latitude in the design and control of solder processes. (See the temperature-time graph below.)
- An alternative material when silver end terminations are restricted.

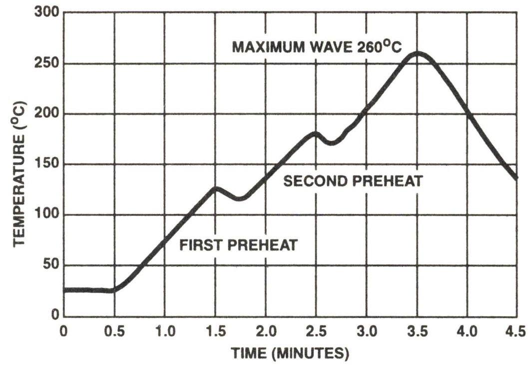


FIGURE 6. WAVE SOLDER PROFILE

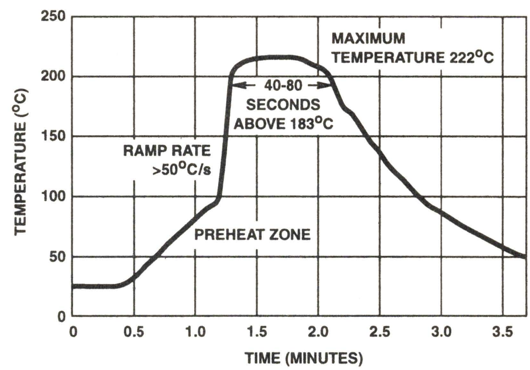


FIGURE 7. VAPOR PHASE SOLDER PROFILE

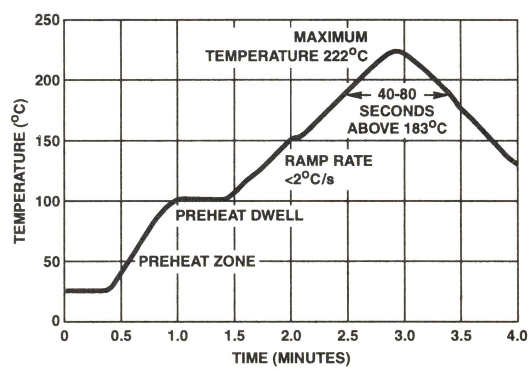


FIGURE 8. REFLOW SOLDER PROFILE

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MULTILAYER PRODUCTS

Solder Process Time Advantages for Nickel/Tin Terminated Multilayer Suppressors

Certain surface mount soldering processes require long duration or multiple soldering cycles for top and bottom side assemblies and/or for reworking rejected product. In these instances, devices with a Nickel/Tin finish offer greater dwell time, for example, when end termination leaching is of concern. The Solder Temperature-Time Curve shown can be used as a guideline when designing process variables and rework operations and illustrates the greater latitude afforded with this material.

Since end termination leaching is a function of the cumulative molten dwell time, then the molten time duration allowed at subsequent operations is reduced by the percentage of time used by the initial operation. Using the curve for the applicable material,

$$\frac{\text{Total Time at Initial Temp - Actual Time at Initial Temp}}{\text{Total Time at Initial Temp}} \times \text{Total Time Permitted at the Subsequent Temp}$$

For example, if the initial process is for 20 seconds at 220^{o}C and the next process is at 260^{o}C, then the maximum time allowed at 260^{o}C is:

For Nickel/Tin Termination:

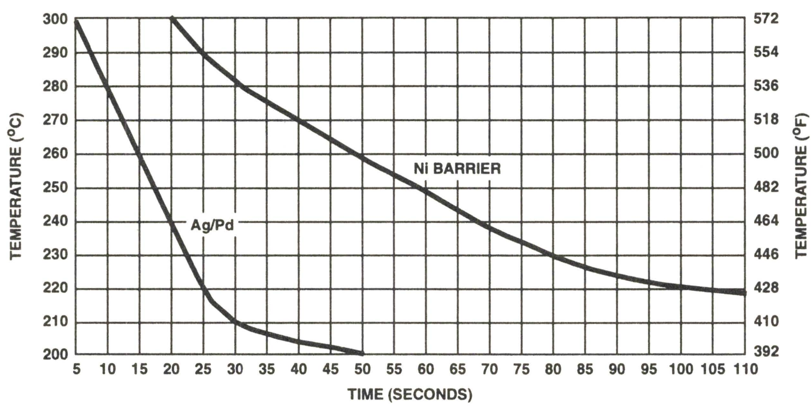
$$\frac{100-20}{100} \times 48 = 38.4 \text{ seconds}$$

For Ag/Pd Termination:

$$\frac{25-20}{25} \times 15 = 3.0 \text{ seconds}$$

Also, if the initial soldering process is for 10 seconds at 280^{o}C, the Nickel/Tin termination can withstand a further 20 seconds at 280^{o}C or an equivalent percentage of time at a subsequent temperature. For example, If the next soldering process is at 230^{o}C, the total time allowed at this temperature is:

$$\frac{30-10}{30} \times 80 = 53 \text{ seconds}$$

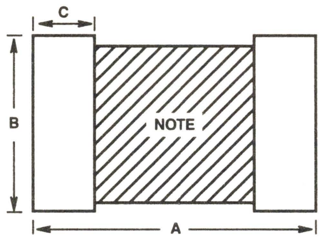


NOTES:

6. Comparative Temperature-Time data for Silver/Palladium and Nickel/Tin terminated Multilayer Suppressors.
7. The curves indicate the point at which 5% leaching of the termination will occur after immersion in a static solder bath for an 0805 size device.
8. Static solder bath = Sn/Pb (63/67). RMA no clean flux.

FIGURE 9. SOLDER TEMPERATURE-TIME CURVE

Recommended Pad Outline



NOTE: Avoid metal runs in this area.

SYMBOL	RECOMMENDED PAD SIZE DIMENSIONS					
	FOR 1206 SIZE DEVICE		FOR 0805 SIZE DEVICE		FOR 0603 SIZE DEVICE	
	IN	MM	IN	MM	IN	MM
A	0.203	5.15	0.144	3.66	0.11	2.8
B	0.103	2.62	0.084	2.13	0.064	1.62
C	0.065	1.65	0.058	1.48	0.044	1.12

Explanation of Terms

Rated DC Voltage ($V_{M(DC)}$)

This is the maximum continuous DC voltage which may be applied up to the maximum operating temperature of the device. The rated DC operating voltage (working voltage) is also used as the reference point for leakage current. This voltage is always less than the breakdown voltage of the device.

Leakage (I_L) at Rated DC Voltage

In the nonconducting mode, the device is at a very high impedance ($10^6\Omega$) and appears essentially as an open circuit in the system. The leakage current drawn at this level is very low. See Device Ratings.

Nominal Voltage ($V_{N(DC)}$)

This is the voltage at which the device changes from the off state to the on state and enters its conduction mode of operation. The voltage is usually characterized at the 1mA point and has a specified minimum and maximum voltage listed.

Clamping Voltage (V_C)

This is the peak voltage appearing across the suppressor when measured at conditions of specified pulse current and specified waveform. See Device Ratings.

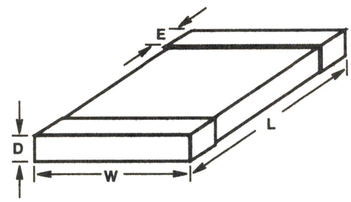
Capacitance (C)

This is the capacitance of the device at a specified frequency (1MHz) and bias (1V_{P-P}). See Device Ratings.

IEC 1000-4-2

The electrostatic discharge requirements portion of the electromagnetic compatibility standard written by the International Electrotechnical Commission. The specification describes a specific human body model test conditions and methods.

Mechanical Dimensions



SYMBOL	DEVICE DIMENSIONS					
	1206 SIZE		0805 SIZE		0603 SIZE	
	INCH	MM	INCH	MM	INCH	MM
D Max.	0.071	1.80	0.043	1.1	0.035	0.9
E	0.02 ±0.01	0.50 ±0.25	0.02 to ±0.01	0.50 to ±0.25	0.015 ±0.008	0.4 ±0.2
L	0.125 ±0.012	3.20 ±0.03	0.079 ±0.008	2.01 ±0.2	0.063 ±0.006	1.6 ±0.15
W	0.06 ±0.011	1.60 ±0.28	0.049 ±0.008	1.25 ±0.2	0.032 ±0.006	0.8 ±0.15

Ordering Information

VXXMLE TYPES

V 18 ML X 1206 X X X

DEVICE FAMILY
Harris TVSS Device

MAXIMUM DC WORKING VOLTAGE

MULTILAYER DESIGNATOR

PERFORMANCE DESIGNATOR
A: Standard
E: ESD (See ML Data Sheet)

DEVICE SIZE:
i.e., 120 mil x 60 mil

CAPACITANCE OPTION
No Letter: Standard
L: Low Capacitance Version (Where available - see device ratings for standard versions)

END TERMINATION OPTION
No Letter: Ag/P_t (Standard)
W: Ag/P_d
N: Ni/Sn

PACKING OPTIONS
A: <100 pc Bulk Pak
H: 7in (178mm) Diameter Reel (Note)
T: 13in (330mm) Diameter Reel (Note)

NOTE: See quantity table.

Standard Shipping Quantities

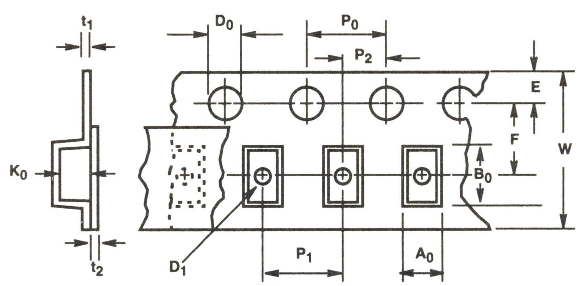
DEVICE SIZE	"13" INCH REEL ("T" OPTION)	"7" INCH REEL ("H" OPTION)	BULK PACK ("A" OPTION)
1206	10,000	2,500	100
0805	10,000	2,500	100
0603	10,000	2,500	100

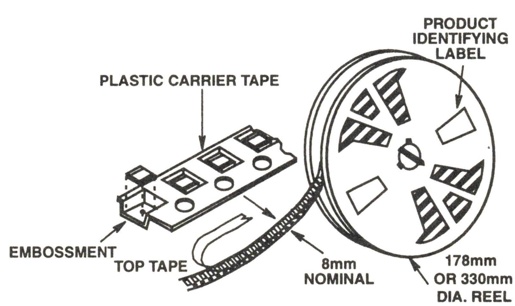
Tape and Reel Specifications

- **Conforms to EIA - 481, Revision A**
- **Can be Supplied to IEC Publication 286 - 3**

SYMBOL	DESCRIPTION	MILLIMETERS
A_0	Width of Cavity	Dependent on Chip Size to Minimize Rotation.
B_0	Length of Cavity	Dependent on Chip Size to Minimize Rotation.
K_0	Depth of Cavity	Dependent on Chip Size to Minimize Rotation.
W	Width of Tape	8 ± 0.2
F	Distance Between Drive Hole Centers and Cavity Centers	3.5 ± 0.5
E	Distance Between Drive Hole Centers and Tape Edge	1.75 ± 0.1
P_1	Distance Between Cavity Center	4 ± 0.1
P_2	Axial Distance Between Drive Hole Centers and Cavity Centers	2 ± 0.1
P_0	Axial Distance Between Drive Hole Centers	4 ± 0.1
D_0	Drive Hole Diameter	1.55 ± 0.05
D_1	Diameter of Cavity Piercing	1.05 ± 0.05
t_1	Embossed Tape Thickness	0.3 max
t_2	Top Tape Thickness	0.1 max

NOTE: Dimensions in millimeters.





5

MULTILAYER PRODUCTS

HARRIS SEMICONDUCTOR

AUML Series

January 1998

Multilayer Surface Mount Automotive Transient Surge Suppressors

Features

- **Load Dump Energy Rated per SAE Specification J1113**
- **Leadless, Surface Mount Chip Form**
- **"Zero" Lead Inductance**
- **Variety of Energy Ratings Available**
- **No Temperature Derating up to 125°C Ambient**
- **High Peak Surge Current Capability**
- **Low Profile, Compact Industry Standard Chip Size; (1206, 1210, 1812 and 2220 Sizes)**
- **Inherent Bidirectional Clamping**
- **No Plastic or Epoxy Packaging Assures Better than 94V-0 Flammability Rating**

Description

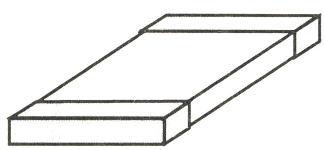
The AUML Series of Multilayer Transient Surge Suppressors was specifically designed to suppress the destructive transient voltages found in an automobile. The most common transient condition results from large inductive energy discharges. The electronic systems in the automobile, e.g. antilock brake systems, direct ignition systems, engine control, airbag control systems, wiper motor controls, etc., are susceptible to damage from these voltage transients and thus require protection. The AUML transient suppressors have temperature independent suppression characteristics affording protection from -55°C to 125°C.

The AUML suppressor is manufactured from semiconducting ceramics which offer rugged protection and excellent transient energy absorption in a small package. The devices are in ceramic leadless chip form, eliminating lead inductance and assuring fast speed of response to transient surges. These Suppressors require significantly smaller space and land pads than silicon TVS diodes, offering greater circuit board layout flexibility for the designer.

Also see the Harris ML Series and MLE Series of Multilayer Suppressors.

Packaging

AUML SERIES



File Number **3387.4**

Absolute Maximum Ratings For ratings of individual members of a series, see Device Ratings and Specifications chart

	AUML SERIES	UNITS
Continuous:		
Steady State Applied Voltage:		
DC Voltage Range ($V_{M(DC)}$)	18	V
Transient:		
Load Dump Energy, (W_{LD})	1.5 to 25	J
Jump Start Capability (5 minutes), (V_{JUMP})	24.5	V
Operating Ambient Temperature Range (T_A)	-55 to 125	^oC
Storage Temperature Range (T_{STG})	-55 to 150	^oC
Temperature Coefficient (αv) of Clamping Voltage (V_C) at Specified Test Current	<0.01	%/^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Device Ratings and Specifications

PART NUMBER	MAXIMUM RATINGS (125^{o}C)			SPECIFICATIONS (25^{o}C)				
	MAXIMUM CONTINUOUS DC VOLTAGE	JUMP START VOLTAGE (5 MIN)	LOAD DUMP ENERGY (10 PULSES)	NOMINAL VARISTOR VOLTAGE AT 10mA DC TEST CURRENT		MAXIMUM STANDBY LEAKAGE (AT 13V DC)	MAXIMUM CLAMPING VOLTAGE (V_C) AT TEST CURRENT (8/20μs)	
	$V_{M(DC)}$	V_{JUMP}	W_{LD}	$V_{N(DC)}$ MIN	$V_{N(DC)}$ MAX	I_L	V_C	I_P
	(V)	(V)	(J)	(V)	(V)	(μA)	(V)	(A)
V18AUMLA1206	18	24.5	1.5	23	32	50	40	1.5
V18AUMLA1210	18	24.5	3	23	32	50	40	1.5
V18AUMLA1812	18	24.5	6	23	32	100	40	5
V18AUMLA2220	18	24.5	25	23	32	200	40	40

NOTES:

1. Average power dissipation of transients not to exceed 0.1W, 0.15W, 0.3W and 1W for model sizes 1206, 1210, 1812 and 2220 respectively.
2. Load dump energy rating (into the suppressor) of a voltage transient with a resultant time constant of 115ms to 230ms.
3. Thermal shock capability per Mil-Std-750, Method 1051: -55^{o}C to 125^{o}C, 5 minutes at 25^{o}C, 25 Cycles: 15 minutes at each extreme.
4. For application specific requirements, please contact Harris sales office.

Power Dissipation Ratings

When transients occur in rapid succession, the average power dissipation is the energy (watt-seconds) per pulse times the number of pulses per second. The power so developed must be within the specifications shown on the Device Ratings and Characteristics table for the specific device. Certain parameter ratings must be derated at high temperatures as shown in Figure 1.

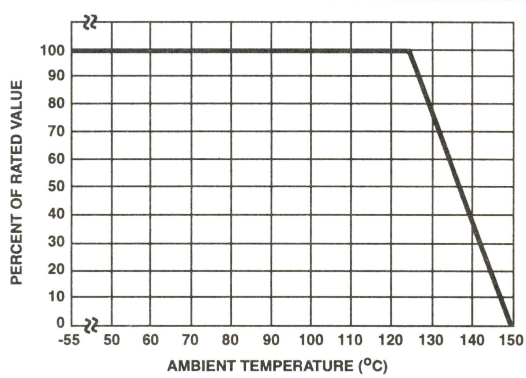


FIGURE 1. CURRENT, ENERGY AND POWER DERATING CURVE

V-I Characteristics Curves

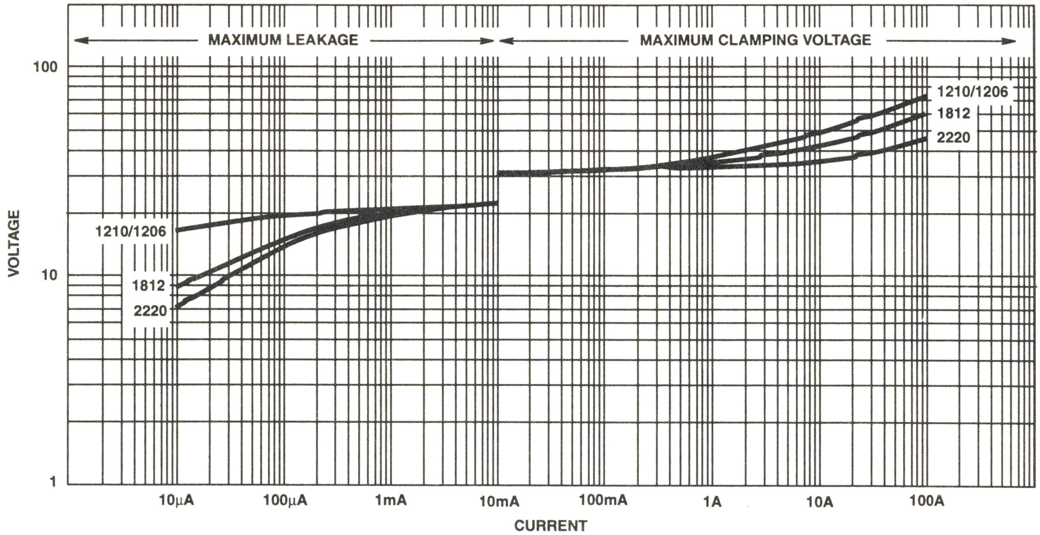


FIGURE 2. MAXIMUM LEAKAGE CURRENT/CLAMPING VOLTAGE CURVE FOR AUML SERIES AT 25°C

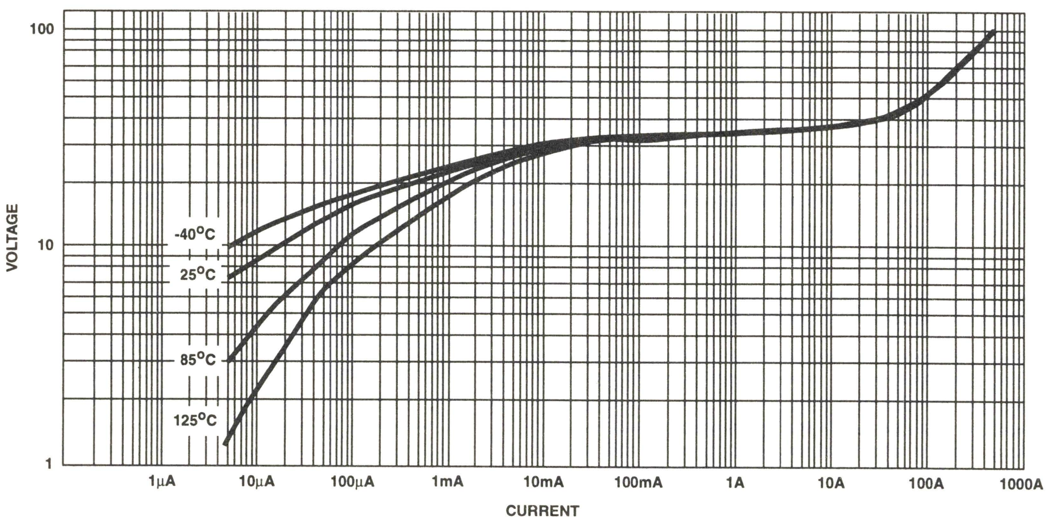


FIGURE 3. TYPICAL V-I CHARACTERISTICS OF THE V18AUMLA2220 at -40°C, 25°C, 85°C AND 125°C

Temperature Effects

In the leakage region of the AUML suppressor, the device characteristics approaches a linear (ohmic) relationship and shows a temperature dependent affect. In this region the suppressor is in a high resistance mode (approaching $10^6\Omega$) and appears as a near open-circuit. Leakage currents at maximum rated voltage are in the microamp range. When clamping transients at higher currents (at and above the ten milliamp range), the AUML suppressor approaches a 1-10Ω characteristic. In this region the characteristics of the AUML are virtually temperature independent. Figure 3 shows the typical effect of temperature on the V-I characteristics of the AUML suppressor.

Load Dump Energy Capability

A Load dump transient occurs when the alternator load in the automobile is abruptly reduced. The worst case scenario of this transient occurs when the battery is disconnected while operating at full rated load. There are a number of different load dump specifications in existence in the automotive industry, with the most common one being that recommended by the Society of Automotive Engineers, specification #SAE J1113. Because of the diversity of these load dump specifications Harris defines the load dump energy capability of the AUML suppressor range as that energy dissipated by the device itself, independent of the test circuit setup. The resultant load dump energy handling capability serves as an excellent figure of merit for the AUML suppressor.

Standard load dump specifications require a device capability of 10 pulses at rated energy, across a temperature range of -40°C to 125°C. This capability requirement is well within the ratings of all of the AUML series (Figure 6).

Further testing on the AUML series has concentrated on extending the number of load dump pulses, at rated energy, which are applied to the devices. The reliability information thus generated gives an indication of the inherent capability of these devices. As an example of device durability the 1210 size has been subjected to over 2000 pulses at its rated energy of 3 joules; the 1812 size have been pulsed over 1000 times at 6 joules and 2220 size has been pulsed at its rated energy of 25 joules over 300 times. In all cases there has been little or no change in the device characteristics (Figure 7).

The very high energy absorption capability of the AUML suppressor is achieved by means of a highly controlled manufacturing process. This technology ensures that a large volume of suppressor material, with an interdigitated layer construction, is available for energy absorption in an extremely small package. Unlike equivalent rated silicon TVS diodes, the entire AUML device volume is available to dissipate the load dump energy. Hence, the peak temperatures generated by the load dump transient are significantly lower and evenly dissipated throughout the complete device (Figure 4). This even energy dissipation ensures that there are lower peak temperatures generated at the P-N grain boundaries of the AUML suppressor.

There are a number of different size devices available in the AUML series, each one with a load dump energy rating, which is size dependent.

Experience has shown that while the effects of a load dump transient is of real concern, its frequency of occurrence is much less than those of low energy inductive spikes. Such low energy inductive spikes may be generated as a result of motors switching on and off, from ESD occurrences, fuse blowing, etc. It is essential that the suppression technology selected also has the capability to suppress such transients. Testing on the V18AUMLA2220 has shown that after being subjected to a repetitive energy pulse of 2 joules, over 6000 times, no characteristic changes have occurred (Figure 8.)

Speed of Response

The clamping action of the AUML suppressor depends on a conduction mechanism similar to that of other semiconductor devices (i.e. P-N Junctions). The apparent slow response time often associated with transient voltage suppressors (Zeners, MOVs) is often due to parasitic inductance in the package and leads of the device and less dependent of the basic material (silicon, zinc oxide). Thus, the single most critical element affecting the response time of any suppressor is its lead inductance. The AUML suppressor is a surface mount device, with no leads or external packaging, and thus, it has virtually zero inductance. The actual response time of a AUML surge suppressor is in the 1 to 5 nanosecond range, more than sufficient for the transients which are likely to be encountered in an automotive environment.

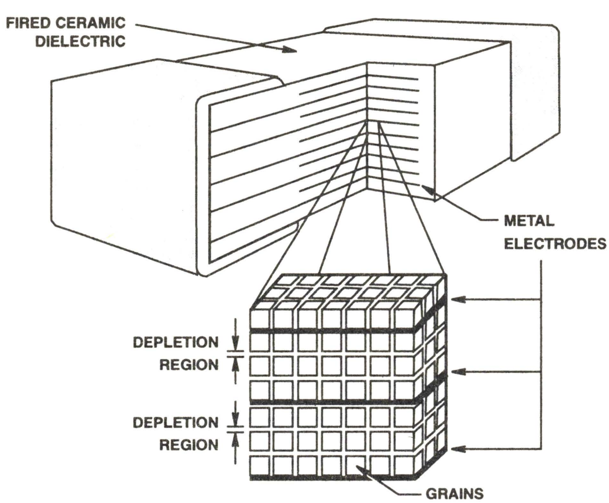


FIGURE 4. INTERDIGITATED CONSTRUCTION OF AUML SUPPRESSOR

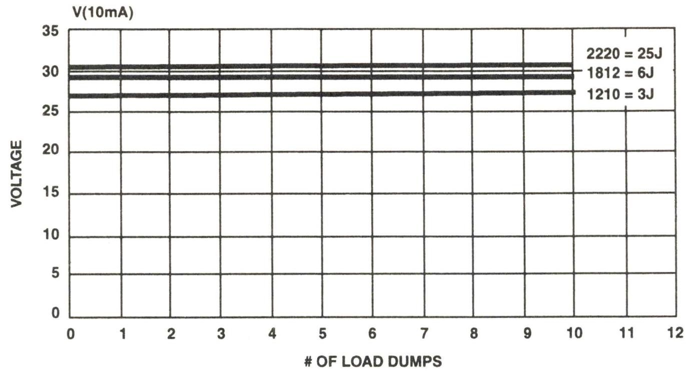


FIGURE 5. AUML LOAD DUMP PULSING OVER A TEMPERATURE RANGE OF -55°C TO 125°C

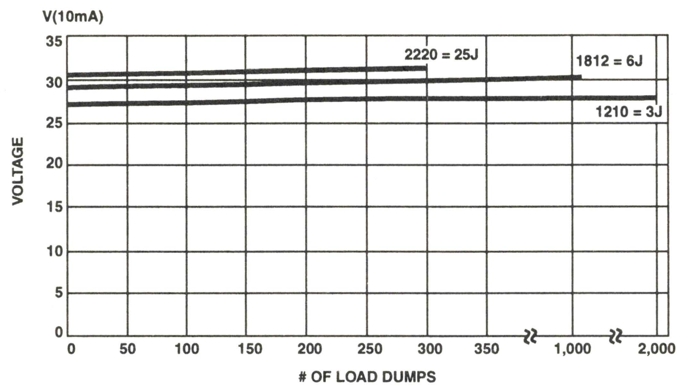


FIGURE 6. REPETITIVE LOAD DUMP PULSING AT RATED ENERGY

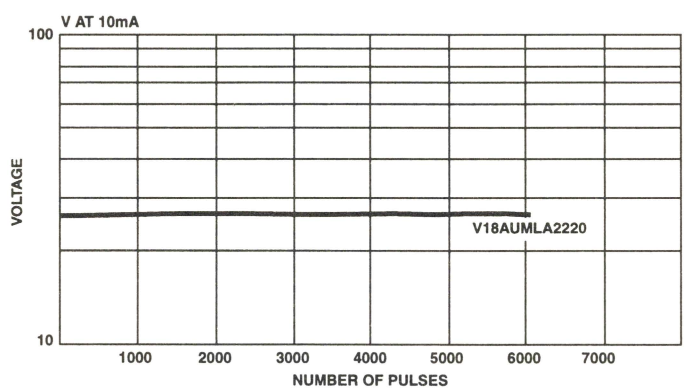


FIGURE 7. REPETITIVE ENERGY TESTING OF THE V18AUMLA2220 AT AN ENERGY LEVEL OF 2 JOULES

Soldering Recommendations

The principal techniques used for the soldering of components in surface mount technology are Infra Red (IR) Reflow, Vapour Phase Reflow, and Wave Soldering. When wave soldering, the suppressor is attached to the circuit board by means of an adhesive. The assembly is then placed on a conveyor and run through the soldering process to contact the wave. With IR and Vapour Phase Reflow, the device is placed in a solder paste on the substrate. As the solder paste is heated, it reflows and solders the unit to the board.

The recommended solder is a 62/36/2 (Sn/Pb/Ag), 60/40 (Sn/Pb), or 63/37 (Sn/Pb). Harris also recommends an RMA solder flux.

Wave soldering is the most strenuous of the processes. To avoid the possibility of generating stresses due to thermal shock, a preheat stage in the soldering process is recommended, and the peak temperature of the solder process should be rigidly controlled.

When using a reflow process, care should be taken to ensure that the chip is not subjected to a thermal gradient steeper than 4 degrees per second; the ideal gradient being 2 degrees per second. During the soldering process, preheating to within 100 degrees of the solders peak temperature is essential to minimize thermal shock. Examples of the soldering conditions for the AUML Series of suppressors are given in the tables below.

Once the soldering process has been completed, it is still necessary to ensure that any further thermal shocks are avoided. One possible cause of thermal shock is hot printed circuit boards being removed from the solder process and subjected to cleaning solvents at room temperature. The boards must be allowed to gradually cool to less than 50°C before cleaning.

Termination Options

Harris offers three types of termination finish on the Multilayer product series:

1. Silver/Platinum (standard)
2. Silver/Palladium (optional)
3. Nickel/Tin (optional) (1206/1210 only)

(The ordering information section describes how to designate them.)

The Nickel/Tin plated termination can provide certain solder process application benefits such as:

- A better match to Tin/Lead solders resulting in improved solder wetting and solder fillet height (typically 70% of component height).
- An enhanced resistance to solder leaching permits greater flexibility/latitude in the design and control of solder processes. (See the temperature-time graph below.)
- An alternative material when silver end terminations are restricted.

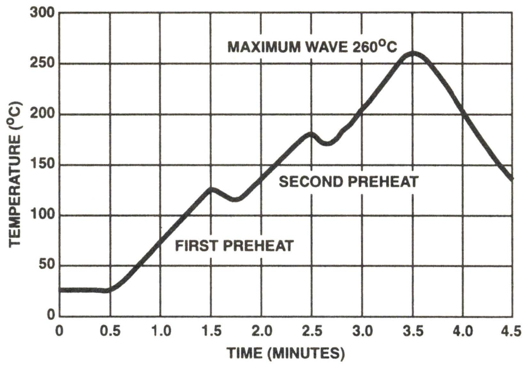


FIGURE 8. WAVE SOLDER PROFILE

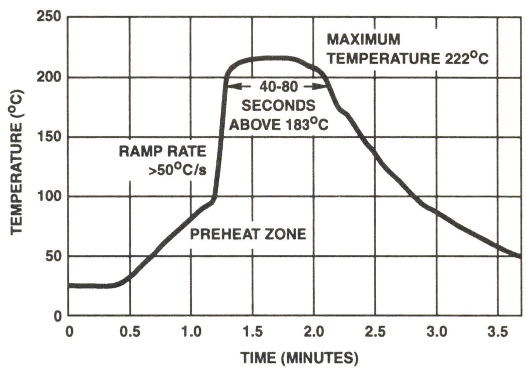


FIGURE 9. VAPOR PHASE SOLDER PROFILE

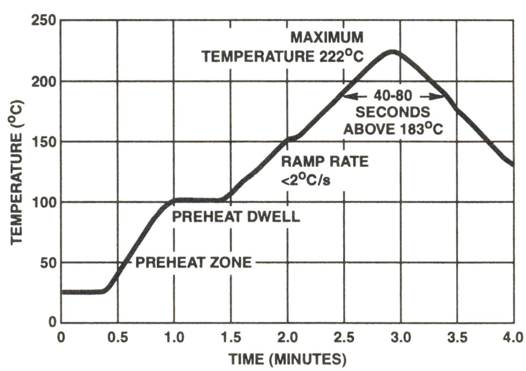


FIGURE 10. REFLOW SOLDER PROFILE

5
MULTILAYER PRODUCTS

Solder Process Time Advantages for Nickel/Tin Terminated Multilayer Suppressors

Certain surface mount soldering processes require long duration or multiple soldering cycles for top and bottom side assemblies and/or for reworking rejected product. In these instances, devices with a Nickel/Tin finish offer greater dwell time, for example, when end termination leaching is of concern. The Solder Temperature-Time Curve shown can be used as a guideline when designing process variables and rework operations and illustrates the greater latitude afforded with this material.

Since end termination leaching is a function of the cumulative molten dwell time, then the molten time duration allowed at subsequent operations is reduced by the percentage of time used by the initial operation. Using the curve for the applicable material,

$$\frac{\text{Total Time at Initial Temp - Actual Time at Initial Temp}}{\text{Total Time at Initial Temp}}$$

$$\times \text{Total Time Permitted at the Subsequent Temp}$$

For example, if the initial process is for 20 seconds at 220^{o}C and the next process is at 260^{o}C, then the maximum time allowed at 260^{o}C is:

For Nickel/Tin Termination:

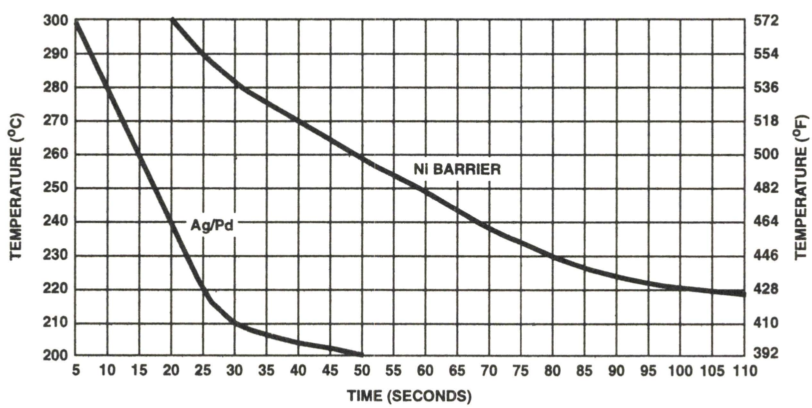
$$\frac{100 - 20}{100} \times 48 = 38.4 \text{ seconds}$$

For Ag/Pd Termination:

$$\frac{25 - 20}{25} \times 15 = 3.0 \text{ seconds}$$

Also, if the initial soldering process is for 10 seconds at 280^{o}C, the Nickel/Tin termination can withstand a further 20 seconds at 280^{o}C or an equivalent percentage of time at a subsequent temperature. For example, If the next soldering process is at 230^{o}C, the total time allowed at this temperature is:

$$\frac{30 - 10}{30} \times 80 = 53 \text{ seconds}$$

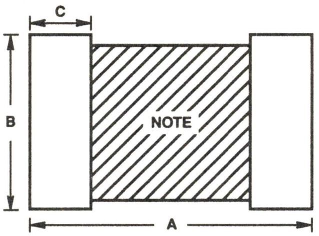


NOTES:

5. Comparative Temperature-Time data for Silver/Palladium and Nickel/Tin terminated Multilayer Suppressors.
6. The curves indicate the point at which 5% leaching of the termination will occur after immersion in a static solder bath for an 0805 size device.
7. Static solder bath = Sn/Pb (63/67). RMA no clean flux.

FIGURE 11. SOLDER TEMPERATURE-TIME CURVE

Recommended Pad Outline



NOTE: Avoid metal runs in this area.

SYMBOL	CHIP SIZE							
	1206		1210		1812		2220	
	IN	MM	IN	MM	IN	MM	IN	MM
A	0.203	5.15	0.219	5.51	0.272	6.91	0.315	8.00
B	0.103	2.62	0.147	3.73	0.172	4.36	0.240	6.19
C	0.065	1.65	0.073	1.85	0.073	1.85	0.073	1.85

Explanation of Terms

Maximum Continuous DC Working Voltage ($V_{M(DC)}$)

This is the maximum continuous DC voltage which may be applied, up to the maximum operating temperature (125°C), to the ML suppressor. This voltage is used as the reference test point for leakage current and is always less than the breakdown voltage of the device.

Load Dump Energy Rating (W_{LD})

This is the actual energy the part is rated to dissipate under load dump conditions (not to be confused with the "source energy" of a load dump test specification).

Maximum Clamping Voltage (V_C)

This is the peak voltage appearing across the suppressor when measured at conditions of specified pulse current and specified waveform (8/20μs). It is important to note that the peak current and peak voltage may not necessarily be coincidental in time.

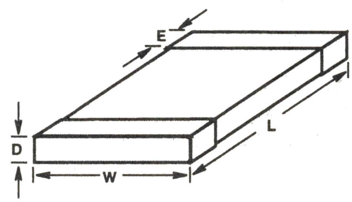
Leakage Current (I_L)

In the nonconducting mode, the device is at a very high impedance (approaching $10^6\Omega$ at its rated working voltage) and appears as an almost open circuit in the system. The leakage current drawn at this level is very low (<25μA at ambient temperature) and, unlike the zener diode, the multilayer TVS has the added advantage that, when operated up to its maximum temperature, its leakage current will not increase above 500μA.

Nominal Voltage ($V_{N(DC)}$)

This is the voltage at which the AUML enters its conduction state and begins to suppress transients. In the automotive environment this voltage is defined at the 10 milliamp point and has a minimum ($V_{N(DC)\ MIN}$) and maximum ($V_{N(DC)\ MAX}$) voltage specified.

Mechanical Dimensions

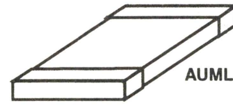


SYMBOL	CHIP SIZE							
	1206		1210		1812		2220	
	IN	MM	IN	MM	IN	MM	IN	MM
D MAX	0.071	1.80	0.070	1.80	0.07	1.8	0.118	3.00
E	0.02 ±0.01	0.50 ±0.25	0.02 ±0.01	0.50 ±0.25	0.02 ±0.01	0.5 ±0.25	0.03 ±0.01	0.75 ±0.25
L	0.125 ±0.012	3.20 ±0.03	0.125 ±0.012	3.20 ±0.30	0.18 ±0.014	4.5 ±0.35	0.225 ±0.016	5.7 ±0.4
W	0.06 ±0.011	1.60 ±0.28	0.10 ±0.012	2.54 ±0.30	0.125 ±0.012	3.2 ±0.30	0.197 ±0.016	5 ±0.4

Ordering Information

V18AUMLAXXXX TYPES

V 18 AUML A 2220 X X



AUML SERIES

DEVICE FAMILY
Harris TVSS Device

MAXIMUM DC WORKING VOLTAGE

AUTOMOTIVE MULTILAYER DESIGNATOR

LOAD DUMP ENERGY RATING INDICATOR

DEVICE SIZE:
i.e., 220 mil x 200 mil

END TERMINATION OPTION
No Letter: Ag/P_t (Standard)
W: Ag/P_d
N: Ni/Sn (1206/1210 Only)

PACKING OPTIONS
A: <100 pc Bulk Pack
H: 7in (178mm) Diameter Reel (Note)
T: 13in (330mm) Diameter Reel (Note)

NOTE: See quantity table.

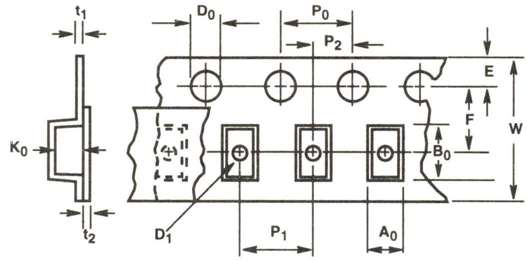
Standard Shipping Quantities

DEVICE SIZE	"13" INCH REEL ("T" OPTION)	"7" INCH REEL ("H" OPTION)	BULK PACK ("A" OPTION)
1206	10,000	2,500	100
1210	8,000	2,000	100
1812	4,000	1,000	100
2220	4,000	1,000	100

Tape and Reel Specifications

- **Conforms to EIA - 481, Revision A**
- **Can be Supplied to IEC Publication 286 - 3**

TAPE	8mm WIDE TAPE		12mm WIDE TAPE	
Chip Size	1206	1210	1812	2220

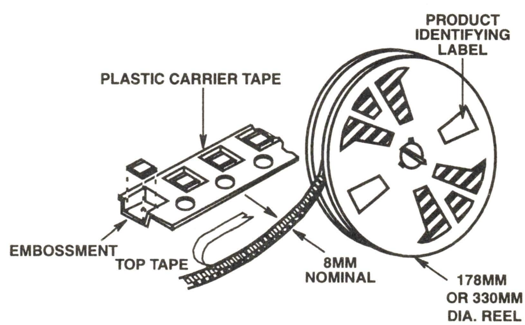


SYMBOL	DESCRIPTION	TAPE WIDTH	
		8mm	12mm
A_0	Width of Cavity	Dependent on Chip Size to Minimize Rotation.	
B_0	Length of Cavity	Dependent on Chip Size to Minimize Rotation.	
K_0	Depth of Cavity	Dependent on Chip Size to Minimize Rotation.	
W	Width of Tape	8 ± 0.2	12 ± 0.2
F	Distance Between Drive Hole Centers and Cavity Centers	3.5 ± 0.5	5.4 ± 0.5
E	Distance Between Drive Hole Centers and Tape Edge	1.75 ± 0.1	
P_1	Distance Between Cavity Center	4 ± 0.1	8 ± 0.1
P_2	Axial Distance Between Drive Hole Centers and Cavity Centers	2 ± 0.1	
P_0	Axial Distance Between Drive Hole Centers	8 ± 0.1	
D_0	Drive Hole Diameter	1.55 ± 0.05	
D_1	Diameter of Cavity Piercing	1.05 ± 0.05	1.55 ± 0.05
t_1	Embossed Tape Thickness	0.3 max	0.4 max
t_2	Top Tape Thickness	0.1 max	

NOTE: Dimensions in millimeters.

Standard Packaging

Tape and reel is the standard packaging method of the AUML series. The standard 330 millimeter (13 inch) reel utilized contains 4000 pieces for the 2220 and 1812 chips, 8000 pieces for the 1210 chip and 10,000 pieces for the 1206 size. To order add "T" to the standard part number, e.g. V18AUMLA2220T.



Special Packaging

Option 1: 178 millimeter (7 inch) reels containing 1000 (2220, 1812), 2000 (1210), 2500 (1206), pieces are available. To order add "H" to the standard part number, e.g. V18AUMLA2220H.

Option 2: For small sample quantities (less than 100 pieces) the units are shipped bulk pack. To order add "A" to the standard part number, e.g. V18AUMLA2220A.

5

MULTILAYER PRODUCTS

TVS 6

INTEGRATED PROTECTION CIRCUITS

Integrated Protection Circuit Overview

The Harris SP Series is comprised of Silicon Integrated Circuit Arrays of SCR/Diode structures. These devices have been designed and developed to withstand extreme ESD conditions, enabling them to protect other Silicon devices on data, signal and control lines. The unique SP Series functions by diverting transients from these lines to the power supply - away from sensitive components.

The family includes devices capable of withstanding 15kV (IEC air discharge method) or 8kV (IEC contact method) themselves without damage or degradation. Supplied in DIP and SOP, the SP720, 721 and 723 are designed for the circuit board-level, working up to 35VDC. These devices provide suppression of ESD and other transients for the protection of products such as those listed in the Selection Guide table below.

Supplemental application notes are provided in Section 11.

Transient Voltage Suppressor Device Selection Guide

MARKET SEGMENT	TYPICAL APPLICATIONS AND CIRCUITS EXAMPLES	DEVICE FAMILY OR SERIES	DATA BOOK SECTION	TECHNOLOGY	SURFACE MOUNT PRODUCT?
Low Voltage, Board Level Products	• Hand-Held/Portable Devices • EDP • Computer • I/O Port and Interfaces • Controllers • Instrumentation • Remote Sensors • Medical Electronics, etc.	CH	4	MOV	✓
		MA, ZA, RA	4	MOV	
		ML, MLE	5	Multilayer Suppressor	✓
		SP72X	**6**	**SCR/Diode Array**	✓ †
AC Line, TVSS Products	• UPS • AC Panels • AC Power Taps • TVSS Devices • AC Appliance/Controls • Power Meters • Power Supplies • Circuit Breakers • Consumer Electronics	UltraMOV™, "C" III, LA, HA, RA	4	MOV	
		CH	4	MOV	✓
		GDT	7	Gas Discharge Tube	
Automotive Electronics	• ABS • EEC • Instrument Cluster • Air Bag • Window Control • Wiper Modules • Multiplex Bus • EFI	CH	4	MOV	✓
		ZA	4	MOV	
		AUML, ML	5	Multilayer Suppressor	✓
		SP72X	**6**	**SCR/Diode Array**	✓ †
Telecommunications Products	• Cellular/Cordless Phone • Modems • Secondary Phone Line Protectors • Data Line Connectors • Repeaters • Line Cards	CH	4	MOV	✓
		CP, CS, ZA	4	MOV	
		ML, MLE	5	Multilayer Suppressor	✓
		SP72X	**6**	**SCR/Diode Array**	✓ †
		GDT	7	Gas Discharge Tube	
		Surgector	8	Thyristor/Zener	
Industrial, High Energy AC Products	• High Current Relays • Solenoids • Motor Drives • AC Distribution Panels • Robotics • Large Motors	DA/DB, BA/BB, CA, HA, NA, PA	4	MOV	
		GDT	7	Gas Discharge Tube	
Arrester Products	• Lightning Arrester Assemblies for High Voltage AC Power Distribution Lines and Utility Transformers	AS	9	MOV	

†Available in both surface mount and through-hole packages.

HARRIS SEMICONDUCTOR

SP720

Electronic Protection Array for ESD and Over-Voltage Protection

January 1998

Features

- ESD Interface Capability for HBM Standards
  - MIL STD 3015.7 .... 15kV
  - IEC 1000-4-2, Direct Discharge,
    Single Input .... 4kV (Level 2)
    Two Inputs in Parallel .... 8kV (Level 4)
  - IEC 1000-4-2, Air Discharge .... 15kV (Level 4)
- High Peak Current Capability
  - IEC 1000-4-5 (8/20μs) .... ±3A
  - Single Pulse, 100μs Pulse Width .... ±2A
  - Single Pulse, 4μs Pulse Width .... ±5A
- Designed to Provide Over-Voltage Protection
  - Single-Ended Voltage Range to .... +30V
  - Differential Voltage Range to .... ±15V
- Fast Switching .... 2ns Risetime
- Low Input Leakages .... 1nA at 25°C (Typ)
- Low Input Capacitance .... 3pF (Typ)
- An Array of 14 SCR/Diode Pairs
- Operating Temperature Range .... -40°C to 105°C

Applications

- Microprocessor/Logic Input Protection
- Data Bus Protection
- Analog Device Input Protection
- Voltage Clamp

Description

The SP720 is an array of SCR/Diode bipolar structures for ESD and over-voltage protection to sensitive input circuits. The SP720 has 2 protection SCR/Diode device structures per input. A total of 14 available inputs can be used to protect up to 14 external signal or bus lines. Over-voltage protection is from the IN (pins 1-7 and 9-15) to V+ or V-. The SCR structures are designed for fast triggering at a threshold of one $+V_{BE}$ diode threshold above V+ (Pin 16) or a $-V_{BE}$ diode threshold below V- (Pin 8). From an IN input, a clamp to V+ is activated if a transient pulse causes the input to be increased to a voltage level greater than one V_{BE} above V+. A similar clamp to V- is activated if a negative pulse, one V_{BE} less than V-, is applied to an IN input. Standard ESD Human Body Model (HBM) Capability is:

HBM STANDARD	MODE	R	C	ESD (V)
IEC 1000-4-2	Air	330Ω	150pF	>15kV
	Direct	330Ω	150pF	>4kV
	Direct, Dual Pins	330Ω	150pF	>8kV
MIL-STD-3015.7	Direct, In-circuit	1.5kΩ	100pF	>15kV

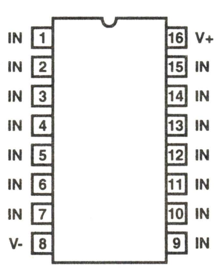
Refer to Figure 1 and Table 1 for further detail. Refer to Application Note AN9304 and AN9612 for additional information.

Ordering Information

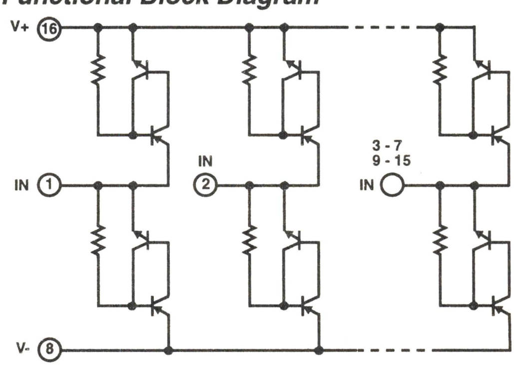
PART NO.	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
SP720AP	-40 to 105	16 Ld PDIP	E16.3
SP720AB	-40 to 105	16 Ld SOIC	M16.15
SP720ABT	-40 to 105	16 Ld SOIC Tape and Reel	M16.15

Pinout

SP720 (PDIP, SOIC)
TOP VIEW



Functional Block Diagram



6
INTEGRATED PROTECTION CKTs

NOTE: The design of the SP720 SCR/Diode ESD Protection Arrays is covered by Harris patent 4567500.

File Number 2791.10

Absolute Maximum Ratings

Continuous Supply Voltage, (V+) - (V-). . . . . +35V
Forward Peak Current, I_{IN} to V_{CC}, I_{IN} to GND
(Refer to Figure 6). . . . . ±2A, 100µs
ESD Ratings and Capability (Figure 1, Table 1)
Load Dump and Reverse Battery (Note 2)

Thermal Information

Thermal Resistance (Typical, Note 1) θ_{JA} (°C/W)
PDIP Package 90
SOIC Package 130
Maximum Storage Temperature Range . . . . -65°C to 150°C
Maximum Junction Temperature (Plastic Package) . . . . 150°C
Maximum Lead Temperature (Soldering 10s) . . . . 300°C
(SOIC Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

T_A = -40°C to 105°C; V_{IN} = 0.5V_{CC} Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage Range, V_{SUPPLY} = [(V+) - (V-)]	V_{SUPPLY}		-	2 to 30	-	V
Forward Voltage Drop:		I_{IN} = 1A (Peak Pulse)				
IN to V-	V_{FWDL}		-	2	-	V
IN to V+	V_{FWDH}		-	2	-	V
Input Leakage Current	I_{IN}		-20	5	20	nA
Quiescent Supply Current	$I_{QUIESCENT}$		-	50	200	nA
Equivalent SCR ON Threshold		Note 3	-	1.1	-	V
Equivalent SCR ON Resistance		V_{FWD}/I_{FWD}; Note 3	-	1	-	Ω
Input Capacitance	C_{IN}		-	3	-	pF
Input Switching Speed	t_{ON}		-	2	-	ns

NOTES:

2. In automotive and battery operated systems, the power supply lines should be externally protected for load dump and reverse battery. When the V+ and V- pins are connected to the same supply voltage source as the device or control line under protection, a current limiting resistor should be connected in series between the external supply and the SP720 supply pins to limit reverse battery current to within the rated maximum limits. Bypass capacitors of typically 0.01µF or larger from the V+ and V- pins to ground are recommended.
3. Refer to the Figure 3 graph for definitions of equivalent "SCR ON Threshold" and "SCR ON Resistance." These characteristics are given here for thumb-rule information to determine peak current and dissipation under EOS conditions.

ESD Capability

ESD capability is dependent on the application and defined test standard. The evaluation results for various test standards and methods based on Figure 1 are shown in Table 1.

For the "Modified" MIL-STD-3015.7 condition that is defined as an "in-circuit" method of ESD testing, the V+ and V- pins have a return path to ground and the SP720 ESD capability is typically greater than 15kV from 100pF through 1.5kΩ. By strict definition of MIL-STD-3015.7 using "pin-to-pin" device testing, the ESD voltage capability is greater than 6kV. The MIL-STD-3015.7 results were determined from AT&T ESD Test Lab measurements.

The HBM capability to the IEC 1000-4-2 standard is greater than 15kV for air discharge (Level 4) and greater than 4kV for direct discharge (Level 2). Dual pin capability (2 adjacent pins in parallel) is well in excess of 8kV (Level 4).

For ESD testing of the SP720 to EIAJ IC121 Machine Model (MM) standard, the results are typically better than 1kV from 200pF with no series resistance.

TABLE 1. ESD TEST CONDITIONS

STANDARD	TYPE/MODE	R_D	C_D	$\pm V_D$
MIL STD 3015.7	Modified HBM	1.5kΩ	100pF	15kV
	Standard HBM	1.5kΩ	100pF	6kV
IEC 1000-4-2	HBM, Air Discharge	330Ω	150pF	15kV
	HBM, Direct Discharge	330Ω	150pF	4kV
	HBM, Direct Discharge, Two Parallel Input Pins	330Ω	150pF	8kV
EIAJ IC121	Machine Model	0kΩ	200pF	1kV

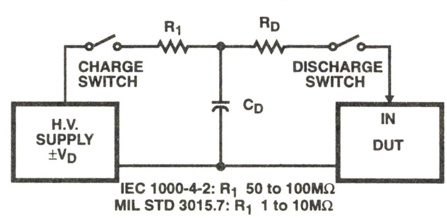


FIGURE 1. ELECTROSTATIC DISCHARGE TEST

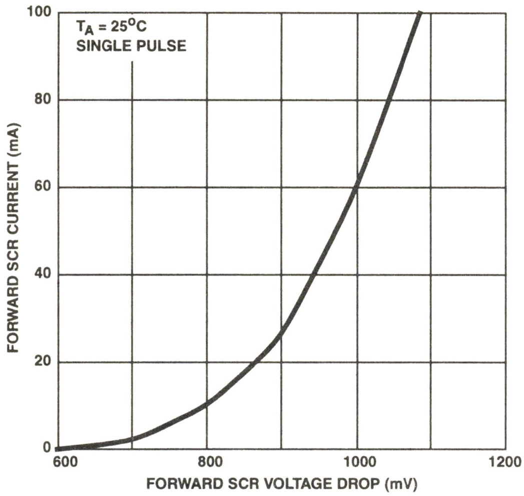


FIGURE 2. LOW CURRENT SCR FORWARD VOLTAGE DROP CURVE

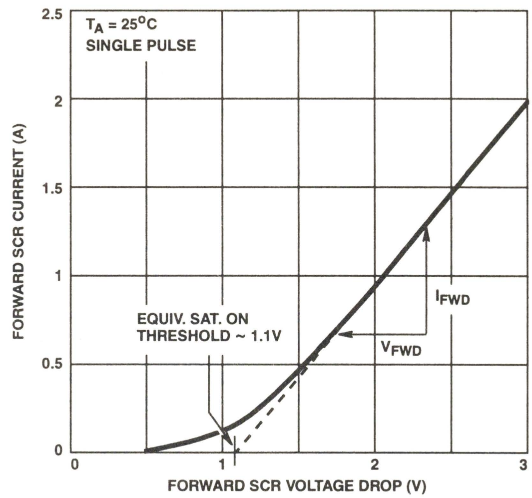


FIGURE 3. HIGH CURRENT SCR FORWARD VOLTAGE DROP CURVE

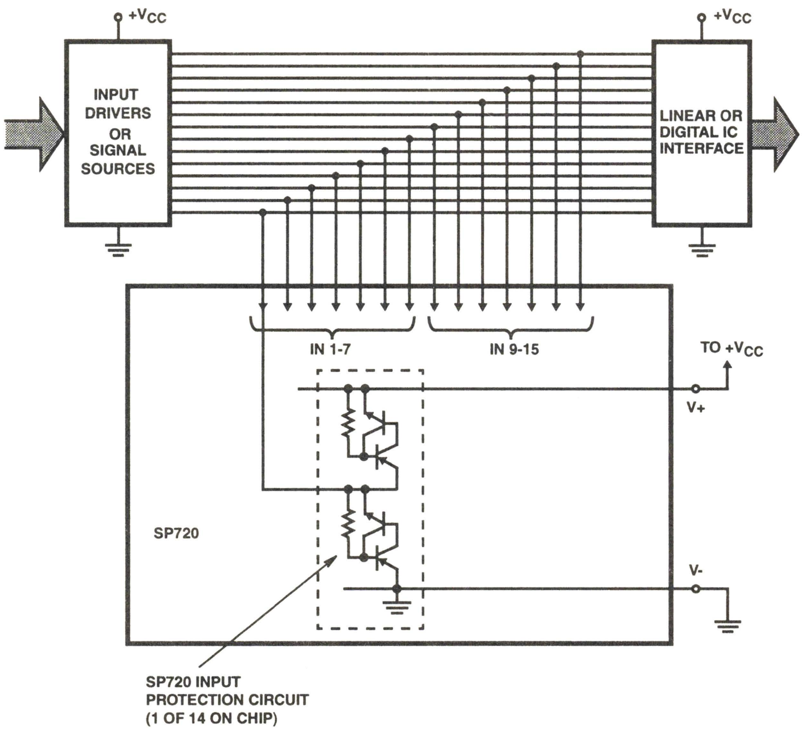


FIGURE 4. TYPICAL APPLICATION OF THE SP720 AS AN INPUT CLAMP FOR OVER-VOLTAGE, GREATER THAN $1V_{BE}$ ABOVE V+ OR LESS THAN $-1V_{BE}$ BELOW V-

6

INTEGRATED PROTECTION CKTs

Peak Transient Current Capability of the SP720

The peak transient current capability rises sharply as the width of the current pulse narrows. Destructive testing was done to fully evaluate the SP720's ability to withstand a wide range of transient current pulses. The circuit used to generate current pulses is shown in Figure 5.

The test circuit of Figure 5 is shown with a positive pulse input. For a negative pulse input, the (-) current pulse input goes to an SP720 'IN' input pin and the (+) current pulse input goes to the SP720 V- pin. The V+ to V- supply of the SP720 must be allowed to float. (i.e. It is not tied to the ground reference of the current pulse generator.) Figure 6 shows the point of over-stress as defined by increased leakage in excess of the data sheet published limits.

The maximum peak input current capability is dependent on the V+ to V- voltage supply level, improving as the supply voltage is reduced. Values of 0, 5, 15 and 30 voltages are shown. The safe operating range of the transient peak current should be limited to no more than 75% of the measured over-stress level for any given pulse width as shown in Figure 6.

When adjacent input pins are paralleled, the sustained peak current capability is increased to nearly twice that of a single pin. For comparison, tests were run using dual pin combinations 1+2, 3+4, 5+6, 7+9, 10+11, 12+13 and 14+15. The over-stress curve is shown in Figure 6 for a 15V supply condition. The dual pins are capable of 10A peak current for a 10µs pulse and 4A peak current for a 1ms pulse. The complete for single pulse peak current vs. pulse width time ranging up to 1 second are shown in Figure 6.

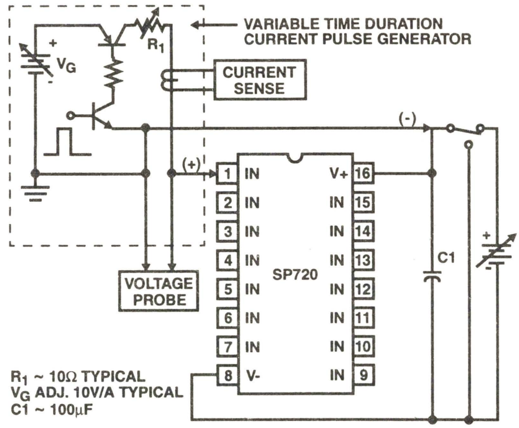


FIGURE 5. TYPICAL SP720 PEAK CURRENT TEST CIRCUIT WITH A VARIABLE PULSE WIDTH INPUT

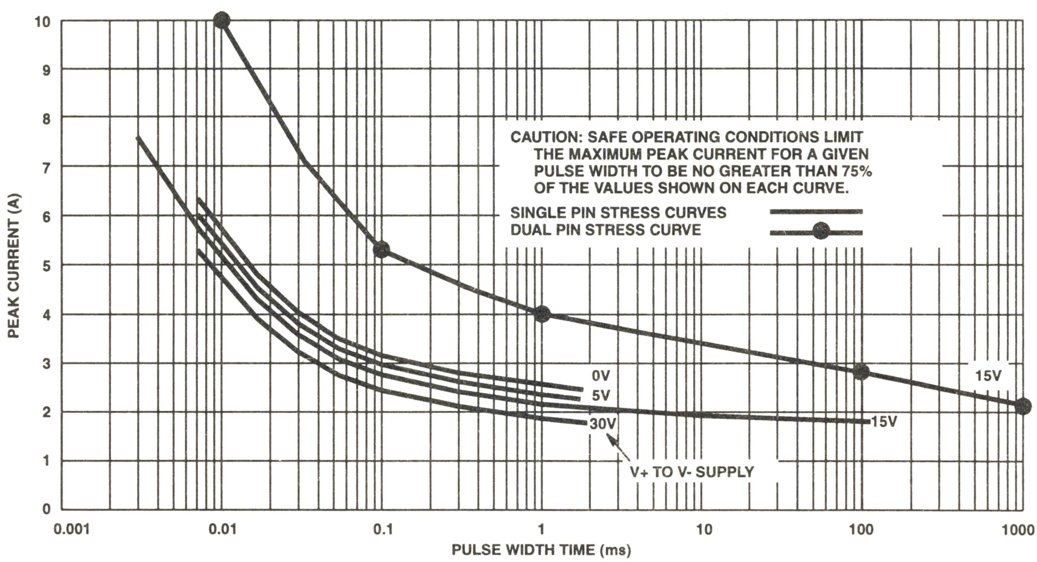
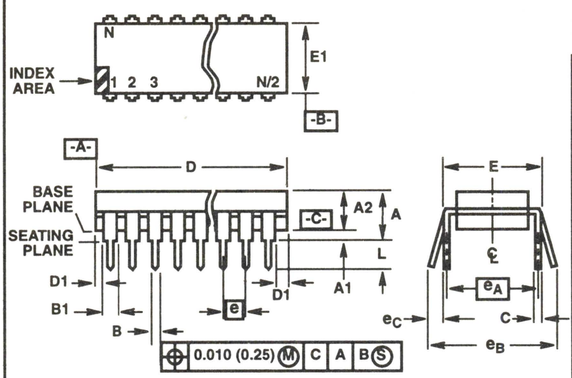


FIGURE 6. SP720 TYPICAL SINGLE PULSE PEAK CURRENT CURVES SHOWING THE MEASURED POINT OF OVER-STRESS IN AMPERES vs PULSE TIME IN MILLISECONDS, ($T_A = 25^oC$)

Dual-In-Line Plastic Packages (PDIP)



E16.3 (JEDEC MS-001-BB ISSUE D)
16 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8, 10
C	0.008	0.014	0.204	0.355	-
D	0.735	0.775	18.66	19.68	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	16		16		9

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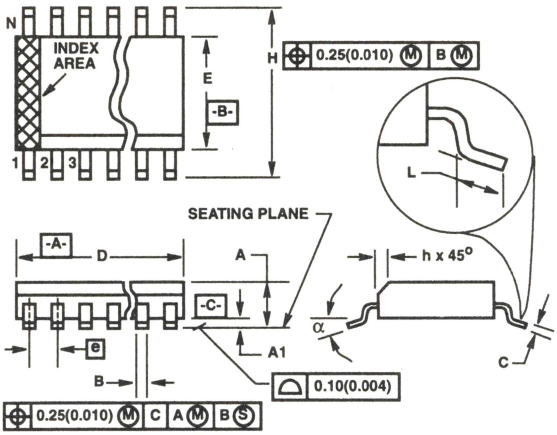
NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and $\boxed{e_A}$ are measured with the leads constrained to be perpendicular to datum $\boxed{-C-}$.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

Small Outline Plastic Packages (SOIC)



M16.15 (JEDEC MS-012-AC ISSUE C)
16 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.3859	0.3937	9.80	10.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	16		16		7
α	0°	8°	0°	8°	-

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NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

HARRIS SEMICONDUCTOR

SP721

Electronic Protection Array for ESD and Over-Voltage Protection

January 1998

Features

- ESD Interface Capability for HBM Standards
  - MIL STD 3015.7 . . . . 15kV
  - IEC 1000-4-2, Direct Discharge,
    Single Input . . . . 4kV (Level 2)
    Two Inputs in Parallel . . . . 8kV (Level 4)
  - IEC 1000-4-2, Air Discharge . . . . 15kV (Level 4)
- High Peak Current Capability
  - IEC 1000-4-5 (8/20μs) . . . . ±3A
  - Single Pulse, 100μs Pulse Width . . . . ±2A
  - Single Pulse, 4μs Pulse Width . . . . ±5A
- Designed to Provide Over-Voltage Protection
  - Single-Ended Voltage Range to . . . . +30V
  - Differential Voltage Range to . . . . ±15V
- Fast Switching . . . . 2ns Risetime
- Low Input Leakages . . . . 1nA at 25°C Typical
- Low Input Capacitance . . . . 3pF Typical
- An Array of 6 SCR/Diode Pairs
- Operating Temperature Range . . . . -40°C to 105°C

Applications

- Microprocessor/Logic Input Protection
- Data Bus Protection
- Analog Device Input Protection
- Voltage Clamp

Description

The SP721 is an array of SCR/Diode biploar structures for ESD and over-voltage protection to sensitive input circuits. The SP721 has 2 protection SCR/Diode device structures per input. There are a total of 6 available inputs that can be used to protect up to 6 external signal or bus lines. Over-voltage protection is from the IN (Pins 1 - 3 and Pins 5 - 7) to V+ or V-.

The SCR structures are designed for fast triggering at a threshold of one $+V_{BE}$ diode threshold above V+ (Pin 8) or a $-V_{BE}$ diode threshold below V- (Pin 4). From an IN input, a clamp to V+ is activated if a transient pulse causes the input to be increased to a voltage level greater than one V_{BE} above V+. A similar clamp to V- is activated if a negative pulse, one V_{BE} less than V-, is applied to an IN input. Standard ESD Human Body Model (HBM) Capability is:

HBM STANDARD	MODE	R	C	ESD (V)
IEC 1000-4-2	Air	330Ω	150pF	>15kV
	Direct	330Ω	150pF	>4kV
	Direct, Dual Pins	330Ω	150pF	>8kV
MIL-STD-3015.7	Direct, In-Circuit	1.5kΩ	100pF	>15kV

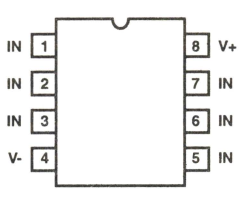
Refer to Figure 1 and Table 1 for further detail. Refer to Application Notes AN9304 and AN9612 for additional information.

Ordering Information

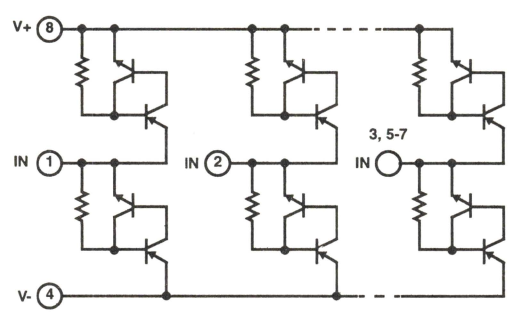
PART NO.	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
SP721AP	-40 to 105	8 Ld PDIP	E8.3
SP721AB	-40 to 105	8 Ld SOIC	M8.15
SP721ABT	-40 to 105	8 Ld SOIC Tape and Reel	M8.15

Pinout

SP721 (PDIP, SOIC)
TOP VIEW



Functional Block Diagram



NOTE: The design of the SP721 SCR/Diode ESD Protection Arrays is covered by Harris patent 4567500.

File Number 3590.5

Absolute Maximum Ratings

Continuous Supply Voltage, (V+) - (V-). . . . . +35V
Forward Peak Current, I_{IN} to V_{CC}, I_{IN} to GND (Refer to Figure 6). . . . . ±2A, 100μs
ESD Ratings and Capability (Figure 1, Table 1)
Load Dump and Reverse Battery (Note 2)

Thermal Information

Thermal Resistance (Typical, Note 1) θ_{JA} (°C/W)
PDIP Package 160
SOIC Package 170
Maximum Storage Temperature Range . . . .-65°C to 150°C
Maximum Junction Temperature (Plastic Package) . . . . 150°C
Maximum Lead Temperature (Soldering 10s) . . . . 300°C
(SOIC Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications T_A = -40°C to 105°C, V_{IN} = 0.5V_{CC} Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage Range, V_{SUPPLY} = [(V+) - (V-)]	V_{SUPPLY}		-	2 to 30	-	V
Forward Voltage Drop						
IN to V-	V_{FWDL}	I_{IN} = 1A (Peak Pulse)	-	2	-	V
IN to V+	V_{FWDH}		-	2	-	V
Input Leakage Current	I_{IN}		-20	5	+20	nA
Quiescent Supply Current	$I_{QUIESCENT}$		-	50	200	nA
Equivalent SCR ON Threshold		Note 3	-	1.1	-	V
Equivalent SCR ON Resistance		V_{FWD}/I_{FWD}; Note 3	-	1	-	Ω
Input Capacitance	C_{IN}		-	3	-	pF
Input Switching Speed	t_{ON}		-	2	-	ns

NOTES:

2. In automotive and battery operated systems, the power supply lines should be externally protected for load dump and reverse battery. When the V+ and V- Pins are connected to the same supply voltage source as the device or control line under protection, a current limiting resistor should be connected in series between the external supply and the SP721 supply pins to limit reverse battery current to within the rated maximum limits. Bypass capacitors of typically 0.01μF or larger from the V+ and V- Pins to ground are recommended.
3. Refer to the Figure 3 graph for definitions of equivalent "SCR ON Threshold" and "SCR ON Resistance". These characteristics are given here for thumb-rule information to determine peak current and dissipation under EOS conditions.

ESD Capability

ESD capability is dependent on the application and defined test standard. The evaluation results for various test standards and methods based on Figure 1 are shown in Table 1.

For the "Modified" MIL-STD-3015.7 condition that is defined as an "in-circuit" method of ESD testing, the V+ and V- pins have a return path to ground and the SP721 ESD capability is typically greater than 15kV from 100pF through 1.5kΩ. By strict definition of MIL-STD-3015.7 using "pin-to-pin" device testing, the ESD voltage capability is greater than 6kV. The MIL-STD-3015.7 results were determined from AT&T ESD Test Lab measurements.

The HBM capability to the IEC 1000-4-2 standard is greater than 15kV for air discharge (Level 4) and greater than 4kV for direct discharge (Level 2). Dual pin capability (2 adjacent pins in parallel) is well in excess of 8kV (Level 4).

For ESD testing of the SP721 to EIAJ IC121 Machine Model (MM) standard, the results are typically better than 1kV from 200pF with no series resistance.

TABLE 1. ESD TEST CONDITIONS

STANDARD	TYPE/MODE	R_D	C_D	$\pm V_D$
MIL-STD-3015.7	Modified HBM	1.5kΩ	100pF	15kV
	Standard HBM	1.5kΩ	100pF	6kV
IEC 1000-4-2	HBM, Air Discharge	330Ω	150pF	15kV
	HBM, Direct Discharge	330Ω	150pF	4kV
	HBM, Direct Discharge, Two Parallel Input Pins	330Ω	150pF	8kV
EIAJ IC121	Machine Model	0kΩ	200pF	1kV

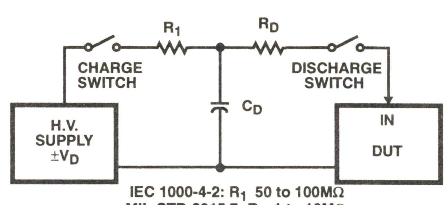


FIGURE 1. ELECTROSTATIC DISCHARGE TEST

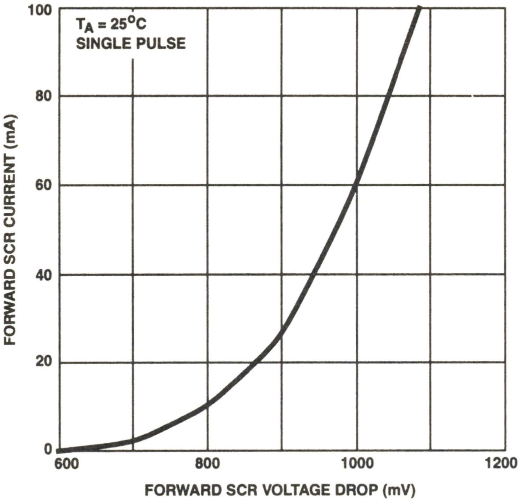


FIGURE 2. LOW CURRENT SCR FORWARD VOLTAGE DROP CURVE

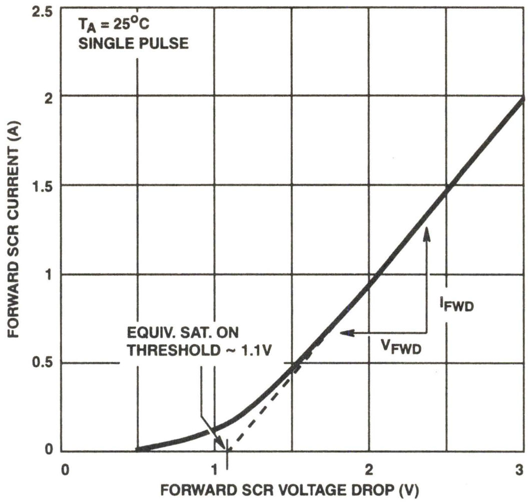


FIGURE 3. HIGH CURRENT SCR FORWARD VOLTAGE DROP CURVE

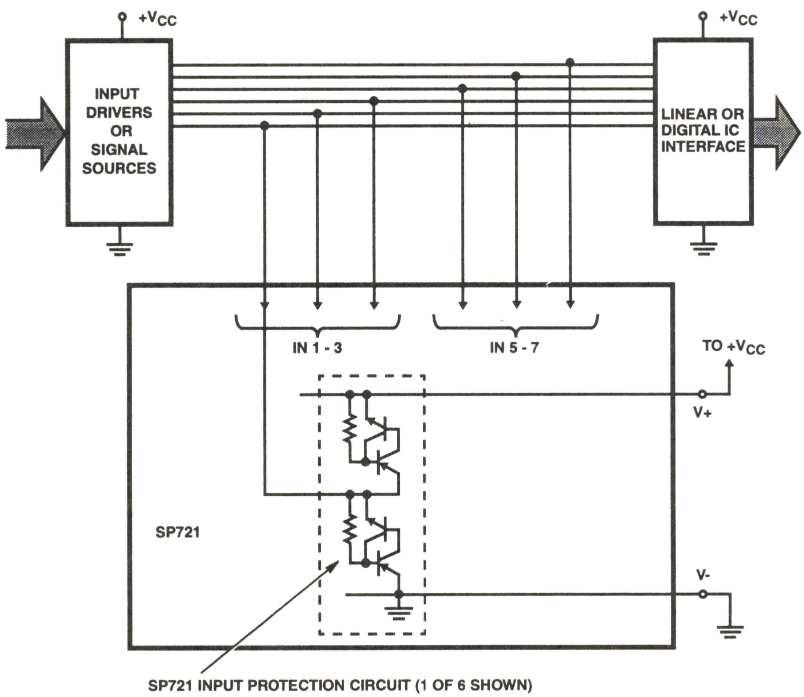


FIGURE 4. TYPICAL APPLICATION OF THE SP721 AS AN INPUT CLAMP FOR OVER-VOLTAGE, GREATER THAN $1V_{BE}$ ABOVE V+ OR LESS THAN $-1V_{BE}$ BELOW V-

6

INTEGRATED PROTECTION CKTs

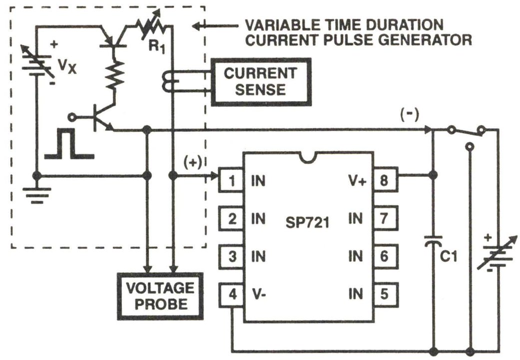
Peak Transient Current Capability of the SP721

The peak transient current capability rises sharply as the width of the current pulse narrows. Destructive testing was done to fully evaluate the SP721's ability to withstand a wide range of peak current pulses vs time. The circuit used to generate current pulses is shown in Figure 5.

The test circuit of Figure 5 is shown with a positive pulse input. For a negative pulse input, the (-) current pulse input goes to an SP721 'IN' input pin and the (+) current pulse input goes to the SP721 V- pin. The V+ to V- supply of the SP721 must be allowed to float. (i.e., It is not tied to the ground reference of the current pulse generator.) Figure 6 shows the point of over-stress as defined by increased leakage in excess of the data sheet published limits.

The maximum peak input current capability is dependent on the ambient temperature, improving as the temperature is reduced. Peak current curves are shown for ambient temperatures of 25°C and 105°C and a 15V power supply condition. The safe operating range of the transient peak current should be limited to no more than 75% of the measured over-stress level for any given pulse width as shown in the curves of Figure 6.

Note that adjacent input pins of the SP721 may be paralleled to improve current (and ESD) capability. The sustained peak current capability is increased to nearly twice that of a single pin.



R_1 ~ 10Ω TYPICAL
V_X ADJ. 10V/A TYPICAL
C1 ~ 100µF

FIGURE 5. TYPICAL SP721 PEAK CURRENT TEST CIRCUIT WITH A VARIABLE PULSE WIDTH INPUT

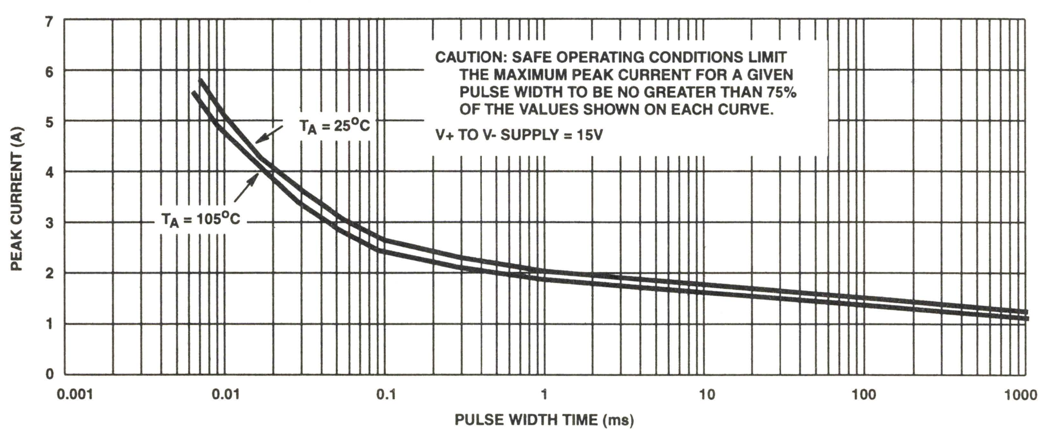
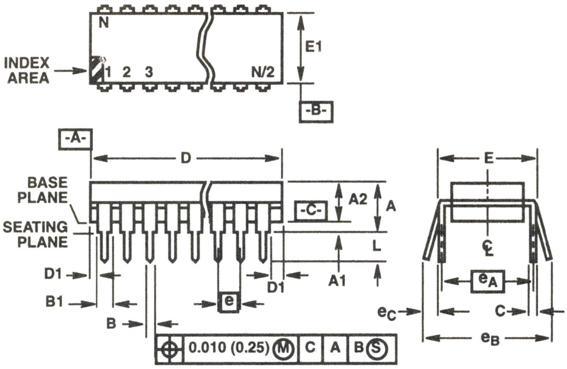


FIGURE 6. SP721 TYPICAL SINGLE PULSE PEAK CURRENT CURVES SHOWING THE MEASURED POINT OF OVER-STRESS IN AMPERES vs PULSE WIDTH TIME IN MILLISECONDS

Dual-In-Line Plastic Packages (PDIP)



NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and $\boxed{e_A}$ are measured with the leads constrained to be perpendicular to datum $\boxed{\text{-C-}}$.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E8.3 (JEDEC MS-001-BA ISSUE D)
8 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8, 10
C	0.008	0.014	0.204	0.355	-
D	0.355	0.400	9.01	10.16	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	8		8		9

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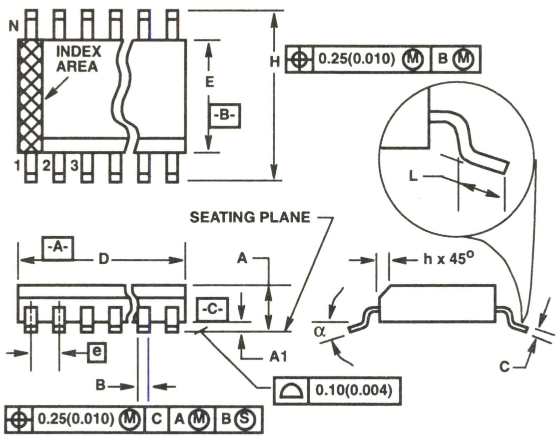
Small Outline Plastic Packages (SOIC)



NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M8.15 (JEDEC MS-012-AA ISSUE C)
8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.1890	0.1968	4.80	5.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	8		8		7
α	0°	8°	0°	8°	-

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HARRIS SEMICONDUCTOR

SP723

Electronic Protection Array for ESD and Over-Voltage Protection

January 1998

Features

- ESD Interface per HBM Standards
  - IEC 1000-4-2, Direct Discharge ...... 8kV (Level 4)
  - IEC 1000-4-2, Air Discharge......... 15kV (Level 4)
  - MIL-STD-3015.7 .... 25kV
- Peak Current Capability
  - IEC 1000-4-5 8/20μs Peak Pulse Current .... ±7A
  - Single Transient Pulse, 100μs Pulse Width..... ±4A
- Designed to Provide Over-Voltage Protection
  - Single-Ended Voltage Range to .... +30V
  - Differential Voltage Range to .... ±15V
- Fast Switching .... 2ns Risetime
- Low Input Leakages .... 2nA at 25°C Typical
- Low Input Capacitance .... 5pF Typical
- An Array of 6 SCR/Diode Pairs
- Operating Temperature Range .... -40°C to 105°C

Applications

- Microprocessor/Logic Input Protection
- Data Bus Protection
- Analog Device Input Protection
- Voltage Clamp

Description

The SP723 is an array of SCR/Diode bipolar structures for ESD and over-voltage protection to sensitive input circuits. The SP723 has 2 protection SCR/Diode device structures per input. There are a total of 6 available inputs that can be used to protect up to 6 external signal or bus lines. Over-voltage protection is from the IN (Pins 1 - 3 and Pins 5 - 7) to V+ or V-.

The SCR structures are designed for fast triggering at a threshold of one $+V_{BE}$ diode threshold above V+ (Pin 8) or a $-V_{BE}$ diode threshold below V- (Pin 4). From an IN input, a clamp to V+ is activated if a transient pulse causes the input to be increased to a voltage level greater than one V_{BE} above V+. A similar clamp to V- is activated if a negative pulse, one V_{BE} less than V-, is applied to an IN input.

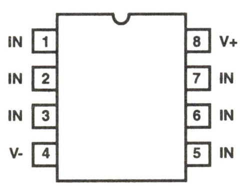
The SP723 is similar to the SP720 and SP721. Refer to Application Note AN9304 and AN9612 for further detail.

Ordering Information

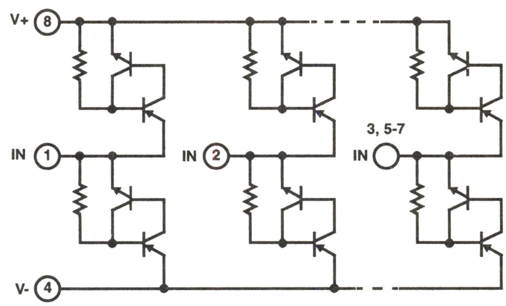
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
SP723AP	-40 to 105	8 Ld PDIP	E8.3
SP723AB	-40 to 105	8 Ld SOIC	M8.15
SP723ABT	-40 to 105	8 Ld SOIC Tape and Reel	M8.15

Pinout

SP723
(PDIP, SOIC)
TOP VIEW



Functional Diagram



NOTE: The design of the SP723 SCR/Diode ESD Protection Arrays is covered by Harris patent 4567500.

File Number 4145.2

Absolute Maximum Ratings

Continuous Supply Voltage, (V+) - (V-) . . . . +35V
Forward Peak Current, I_{IN} to V_{CC}, I_{IN} to GND
(Refer to Figure 6) . . . . ±4A, 100µs
Peak Pulse Current, 8/20µs . . . . ±7A
ESD Ratings and Capability (Figure 1, Table 1)
Load Dump and Reverse Battery (Note 2)

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)
PDIP Package	160
SOIC Package	170

Storage Temperature Range . . . . -65°C to 150°C
Maximum Junction Temperature . . . . 150°C
Lead Temperature (Soldering 10s) . . . . 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

T_A = -40°C to 105°C, V_{IN} = 0.5V_{CC}, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage Range, V_{SUPPLY} = [(V+) - (V-)]	V_{SUPPLY}		-	2 to 30	-	V
Forward Voltage Drop IN to V-	V_{FWDL}	I_{IN} = 2A (Peak Pulse)	-	2	-	V
IN to V+	V_{FWDH}		-	2	-	V
Input Leakage Current	I_{IN}		-20	5	+20	nA
Quiescent Supply Current	$I_{QUIESCENT}$		-	50	200	nA
Equivalent SCR ON Threshold		Note 3	-	1.1	-	V
Equivalent SCR ON Resistance		V_{FWD}/I_{FWD} ; Note 3	-	0.5	-	Ω
Input Capacitance	C_{IN}		-	5	-	pF
Input Switching Speed	t_{ON}		-	2	-	ns

NOTES:

2. In automotive and battery operated systems, the power supply lines should be externally protected for load dump and reverse battery. When the V+ and V- Pins are connected to the same supply voltage source as the device or control line under protection, a current limiting resistor should be connected in series between the external supply and the SP723 supply pins to limit reverse battery current to within the rated maximum limits. Bypass capacitors of typically 0.01µF or larger from the V+ and V- Pins to ground are recommended.
3. Refer to the Figure 3 graph for definitions of equivalent "SCR ON Threshold" and "SCR ON Resistance". These characteristics are given here for thumb-rule information to determine peak current and dissipation under EOS conditions.

ESD Capability

ESD capability is dependent on the application and defined test standard. The evaluation results for various test standards and methods based on Figure 1 are shown in Table 1.

The SP723 has a Level 4 HBM capability when tested as a device to the IEC 1000-4-2 standard. Level 4 specifies a required capability greater than 8kV for direct discharge and greater than 15kV for air discharge.

For the "Modified" MIL-STD-3015.7 condition that is defined as an "in-circuit" method of ESD testing, the V+ and V- pins have a return path to ground and the SP723 ESD capability is typically greater than 25kV from 100pF through 1.5kΩ. By strict definition of MIL-STD-3015.7 using "pin-to-pin" device testing, the ESD voltage capability is greater than 10kV.

For the SP723 EIAJ IC121 Machine Model (MM) standard, the ESD capability is typically greater than 2kV from 200pF with no series resistance.

TABLE 1. ESD TEST CONDITIONS

STANDARD	TYPE/MODE	R_D	C_D	$\pm V_D$
IEC 1000-4-2 (Level 4)	HBM, Air Discharge	330Ω	150pF	15kV
	HBM, Direct Discharge	330Ω	150pF	8kV
MIL-STD-3015.7	Modified HBM	1.5kΩ	100pF	25kV
	Standard HBM	1.5kΩ	100pF	10kV
EIAJ IC121	Machine Model	0kΩ	200pF	2kV

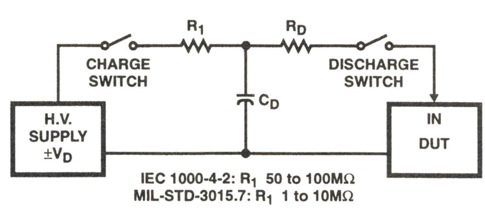


FIGURE 1. ELECTROSTATIC DISCHARGE TEST

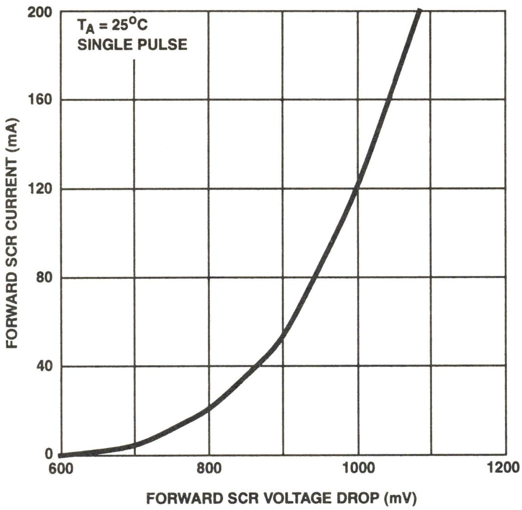


FIGURE 2. LOW CURRENT SCR FORWARD VOLTAGE DROP CURVE

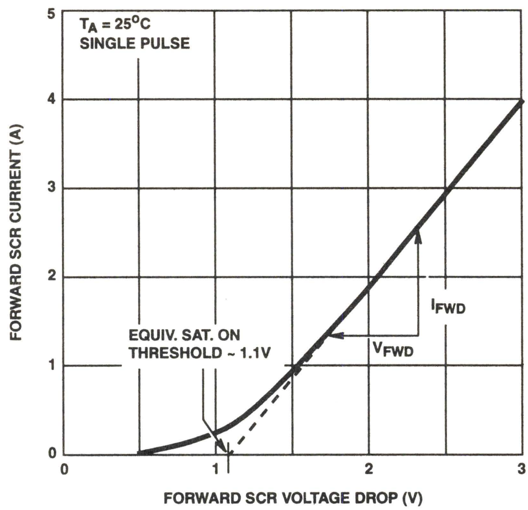


FIGURE 3. HIGH CURRENT SCR FORWARD VOLTAGE DROP CURVE

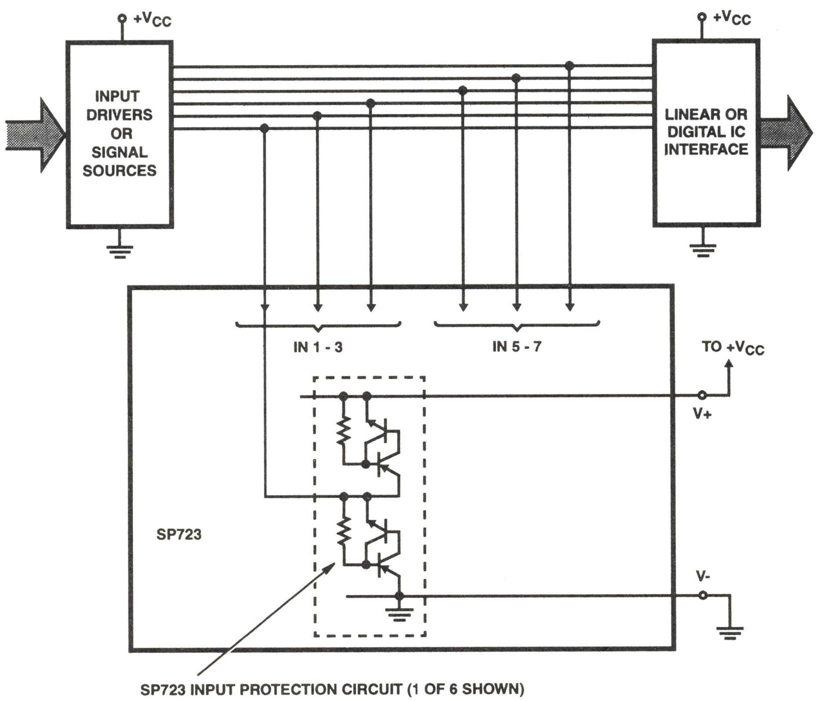


FIGURE 4. TYPICAL APPLICATION OF THE SP723 AS AN INPUT CLAMP FOR OVER-VOLTAGE, GREATER THAN $1V_{BE}$ ABOVE V+ OR LESS THAN $-1V_{BE}$ BELOW V-

6

INTEGRATED PROTECTION CKTs

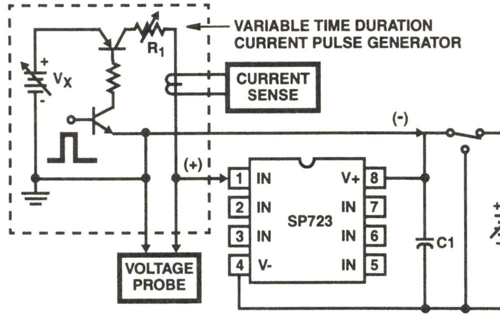
Peak Transient Current Capability of the SP723

The peak transient current capability rises sharply as the width of the current pulse narrows. Destructive testing was done to fully evaluate the SP723's ability to withstand a wide range of peak current pulses vs time. The circuit used to generate current pulses is shown in Figure 5.

The test circuit of Figure 5 is shown with a positive pulse input. For a negative pulse input, the (-) current pulse input goes to an SP723 'IN' input pin and the (+) current pulse input goes to the SP723 V- pin. The V+ to V- supply of the SP723 must be allowed to float. (i.e. It is not tied to the ground reference of the current pulse generator.) Figure 6 shows the point of overstress as defined by increased leakage in excess of the data sheet published limits.

The maximum peak input current capability is dependent on the ambient temperature, improving as the temperature is reduced. Peak current curves are shown for ambient temperatures of 25°C and 105°C and a 15V power supply condition. The safe operating range of the transient peak current should be limited to no more than 75% of the measured overstress level for any given pulse width as shown in the curves of Figure 6.

Note that adjacent input pins of the SP723 may be paralleled to improve current (and ESD) capability. The sustained peak current capability is increased to nearly twice that of a single pin.



R_1 ~ 10Ω TYPICAL
V_X ADJ. 10V/A TYPICAL
C1 ~ 100μF

FIGURE 5. TYPICAL SP723 PEAK CURRENT TEST CIRCUIT WITH A VARIABLE PULSE WIDTH INPUT

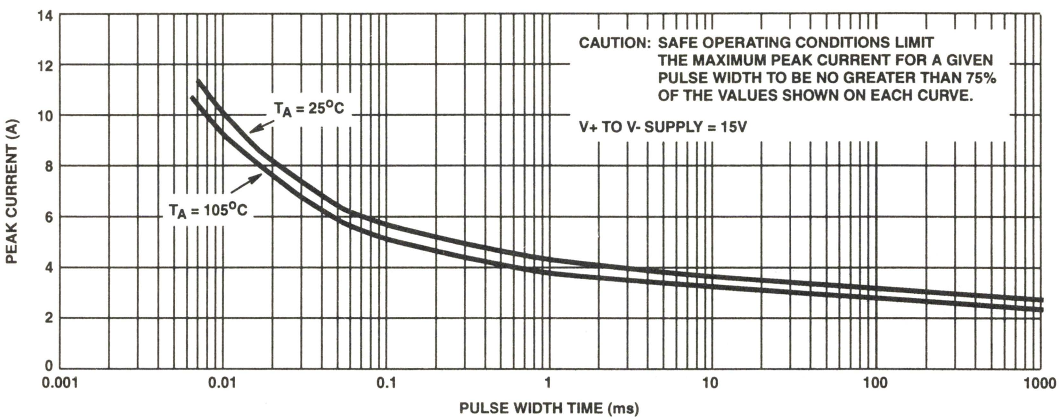
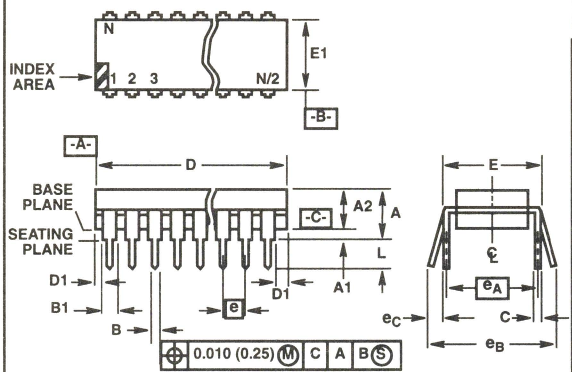


FIGURE 6. SP723 TYPICAL SINGLE PULSE PEAK CURRENT CURVES SHOWING THE MEASURED POINT OF OVERSTRESS IN AMPERES vs PULSE WIDTH TIME IN MILLISECONDS

Dual-In-Line Plastic Packages (PDIP)



E8.3 (JEDEC MS-001-BA ISSUE D)
8 LEAD DUAL-IN-LINE PLASTIC PACKAGE

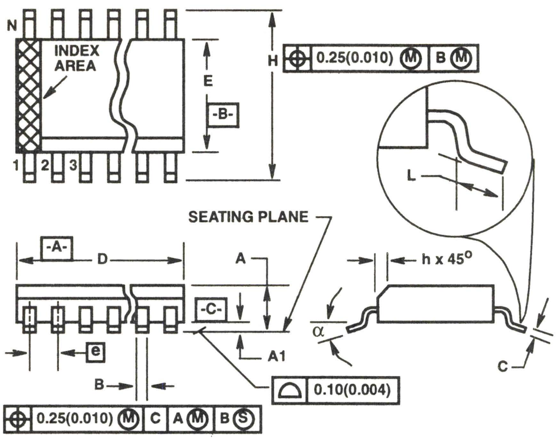
SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8, 10
C	0.008	0.014	0.204	0.355	-
D	0.355	0.400	9.01	10.16	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	8		8		9

Rev. 0 12/93

NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and $\boxed{e_A}$ are measured with the leads constrained to be perpendicular to datum $\boxed{-C-}$.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

Small Outline Plastic Packages (SOIC)



M8.15 (JEDEC MS-012-AA ISSUE C)
8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.1890	0.1968	4.80	5.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	8		8		7
α	0°	8°	0°	8°	-

Rev. 0 12/93

NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

TVS 7

GAS DISCHARGE TUBE PRODUCTS

Gas Discharge Tube Products Overview

The characteristics of Gas Discharge Tube technology such as high surge current capability and low capacitance have made GDT suppression devices ideally suited to a variety of applications as listed in the Selection Guide table below. Harris GDTs range in Breakdown Voltage values from 75V to 8.5kV in five distinct series. The HG/HG2 Series offers the broadest breakdown voltage range – $75V_{DC}$ to $1000V_{DC}$. Available with or without leads, these devices encompass numerous applications such as CATV, communication, industrial instrumentation and power supplies.The HPMT3 Series are three electrode versions specifically intended to offer balanced protection of telephone line service and associated equipment.

The HAC Series is designed with follow current ratings specifically suitable for many AC line transient suppression applications and provide peak surge current capability up to 10kA. The High Voltage versions of the HG3 Series find usage in power supplies, laboratory and industrial equipment.

The HG2-SN and HG3 Series feature non-radioactive materials.

GDTs are also often combined with MOVs in order to take advantage of the attributes of each. This and other GDT topics can be found in the Application Notes compiled in Section 11.

Transient Voltage Suppressor Device Selection Guide

MARKET SEGMENT	TYPICAL APPLICATIONS AND CIRCUITS EXAMPLES	DEVICE FAMILY OR SERIES	DATA BOOK SECTION	TECHNOLOGY	SURFACE MOUNT PRODUCT?
Low Voltage, Board Level Products	• Hand-Held/Portable Devices • EDP • Computer • I/O Port and Interfaces • Controllers • Instrumentation • Remote Sensors • Medical Electronics, etc.	CH	4	MOV	✔
		MA, ZA, RA	4	MOV	
		ML, MLE	5	Multilayer Suppressor	✔
		SP72X	6	SCR/Diode Array	✔ †
AC Line, TVSS Products	• UPS • AC Panels • AC Power Taps • TVSS Devices • AC Appliance/Controls • Power Meters • Power Supplies • Circuit Breakers • Consumer Electronics	UltraMOV™, "C" III, LA, HA, RA	4	MOV	
		CH	4	MOV	✔
		GDT	**7**	**Gas Discharge Tube**	
Automotive Electronics	• ABS • EEC • Instrument Cluster • Air Bag • Window Control • Wiper Modules • Multiplex Bus • EFI	CH	4	MOV	✔
		ZA	4	MOV	
		AUML, ML	5	Multilayer Suppressor	✔
		SP72X	6	SCR/Diode Array	✔ †
Telecommunications Products	• Cellular/Cordless Phone • Modems • Secondary Phone Line Protectors • Data Line Connectors • Repeaters • Line Cards	CH	4	MOV	✔
		CP, CS, ZA	4	MOV	
		ML, MLE	5	Multilayer Suppressor	✔
		SP72X	6	SCR/Diode Array	✔ †
		GDT	**7**	**Gas Discharge Tube**	
		Surgector	8	Thyristor/Zener	
Industrial, High Energy AC Products	• High Current Relays • Solenoids • Motor Drives • AC Distribution Panels • Robotics • Large Motors	DA/DB, BA/BB, CA, HA, NA, PA	4	MOV	
		GDT	**7**	**Gas Discharge Tube**	
Arrester Products	• Lightning Arrester Assemblies for High Voltage AC Power Distribution Lines and Utility Transformers	AS	9	MOV	

†Available in both surface mount and through-hole packages.

HARRIS SEMICONDUCTOR

HAC Series

January 1998

Two Electrode AC Line Protectors

Features

- High AC Follow-On Current Capability . . . . >300A (Peak)
- Small Size
- Rugged Ceramic Metal Construction
- Low Capacitance . . . . <1pF
- Available With or Without Leads
- Available in Tape and Reel Packaging
- Agency Listings
  - UL1449 Recognized (HAC120)
  - Meets IEEE C62.41-1991
  - CSA Approved

Applications

- Long Branch Circuits
  - AC Wall Outlet
- Short Branch Circuits
  - Breaker Box, Computer, etc.
- Power Supplies
- Test Equipment
- Submersible Pumps
- Medical Electronics

Description

Harris Semiconductor's two electrode AC Line Protectors are designed for a high degree of surge suppression in AC line applications at low cost. The two models, HAC120 and HAC240, are designed for use with 120VAC and 240VAC lines, respectively. These devices are able to extinguish in the presence of AC follow-on currents of at least 300A; therefore, a series current-limiting device is usually not needed to ensure turn-off. AC Line Protectors function as switches and therefore handle currents that far surpass other types of transient voltage protection.

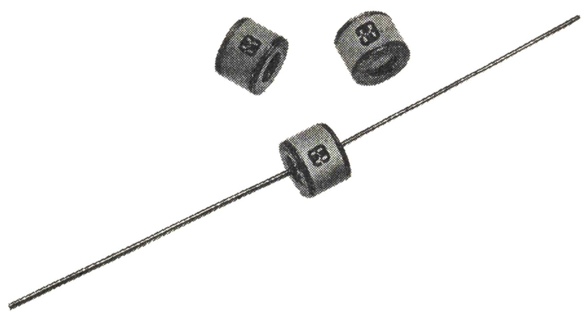
Ordering Information

PART NUMBER	BRAND
HAC120	HAC120
HAC120L	HAC120L
HAC240	HAC240
HAC240L	HAC240L

NOTES:

1. L means leads; see Ordering Nomenclature.
2. When ordering use the entire part number. Add the suffix T to obtain the variant in tape and reel.

Packaging



Absolute Maximum Ratings For ratings of individual members of a series, see device ratings and specifications table.

		HAC SERIES	UNITS
Operating Ambient Temperature Range	T_A	-40 to 125	^oC
Storage Temperature Range	T_{STG}	-40 to 125	^oC

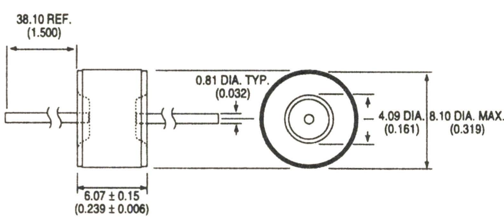
Electrical Specifications T_C at 25^{o}C Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	HAC120, HAC120L			HAC240, HAC240L			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
DC Breakdown	V_{BD}	500V/s	225	-	-	425	-	-	V
Impulse Breakdown	V_{bd}	100V/µs	-	-	700	-	-	800	V
Insulation Resistance	IR	100V	10^{10}	-	-	10^{10}	-	-	Ω
Capacitance	C	1MHz	-	-	1.0	-	-	1.0	pF
Arc Voltage	V_{ARC}	I = 5A Min	-	20	-	-	20	-	V
LIFE RATINGS (Note 1)									
Max Current Surge		10kA (8/20µs)	4	-	-	4	-	-	Surges
AC Follow-On Current (Peak)		1/2 cycle at 60Hz	-	-	300	-	-	300	A

NOTE:

1. End-of-Life limits:
DC: same as minimum initial DC breakdown voltage limit; Impulse: less than 150% of initial impulse breakdown voltage limit.

Mechanical Dimensions



Ordering Nomenclature

A complete part number is represented by the digits below. For example, HAC120 is a non-leaded 120VAC device, HAC240L is a leaded 240VAC device, and HAC240LT is a leaded 240VAC device on tape-and-reel per EIA standard RS-296-D.

HAC GAS DISCHARGE TUBE TYPES

HAC 120 X X

DEVICE FAMILY
Harris HAC Series

AC LINE VOLTAGE
120: 120V
240: 240V

PACKAGING OPTIONS
T: Tape and Reel
Blank: Bulk

LEAD OPTIONS
L: Leads
Blank: No Leads

HARRIS SEMICONDUCTOR

HG Series, HG2 Series

September 1997

Two Electrode Surge Arrestors

Features

- Small Size
- Rugged Ceramic-Metal Construction
- Low Capacitance . . . . <1pF
- Non Radioactive 600-1000 V
- Available With or Without Leads
- Available in Tape-and-Reel Packaging
- Agency Listings
  - UL 1449 recognition
  - Meets REA PE-80

Applications

- Communication Lines
- CATV Equipment
- Test Equipment
- Data Lines
- Power Supplies
- Instrumentation Circuits
- Medical Electronics

Description

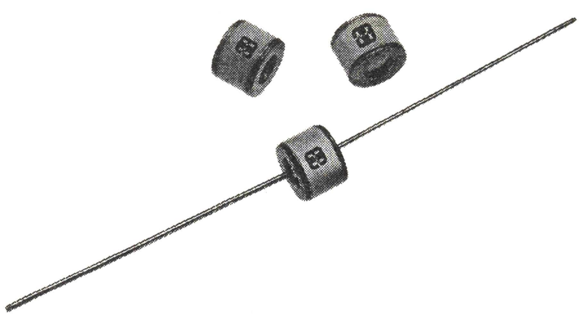
Harris Semiconductor's two electrode HG/HG2 Gas Discharge Tubes (GDTs) are designed for a high degree of surge protection at a low cost. The HG Series (75-110V) is primarily used for protection of test and communication equipment in which low voltage limits and extremely low arc voltages are required.The HG2 Series (145V-1000V) is used for the protection of test and communication equipment for which higher voltage limits and holdover voltages are necessary. GDTs function as switches and therefore handle currents that far surpass other types of transient voltage protection.

Ordering Information

PART NUMBER	BRAND
HG75	HG75
HG75L	HG75L
HG90	HG90
HG90L	HG90L
HG110	HG110
HG110L	HG110L
HG2-145	HG2-145
HG2-145L	HG2-145L
HG2-230	HG2-230
HG2-230L	HG2-230L
HG2-250	HG2-250
HG2-250L	HG2-250L
HG2-300	HG2-300
HG2-300L	HG2-300L
HG2-350	HG2-350
HG2-350L	HG2-350L
HG2-470	HG2-470
HG2-470L	HG2-470L
HG2-600	HG2-600
HG2-600L	HG2-600L
HG2-800	HG2-800
HG2-800L	HG2-800L
HG2-1000	HG2-1000
HG2-1000L	HG2-1000L

NOTES:
1. L means leads; see Ordering Nomenclature.
2. When ordering use the entire part number. Add the suffix T to obtain the variant in tape and reel.

Packaging



Absolute Maximum Ratings For ratings of individual members of a series, see device ratings and specifications table.

		HG, HG2 SERIES	UNITS
Operating Ambient Temperature Range	T_A	-40 to 125	^oC
Storage Temperature Range	T_{STG}	-40 to 125	^oC

Electrical Specifications T_C at 25^{o}C Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	HG75			HG90			HG110			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
DC Breakdown	V_{BD}	500V/s	60	75	90	72	90	108	88	110	132	V
Impulse Breakdown	V_{bd}	100V/µs	-	-	400	-	-	400	-	-	450	V
Insulation Resistance	IR	50V	10^{10}	-	-	10^{10}	-	-	10^{10}	-	-	Ω
Capacitance	C	1MHz	-	-	1	-	-	1	-	-	1	pF
Arc Voltage	V_{ARC}	I = 5A Min	-	10	-	-	10	-	-	10	-	V
LIFE RATINGS (Note 1)												
Surge Life	-	500A (10/1000µs)	1000	-	-	1000	-	-	1000	-	-	Surges
Max Current Surge	-	20kA (8/20µs)	5	-	-	5	-	-	5	-	-	Surges
AC Current	-	10x 1s at 60Hz	-	-	20	-	-		20	-	-	A
DC Holdover Voltage	-	Per REA PE-80, 0.2A	-	55	-	-	65	-	-	80	-	V

Electrical Specifications T_C at 25^{o}C Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	HG2-145			HG2-230			HG2-250			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
DC Breakdown	V_{BD}	500V/s	116	145	174	195	230	265	213	250	288	V
Impulse Breakdown	V_{bd}	100V/µs	-	-	500	-	-	600	-	-	625	V
Insulation Resistance	IR	100V	10^{10}	-	-	10^{10}	-	-	10^{10}	-	-	Ω
Capacitance	C	1MHz	-	-	1	-	-	1	-	-	1	pF
Arc Voltage	V_{ARC}	I = 5A Min	-	15	-	-	15	-	-	15	-	V
LIFE RATINGS (Note 1)												
Surge Life	-	500A (10/1000µs)	1000	-	-	1000	-	-	1000	-	-	Surges
Max Current Surge	-	20kA (8/20µs)	5	-	-	5	-	-	5	-	-	Surges
AC Current	-	10x 1s at 60Hz	-	-	20	-	-	20	-	-	20	A
AC Follow-On Peak Current	-	1/2 Cycle at 60Hz	-	-	20	-	-	20	-	-	20	A
DC Holdover Voltage	-	Per REA PE-80, 0.2A	-	90	-	-	150	-	-	150	-	V

Electrical Specifications T_C at 25^{o}C Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	HG2-300			HG2-350			HG2-470			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
DC Breakdown	V_{BD}	500V/s	255	300	345	297	350	403	400	470	540	V
Impulse Breakdown	V_{bd}	100V/µs	-	-	700	-	-	750	-	-	850	V
Insulation Resistance	IR	100V	10^{10}	-	-	10^{10}	-	-	10^{10}	-	-	Ω
Capacitance	C	1MHz	-	-	1	-	-	1	-	-	1	pF
Arc Voltage	V_{ARC}	I = 5A Min	-	15	-	-	15	-	-	15	-	V
LIFE RATINGS (Note 1)												
Surge Life	-	500A (10/1000µs)	1000	-	-	1000	-	-	1000	-	-	Surges
Max Current Surge	-	20kA (8/20µs)	5	-	-	5	-	-	5	-	-	Surges
AC Current	-	10x 1s at 60Hz	-	-	20	-	-	20	-	-	20	A

Electrical Specifications T_C at 25°C Unless Otherwise Specified **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	HG2-300 MIN	HG2-300 TYP	HG2-300 MAX	HG2-350 MIN	HG2-350 TYP	HG2-350 MAX	HG2-470 MIN	HG2-470 TYP	HG2-470 MAX	UNITS
AC Follow-On Peak Current	-	1/2 Cycle at 60Hz	-	-	20	-	-	20	-	-	20	A
DC Holdover Voltage	-	Per REA PE-80, 0.2A	-	150	-	-	150	-	-	150	-	V

Electrical Specifications T_C at 25°C Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	HG2-600 MIN	HG2-600 TYP	HG2-600 MAX	HG2-800 MIN	HG2-800 TYP	HG2-800 MAX	HG2-1000 MIN	HG2-1000 TYP	HG2-1000 MAX	UNITS
DC Breakdown	V_{BD}	500V/s	510	600	690	680	800	920	850	1000	1150	V
Impulse Breakdown	V_{bd}	100V/μs	-	-	1000	-	-	1200	-	-	1500	V
Insulation Resistance	IR	100V	10^{10}	-	-	10^{10}	-	-	10^{10}	-	-	Ω
Capacitance	C	1MHz	-	-	1	-	-	1	-	-	1	pF
Arc Voltage	V_{ARC}	I = 5A Min	-	15	-	-	15	-	-	15	-	V
LIFE RATINGS (Note 1)												
Surge Life	-	500A (10/1000μs)	1000	-	-	1000	-	-	1000	-	-	Surges
Max Current Surge	-	20kA (8/20μs)	10	-	-	10	-	-	10	-	-	Surges
AC Current	-	10x 1s at 60Hz	-	-	20	-	-	20	-	-	20	A
AC Follow-On Peak Current	-	1/2 Cycle at 60Hz	-	-	20	-	-	20	-	-	20	A
DC Holdover Voltage	-	Per REA PE-80, 0.2A	-	150	-	-	150	-	-	150	-	V

NOTE:

1. End-of-Life limits:
   DC: 50% of minimum initial DC breakdown voltage limit to150% of maximum initial DC breakdown voltage limit.
   Impulse: less that 150% of initial impulse breakdown voltage limit.

Typical Performance Curves

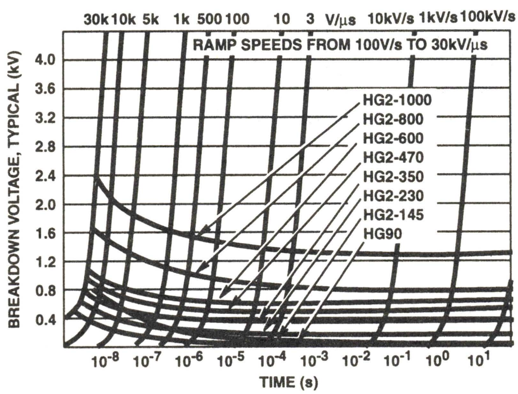


FIGURE 1. HG, HG2 SERIES VOLTAGE BREAKDOWN

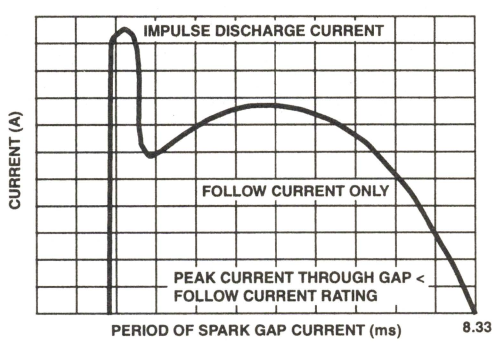


FIGURE 2. HG, HG2 FOLLOW-ON CURRENT

Typical Performance Curves (Continued)

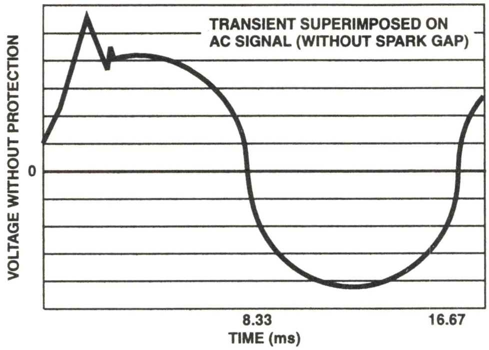


FIGURE 3. LINE VOLTAGE - NO PROTECTION

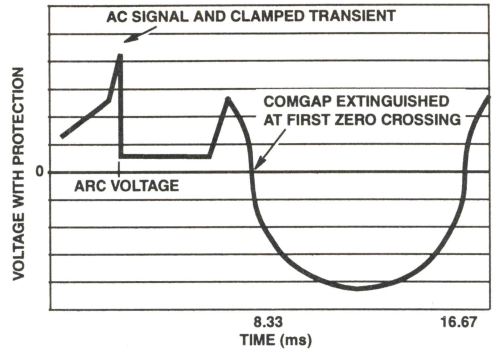
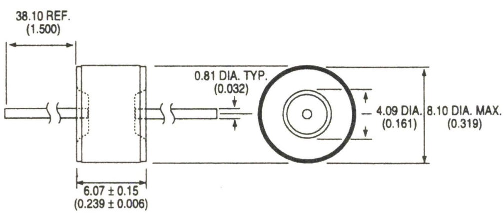


FIGURE 4. LINE VOLTAGE - WITH PROTECTION

Mechanical Dimensions



Ordering Nomenclature

A complete part number is represented by the digits below. For example, HG75 is a non-leaded 75V device, HG2-230L is a leaded 230V Device, and the HG2-800LT is a leaded 800V device on tape and reel per EIA standard RS-296-D.

HG, HG2 GAS DISCHARGE TUBE TYPES

HG 90 X X
HG2-300 X X

DEVICE FAMILY
Harris HG, HG2 Series

BREAKDOWN VOLTAGE

HG Types	250: 250V
75: 75V	300: 300V
90: 90V	350: 350V
110: 110V	470: 470V
HG2 Types	600: 600V
145: 145V	800: 800V
230: 230V	1000: 1000V

LEAD OPTIONS
L: Leads
Blank: No Leads

PACKAGING OPTIONS
T: Tape and Reel
Blank: Bulk

HARRIS SEMICONDUCTOR

HG2-SN Series

January 1998

Two Electrode Non-Radioactive Arresters

Features

- Small Size
- Rugged Ceramic-Metal Construction
- Non-Radioactive
- Low Capacitance .... <1pF
- Available in Tape-and-Reel Packaging
- Available With or Without Leads
- Agency Listings
  - Meets REA PE-80
  - Designed to Meet CCITT-K12

Applications

- Communication Lines
- CATV Equipment
- Test Equipment
- Power Supplies
- Medical Electronics
- Instrumentation Circuits

Description

Harris Semiconductor's two electrode non-radioactive HG2-SN Gas Discharge Tubes (GDTs) are designed for use in surge protection applications for which the radioactive isotope used in the standard HG/HG2 Series is not desired. The gas-filled, rugged ceramic-metal construction of GDTs makes them well suited to adverse environments. GDTs function as switches and therefore handle currents that far surpass other types of transient voltage protection.

Ordering Information

PART NUMBER	BRAND
HG2-230SN	HG2-230SN
HG2-230LSN	HG2-230LSN
HG2-250SN	HG2-250SN
HG2-250LSN	HG2-250LSN
HG2-300SN	HG2-300SN
HG2-300LSN	HG2-300LSN
HG2-350SN	HG2-350SN
HG2-350LSN	HG2-350LSN
HG2-470SN	HG2-470SN
HG2-470LSN	HG2-470LSN

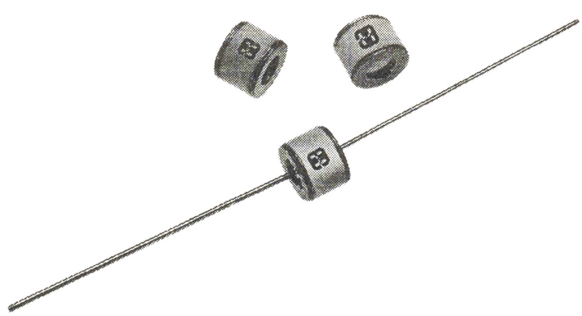
NOTES:

1. L means leads; see Ordering Nomenclature.
2. When ordering use the entire part number. Add the suffix T to obtain the variant in tape and reel.

7

GAS DISCHARGE TUBES

Packaging



Absolute Maximum Ratings For ratings of individual members of a series, see device ratings and specifications table.

		HG2-SN SERIES	UNITS
Operating Ambient Temperature Range	T_A	-40 to 125	^oC
Storage Temperature Range	T_{STG}	-40 to 125	^oC

Electrical Specifications T_C at 25^{o}C Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	HG2-230SN, HG2-230LSN			HG2-250SN, HG2-250LSN			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
DC Breakdown	V_{BD}	500V/s	184	230	276	200	250	300	V
Impulse Breakdown	V_{bd}	100V/µs	-	-	600	-	-	600	V
Insulation Resistance	IR	100VS	10^9	-	-	10^9	-	-	Ω
Capacitance	C	1MHz	-	-	1	-	-	1	pF
Arc Voltage	V_{ARC}	I = 5A Min	-	10	-	-	10	-	V
LIFE RATINGS (Note 1)									
Surge Life	-	500A (10/1000µs)	400	-	-	400	-	-	Surges
Max Current Surge	-	10kA (8/20µs)	10	-	-	10	-	-	Surges
AC Current	-	10x 1s at 60Hz	-	-	20	-	-	20	A
AC Follow-On Current (Peak)	-	1/2 Cycle at 60Hz	-	-	20	-	-	20	A
DC Holdover Voltage	-	Per REA PE-80, 0.2A	-	150	-	-	150	-	V

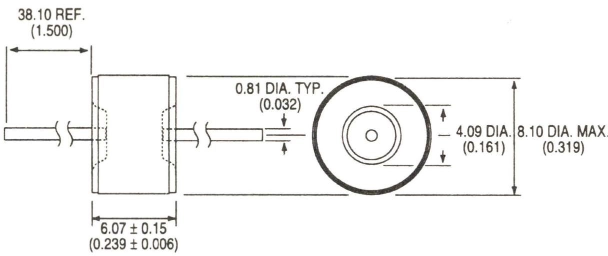
Electrical Specifications T_C at 25^{o}C Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	HG2-300SN, HG2-300LSN			HG2-350SN, HG2-350LSN			HG2-470SN, HG2-470LSN			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
DC Breakdown	V_{BD}	500V/s	240	300	360	280	350	420	376	470	564	V
Impulse Breakdown	V_{bd}	100V/µs	-	-	700	-	-	750	-	-	850	V
Insulation Resistance	IR	100V	10^9	-	-	10^9	-	-	10^9	-	-	Ω
Capacitance	C	1MHz	-	-	1	-	-	1	-	-	1	pF
Arc Voltage	V_{ARC}	I = 5A Min	-	10	-	-	10	-	-	10	-	V
LIFE RATINGS (Note 1)												
Surge Life	-	500A (10/1000µs)	400	-	-	400	-	-	400	-	-	Surges
Max Current Surge	-	10kA (8/20µs)	10	-	-	10	-	-	10	-	-	Surges
AC Current	-	10x 1s at 60Hz	-	-	20	-	-	20	-	-	20	A
AC Follow-On Current (Peak)	-	1/2 Cycle at 60Hz	-	-	20	-	-	20	-	-	20	A
DC Holdover Voltage	-	Per REA PE-80, 0.2A	-	150	-	-	150	-	-	150	-	V

NOTE:

1. End-of-Life limits:
   DC: 50% of minimum initial DC breakdown voltage limit to150% of maximum initial DC breakdown voltage limit.
   Impulse: less that 150% of initial impulse breakdown voltage limit.

Mechanical Dimensions



Ordering Nomenclature

A complete part number is represented by the digits below. For example, HG2-230SN is a non-leaded 230V device, HG2-470LSN is a leaded 470V device, and HG2-300LSNT is a leaded 300V device on tape-and-reel per EIA standard RS-296-D.

HG2-SN GAS DISCHARGE TUBE TYPES

HG2 - 250 L SN X

DEVICE FAMILY
Harris HG2-SN Series

BREAKDOWN VOLTAGE
230: 230V
250: 250V
300: 300V
350: 350V
470: 470V

LEAD OPTIONS
L: Leads
Blank: No Leads

SN (Non Radioactive)

PACKAGING OPTIONS
T: Tape and Reel
Blank: Bulk

HARRIS SEMICONDUCTOR

HG3 Series

September 1997

Two Electrode High Voltage Surge Arresters

Features

- Small Size
- Rugged Ceramic-Metal Construction
- Non-Radioactive
- Low Capacitance . . . . <1pF
- Available in Tape-and-Reel Packaging
- Available With or Without Leads
- Agency Listings
  - UL1414 Recognized (2000V-8500V)
  - UL1449 Recognized
  - CSA Approved

Applications

- CRT Terminal
- CATV Equipment
- Antennas
- Power Supplies
- Medical Electronics

Description

Harris Semiconductor's two electrode high voltage (1kV- 8.5kV) HG3 Gas Discharge Tubes (GDTs) are designed for surge protection in applications for which bias voltages or signal levels of several hundred volts are normally present. GDTs function as switches and therefore handle currents that far surpass other types of transient voltage protection.

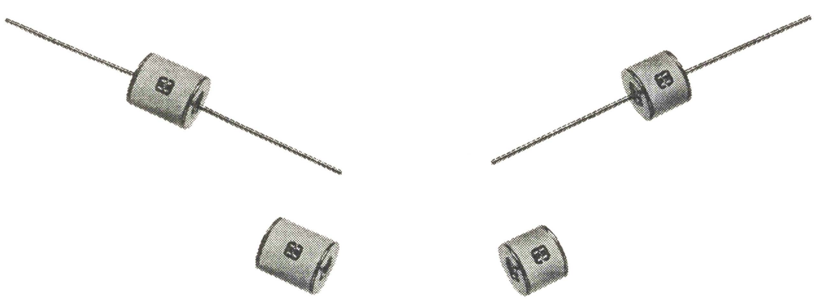
Ordering Information

PART NUMBER	BRAND
HG3-1.0	HG3-1.0
HG3-1.0L	HG3-1.0L
HG3-1.5	HG3-1.5
HG3-1.5L	HG3-1.5L
HG3-2.0	HG3-2.0
HG3-2.0L	HG3-2.0L
HG3-2.5	HG3-2.5
HG3-2.5L	HG3-2.5L
HG3-3.0	HG3-3.0
HG3-3.0L	HG3-3.0L
HG3-4.0	HG3-4.0
HG3-4.0L	HG3-4.0L
HG3-5.0	HG3-5.0
HG3-5.0L	HG3-5.0L
HG3-7.5	HG3-7.5
HG3-7.5L	HG3-7.5L
HG3-8.5	HG3-8.5
HG3-8.5L	HG3-8.5L

NOTES:

1. L means leads; see Ordering Nomenclature.
2. When ordering use the entire part number. Add the suffix T to obtain the variant in tape and reel.

Packaging



File Number **4336**

Absolute Maximum Ratings For ratings of individual members of a series, see device ratings and specifications table.

		HG3 SERIES	UNITS
Operating Ambient Temperature Range	T_A	-40 to 125	^oC
Storage Temperature Range	T_{STG}	-40 to 125	^oC

Electrical Specifications T_C at 25^{o}C Unless Otherwise Specified (PACKAGE OUTLINE A, FIGURE 1)

PARAMETER	SYMBOL	TEST CONDITIONS	HG3-1.0, HG3-1.0L			HG3-1.5, HG3-1.5L			HG3-2.0, HG3-2.0L			HG3-2.5, HG3-2.5L			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
DC Breakdown	V_{BD}	500V/s	800	1000	1200	1200	1500	1800	1600	2000	2400	2000	2500	3000	V
Impulse Breakdown	V_{bd}	100V/µs	-	-	1500	-	-	2200	-	-	3000	-	-	3750	V
Insulation Resistance	IR	100V	10^{10}	-	-	10^{10}	-	-	10^{10}	-	-	10^{10}	-	-	Ω
Capacitance	C	1MHz	-	-	1	-	-	1	-	-	1	-	-	1	pF
Arc Voltage	V_{ARC}	I = 5A Min	-	10	-	-	10	-	-	10	-	-	10	-	V
LIFE RATINGS (Note 1)															
Surge Life	-	0.002µF, 100Ω	500	-	-	500	-	-	500	-	-	500	-	-	Surges
Max Current Surge	-	10kA (8/20µs)	5	-	-	5	-	-	5	-	-	5	-	-	Surges
AC Follow-On Current (Peak)	-	1/2 cycle at 60Hz	-	-	300	-	-	300	-	-	300	-	-	300	A

Electrical Specifications T_C at 25^{o}C Unless Otherwise Specified (PACKAGE OUTLINE B, FIGURE 2)

PARAMETER	SYMBOL	TEST CONDI-TIONS	HG3-3.0, HG3-3.0L			HG3-4.0, HG3-4.0L			HG3-5.0, HG3-5.0L			HG3-7.5, HG3-7.5L			HG3-8.5, HG3-8.5L			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
DC Breakdown	V_{BD}	500V/S	2400	3000	3600	3200	4000	4800	4000	5000	6000	6000	7500	9000	6800	8500	10200	V
Impulse Breakdown	V_{bd}	100V/µs	-	-	4500	-	-	6000	-	-	7500	-	-	10000	-	-	13500	V
Insulation Resistance	IR	100V	10^{10}	-	-	10^{10}	-	-	10^{10}	-	-	10^{10}	-	-	10^{10}	-	-	Ω
Capacitance	C	1MHz	-	-	1	-	-	1	-	-	1	-	-	1	-	-	1	pF
Arc Voltage	V_{ARC}	I = 5A Min	-	10	-	-	10	-	-	10	-	-	10	-	-	10	-	V
LIFE RATINGS (Note 1)																		
Surge Life	-	0.002µF, 100Ω	500	-	-	500	-	-	500	-	-	500	-	-	500	-	-	Surges
Max Current Surge	-	10kA (8/20µs)	5	-	-	5	-	-	5	-	-	5	-	-	5	-	-	Surges
AC Follow-On Current (Peak)	-	1/2 Cycle at 60Hz	-	-	300	-	-	300	-	-	300	-	-	300	-	-	300	A

NOTE:

1. End-of-Life limits:
   DC: 50% of minimum initial DC breakdown voltage limit to150% of maximum initial DC breakdown voltage limit.
   Impulse: less that 150% of initial impulse breakdown voltage limit.

Mechanical Dimensions

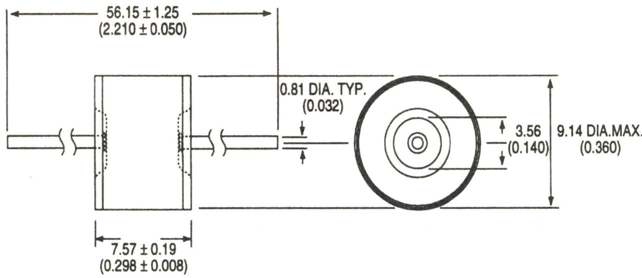


FIGURE 1. OUTLINE A

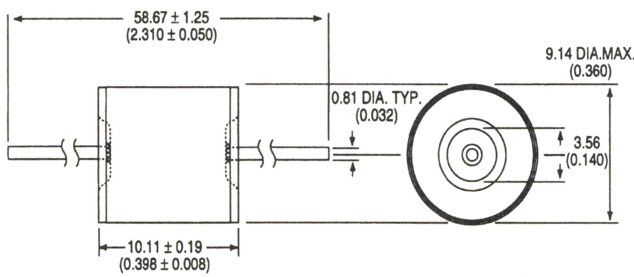


FIGURE 2. OUTLINE B

Ordering Nomenclature

A complete part number is represented by the digits below. For example, HG3-1.5 is a non-leaded 1500V device, HG3-5.0L is a leaded 5000V device, and HG3-7.5LT is a leaded 7500V device on tape-and-reel per EIA standard RS-296-D.

HG3 GAS DISCHARGE TUBE TYPES

HG3- 2.5 X X

DEVICE FAMILY
Harris HG3 Series

BREAKDOWN VOLTAGE
1.0: 1000V
1.5: 1500V
2.0: 2000V
2.5: 2500V
3.0: 3000V
4.0: 4000V
5.0: 5000V
7.5: 7500V
8.5: 8500V

PACKAGING OPTIONS
T: Tape and Reel
Blank: Bulk

LEAD OPTIONS
L: Leads
Blank: No Leads

HPMT3 Series

January 1998

Three Electrode Surge Arresters

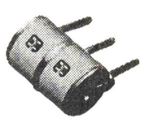
Features

- Small Size
- Rugged Ceramic-Metal Construction
- Low Capacitance . . . . <1pF
- Available with Fail-Safe Clip
- Available With or Without Leads
- Various Lead Configurations
- Available in Tube Packaging
- Agency Listings
  - UL Recognized
  - REA PE-80

Applications

- Telecom Network Interfaces
- Telephone Line Cards
- Repeaters
- Modems
- Line Test Equipment

Packaging



Description

Harris Semiconductor's three electrode HPMT3 Gas Discharge Tubes (GDTs) are designed for a high degree of surge protection at a low cost. This series (150V-500V) is primarily used for the protection of telecommunications equipment in which simultaneous crowbar action of two signal lines is required. GDTs function as switches and therefore handle currents that far surpass other types of transient voltage protection.

Ordering Information

PART NUMBER	BRAND
HPMT3-15001	310-15001
HPMT3-15004	310-15004
HPMT3-15006	310-15006
HPMT3-15010	310-15010
HPMT3-23001	310-23001
HPMT3-23004	310-23004
HPMT3-23006	310-23006
HPMT3-23010	310-23010
HPMT3-25001	310-25001
HPMT3-25004	310-25004
HPMT3-25006	310-25006
HPMT3-25010	310-25010
HPMT3-35001	310-35001
HPMT3-35004	310-35004
HPMT3-35006	310-35006
HPMT3-35010	310-35010
HPMT3-40001	310-40001
HPMT3-40004	310-40004
HPMT3-40006	310-40006
HPMT3-40010	310-40010
HPMT3-50001	310-50001
HPMT3-50004	310-50004
HPMT3-50006	310-50006
HPMT3-50010	310-50010

NOTE:

1. When ordering use the entire part number. Add the suffix F to obtain the variant with failsafe.

Absolute Maximum Ratings For ratings of individual members of a series, see device ratings and specifications table.

		HPMT3 SERIES	UNITS
Operating Ambient Temperature Range	T_A	-40 to 125	^oC
Storage Temperature Range	T_{STG}	-40 to 125	^oC

Electrical Specifications T_C at 25^oC Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	HPMT3-150XX			HPMT3-230XX			HPMT3-250XX			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
DC Breakdown	$V_{BD(I-g)}$	500V/S	120	150	180	184	230	276	200	250	300	V
	$V_{BD(I-I)}$		-	-	360	-	-	552	-	-	600	V
Impulse Breakdown	$V_{bd(I-g)}$	100V/µs	-	-	500	-	-	600	-	-	600	V
Insulation Resistance	IR	100V	10^{10}	-	-	10^{10}	-	-	10^{10}	-	-	Ω
Capacitance	$C_{(I-g)}$	1MHz	-	-	1	-	-	1	-	-	1	pF
	$C_{(I-I)}$		-	-	0.5	-	-	0.5	-	-	0.5	pF
Arc Voltage	V_{ARC}	I = 5A Min	-	16	-	-	16	-	-	16	-	V
LIFE RATINGS ††												
Surge Life	-	500A, 10/1000µs	400	-	-	400	-	-	400	-	-	Surges
Max Current Surge	-	10kA + 10kA † (8/20µs)	1	-	-	1	-	-	1	-	-	Surges
AC Current		11 Cycles at 60Hz	-	N/A	-	-	-	65+65 †	-	-	65+65 †	A
AC Follow-On Current (Peak)	-	1/2 Cycle at 60Hz	-	N/A	-	-	-	20	-	-	20	A

Electrical Specifications T_C at 25^oC Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	HPMT3-350XX			HPMT3-400XX			HPMT3-500XX			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
DC Breakdown	$V_{BD(I-g)}$	500V/S	280	350	420	320	400	480	400	500	600	V
	$V_{BD(I-I)}$		-	-	800	-	-	1000	-	-	1200	V
Impulse Breakdown	$V_{bd(I-g)}$	100V/µs	-	-	750	-	-	750	-	-	850	V
Insulation Resistance	IR	100V	10^{10}	-	-	10^{10}	-	-	10^{10}	-	-	Ω
Capacitance	$C_{(I-g)}$	1MHz	-	-	1	-	-	1	-	-	1	pF
	$C_{(I-I)}$		-	-	0.5	-	-	0.5	-	-	0.5	pF
Arc Voltage	V_{ARC}	I = 5A Min	-	16	-	-	16	-	-	16	-	V
LIFE RATINGS ††												
Surge Life	-	500A, 10/1000µs	400	-	-	400	-	-	400	-	-	Surges
Max Current Surge	-	10kA + 10kA † (8/20µs)	1	-	-	1	-	-	1	-	-	Surges
AC Current		11 Cycles at 60Hz	-	65+65 †	-	-	-	65+65 †	-	-	65+65 †	A
AC Follow-On Current (Peak)	-	1/2 Cycle at 60Hz	-	20	-	-	-	20	-	-	20	A

† Represents current rating from the center electrode to one of the end electrodes "+" the current rating from the center electrode to the other end electrode. Current rating from the center electrode to both end electrodes is the sum (+).

†† End-of-Life limits:
DC: 50% of minimum initial DC breakdown voltage limit to 150% of maximum initial DC breakdown voltage limit.
Impulse: less that 150% of initial impulse breakdown voltage limit.

Mechanical Dimensions

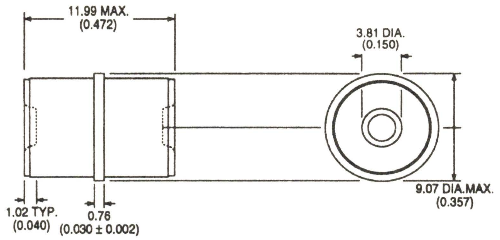


FIGURE 1. OUTLINE 01

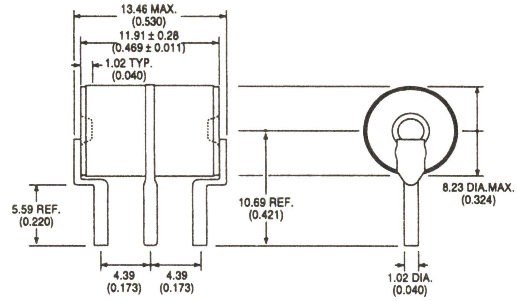


FIGURE 2. OUTLINE 04

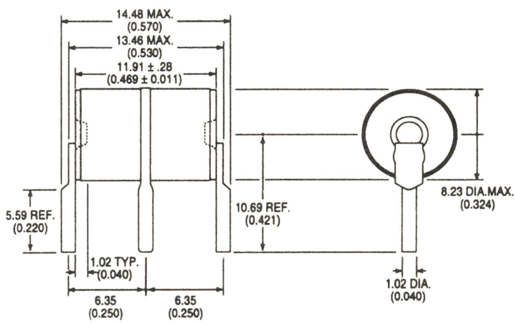


FIGURE 3. OUTLINE 06

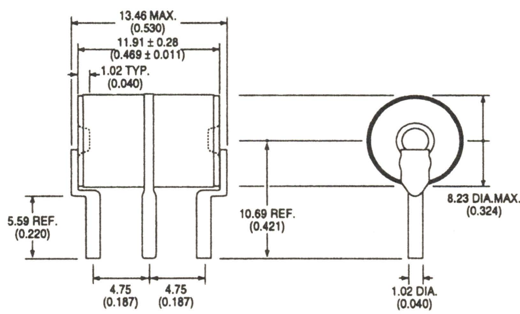


FIGURE 4. OUTLINE 10

Ordering Nomenclature

A complete part number is represented by the digits below. For example, HPMT3-25010 is a 250V device with Outline 10 (see Figure 4) (pins on 4.75mm centers).

HPMT3 GAS DISCHARGE TUBE TYPES

HPMT3 - 250 10 F

DEVICE FAMILY
Harris HPMT3 Series

BREAKDOWN VOLTAGE
150: 150V
230: 230V
250: 250V
400: 400V
500: 500V

OUTLINE OPTIONS
01, 04, 06, 10

PACKAGING OPTIONS
Blank: Bulk
F: Failsafe Option

TVS 8

SURGECTOR PRODUCTS

Surgector Products Series Overview

Surgectors are the Harris discrete Silicon thyristor technology devices that are comprised of self-triggered unidirectional and bidirectional types, as well as unidirectional externally triggered types, all listed in Table 1.

The self-triggered bidirectional devices utilize integral zeners for turn-on at a defined transient voltage level and are further differentiated by peak current and holding current ratings.

Unidirectional types also have integral zeners but include lower trigger voltages.

The externally triggered types are essentially SCR devices requiring trigger zeners provided by the user.

Most surgector types are intended for operation on the telephone line "tip and ring" environment in order to protect phone, modem, or other communication products. Surgectors also find application in alarms, controllers or other circuits desiring an SCR "crowbar" action for transient voltages.

Transient Voltage Suppressor Device Selection Guide

MARKET SEGMENT	TYPICAL APPLICATIONS AND CIRCUITS EXAMPLES	DEVICE FAMILY OR SERIES	DATA BOOK SECTION	TECHNOLOGY	SURFACE MOUNT PRODUCT?
Low Voltage, Board Level Products	• Hand-Held/Portable Devices • EDP • Computer • I/O Port and Interfaces • Controllers • Instrumentation • Remote Sensors • Medical Electronics, etc	CH	4	MOV	✔
		MA, ZA, RA	4	MOV	
		ML, MLE	5	Multilayer Suppressor	✔
		SP72X	6	SCR/Diode Array	✔ †
AC Line, TVSS Products	• UPS • AC Panels • AC Power Taps • TVSS Devices • AC Appliance/Controls • Power Meters • Power Supplies • Circuit Breakers • Consumer Electronics	UltraMOV™ "C" III, LA, HA, RA	4	MOV	
		CH	4	MOV	✔
		GDT	7	Gas Discharge Tube	
Automotive Electronics	• ABS • EEC • Instrument Cluster • Air Bag • Window Control • Wiper Modules • Multiplex Bus • EFI	CH	4	MOV	✔
		ZA	4	MOV	
		AUML, ML	5	Multilayer Suppressor	✔
		SP72X	6	SCR/Diode Array	✔ †
Telecommunications Products	**• Cellular/Cordless Phone • Modems • Secondary Phone Line Protectors • Data Line Connectors • Repeaters • Line Cards**	CH	4	MOV	✔
		CP, CS, ZA	4	MOV	
		ML, MLE	5	Multilayer Suppressor	✔
		SP72X	6	SCR/Diode Array	✔ †
		GDT	7	Gas Discharge Tube	
		Surgector	**8**	**Thyristor/Zener**	
Industrial, High Energy AC Products	• High Current Relays • Solenoids • Motor Drives • AC Distribution Panels • Robotics • Large Motors	DA/DB, BA/BB, CA, HA, NA, PA	4	MOV	
		GDT	7	Gas Discharge Tube	
Arrester Products	• Lightning Arrester Assemblies for High Voltage AC Power Distribution Lines and Utility Transformers	AS	9	MOV	

† Available in both surface mount and through-hole packages.

Surgector Products Series Overview

TABLE 1. SELECTION GUIDE

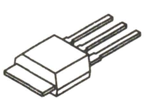
PART NUMBER	FUNCTION	V_Z MIN (V)	V_{BO} MAX (100V/µs)	I_{TSM} (1 x 2µs)	I_{TSM} (10 x 1000µs)	I_H (mA)	PACKAGE STYLE
SGT10S10 (Note 1)	VAR Clamp	100	Note 1	300	100	>100	A
SGT27S10 (Note 1)	VAR Clamp	270	Note 1	300	100	>100	A
SGT27S23 (Note 1)	VAR Clamp	270	Note 1	300	100	>230	A
SGT03U13	Unidirectional	30	< 50	300	100	>130	B
SGT06U13	Unidirectional	60	< 85	300	100	>130	B
SGT23U13	Unidirectional	230	< 275	300	100	>130	B
SGT21B13	Bidirectional	210	270	300	100	>130	B
SGT21B13A	Bidirectional	210	290	300	100	>130	B
SGT22B13	Bidirectional	220	280	300	100	>130	B
SGT22B13A	Bidirectional	220	290	300	100	>130	B
SGT23B13	Bidirectional	230	290	300	100	>130	B
SGT23B13A	Bidirectional	230	315	300	100	>130	B
SGT27B13	Bidirectional	270	345	300	100	>130	B
SGT27B13A	Bidirectional	270	360	300	100	>130	B
SGT27B13B	Bidirectional	270	375	300	100	>130	B
SGT27B27	Bidirectional	270	345	600	200	>270	B
SGT27B27A	Bidirectional	270	360	600	200	>270	B
SGT27B27B	Bidirectional	270	375	600	200	>270	B

NOTES:

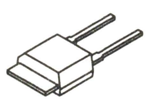
1. Dependent on trigger circuit.
2. All surgectors supplied in modified JEDEC TO-202 Package.
   Package Style A = 3 lead version
   Package Style B = 2 lead version
3. All devices UL recognized to 497B - File Number E135010.

Surgector Packages

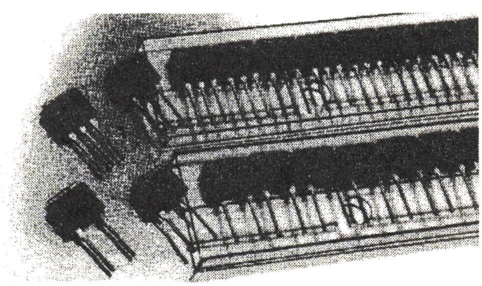
MODIFIED TO-202 PACKAGE STYLE



PACKAGE A



PACKAGE B



Surgector devices are shipped to the customer either in bulk or in plastic rectangular tubes or "rails" that hold 50 surgector devices each.

SEMICONDUCTOR

SGT03U13, SGT06U13, SGT23U13

Unidirectional Transient Surge Suppressors (Surgector)

January 1998

Features

- Clamping Voltages: 33V, 60V, or 230V
- Peak Transient Surge Current: 300A
- Minimum Holding Current: 130mA
- Subnanosecond Clamping Action
- Low On-State Voltage
- UL Recognized File #E135010 to STD 497B

Applications

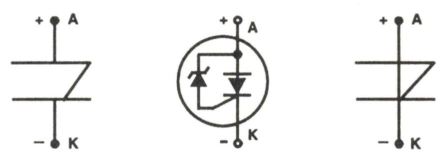
- Telecommunications Equipment
- Data and Communication Links
- Computer Modems
- Alarm Systems

Description

These surgector devices are designed to protect telecommunication equipment, data links, alarm systems, power supplies and other sensitive electrical circuits from damage by switching transients, lightning strikes, load changes, commutation spikes and line crosses.

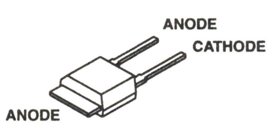
These surgector devices are monolithic compound structures consisting of a thyristor whose gate region contains a special diffused section which acts as a zener diode. This zener diode section permits anode voltage turn-on of the structure. Initial clamping by the zener diode section and fast turn-on by the thyristor, provide excellent voltage limiting even on very fast rise time transients. The thyristor also features very high holding current allowing the surgector to recover to its high impedance off state after a transient. The surgector device's normal off-state condition in the forward blocking mode is a high impedance, low leakage state that prevents loading of the line.

Equivalent Schematic Symbols



Packaging

MODIFIED TO-202



8

SURGECTOR PRODUCTS

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number 1692.2

Absolute Maximum Ratings $T_C = 25^oC$

	SGT03U13	SGT06U13	SGT23U13	UNITS
Continuous Off State Voltage:				
V_{DM}	30	58	225	V
V_{RM}	1	1	1	V
Transient Peak Surge Current: I_{TSM}				
1μs x 2μs (Note 1)	300	300	300	A
8μs x 20μs	200	200	200	A
10μs x 560μs	125	125	125	A
10μs x 1000μs	100	100	100	A
One Half Cycle 50Hz to 60Hz (Note 2)	60	60	60	A
One Second 50Hz to 60Hz, Halfwave	30	30	30	A
Operating Temperature (T_A)		-40 to 85		^oC
Storage Temperature Range (T_{STG})		-40 to 150		^oC

NOTES:

1. Unit designed not to fail open below: 450A.
2. One every 30s maximum.

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications At Case Temperature, $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	SGT10S10 MIN	TYP	MAX	UNITS
Off-State Current	I_{DM}	Maximum Rated V_{DM}				
		$T_A = 25^oC$	-	-	50	nA
		$T_A = 85^oC$	-	-	10	μA
Reverse Current	I_{RM}	$V_{RM} = 1V$				
		$T_A = 25^oC$	-	-	1	mA
		$T_A = 85^oC$	-	-	10	mA
Clamping Voltage	V_Z	$I_Z = 100\mu A$				
SGT03U13			33	-	-	V
SGT06U13			60	-	-	V
SGT23U13			230	-	-	V
Breakover Voltage	V_{BO}	dv/dt = 100V/μs				
SGT03U13			-	-	50	V
SGT06U13			-	-	85	V
SGT23U13			-	-	275	V
Holding Current	I_H		130	-	-	mA
On-State Voltage	V_T	$I_T = 10A$	-	-	2	V
Main Terminal Capacitance	C_O		-	90	-	pF

Performance Curves

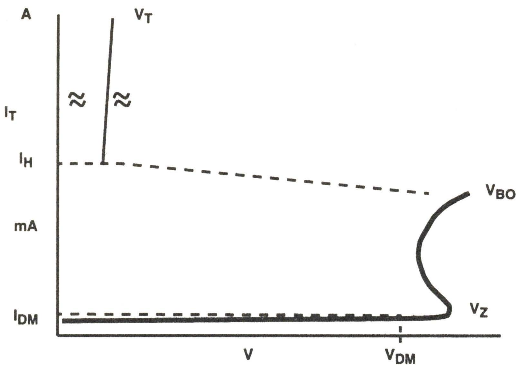


FIGURE 1. TYPICAL VOLT-AMPERE CHARACTERISTICS

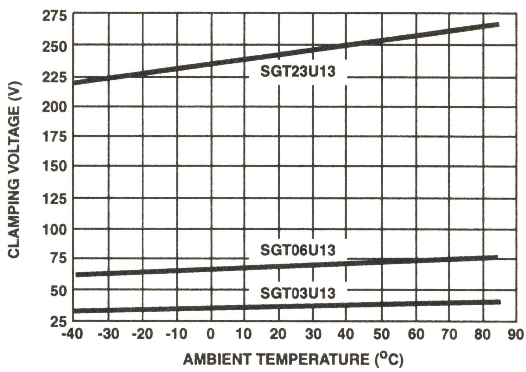


FIGURE 2. TYPICAL CLAMPING VOLTAGE vs TEMPERATURE

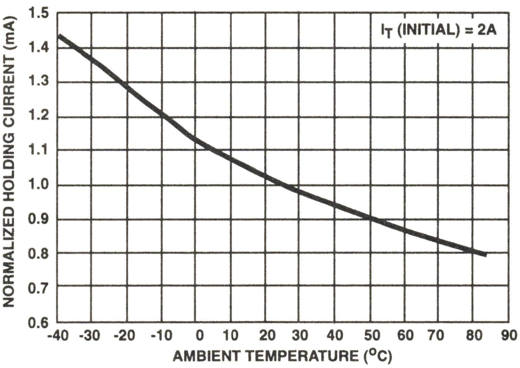


FIGURE 3. TYPICAL HOLDING CURRENT vs TEMPERATURE

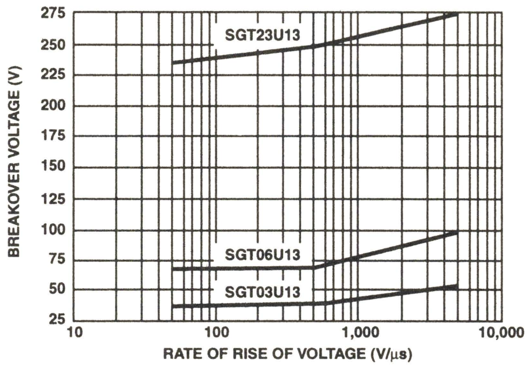


FIGURE 4. TYPICAL V_{BO} vs dv/dt

Terms and Symbols

V_{DM} (Maximum Off-State Voltage) - Maximum off-state voltage (DC or peak) which may be applied continuously.

V_{RM} (Maximum Reverse Voltage) - Maximum reverse-blocking voltage (DC or peak) which may be applied.

I_{TSM} (Maximum Peak Surge Current) - Maximum nonrepetitive current which may be allowed to flow for the time state.

T_A (Ambient Operating Temperature) - Ambient temperature range permitted during operation in a circuit.

T_{STG} (Storage Temperature) - Temperature range permitted during storage.

I_{DM} (Off-State Current) - Maximum value of off-state current that results from the application of the maximum off-state voltage (V_{DM}).

I_{RM} (Reverse Current) - Maximum value of reverse current that results from the application of the maximum reverse voltage (V_{RM}).

V_Z (Clamping Voltage) - Off-state voltage at a specified current.

V_{BO} (Breakdown Voltage) - Voltage at which the device switches from the off-state to the on-state.

I_H (Holding Current) - Minimum on-state current that will hold the device in the on-state after it has been latched on.

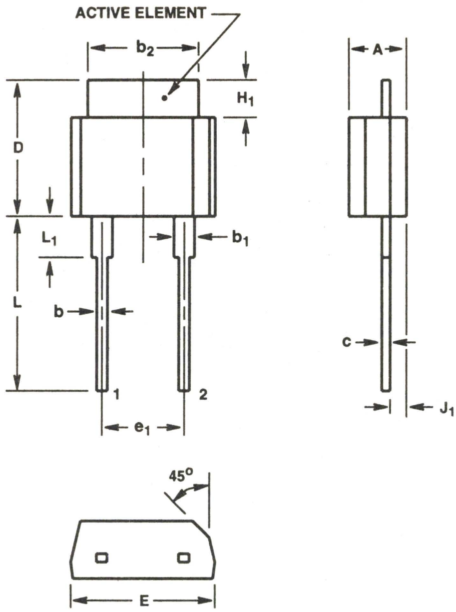
V_T (On-State Voltage) - Voltage across the main terminals for a specified on-state current.

C_O (Main Terminal Capacitance) - Capacitance between the main terminals at a specified off-state voltage.

8

SURGECTOR PRODUCTS

Mechanical Dimensions



TO-202 Modified

2 LEAD JEDEC STYLE TO-202 SHORT TAB PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.130	0.150	3.31	3.81	-
b	0.024	0.028	0.61	0.71	2, 3
b_1	0.045	0.055	1.15	1.39	1, 2, 3
b_2	0.270	0.280	6.86	7.11	-
c	0.018	0.022	0.46	0.55	1, 2, 3
D	0.320	0.340	8.13	8.63	-
E	0.340	0.360	8.64	9.14	-
e_1	0.200 BSC		5.08 BSC		4
H_1	0.080	0.100	2.04	2.54	-
J_1	0.039	0.049	1.00	1.24	5
L	0.410	0.440	10.42	11.17	-
L_1	0.080	0.100	2.04	2.54	1

NOTES:

1. Lead dimension and finish uncontrolled in L_1.
2. Lead dimension (without solder).
3. Add typically 0.002 inches (0.05mm) for solder coating.
4. Position of lead to be measured 0.250 inches (6.35mm) from bottom of dimension D.
5. Position of lead to be measured 0.100 inches (2.54mm) from bottom of dimension D.
6. Controlling dimension: Inch.
7. Revision 3 dated 10-94.

Nomenclature

SGT 03 U 13

- 13 — Holding Current in mA divided by 10
- U — **Type of Surgector**
  - U: Unidirectional
  - B: Bidirectional
  - S: SCR
- 03 — Off-State Voltage Rating Divided by 10
- SGT — Surgector

SGT10S10, SGT27S10

Gate Controlled Unidirectional Transient Surge Suppressors

January 1998

Features

- Blocking Voltage 100V and 270V
- Peak Transient Surge Current 300A
- Minimum Holding Current 100mA
- Subnanosecond Clamping Action
- Low On-State Voltage
- UL Recognized File # E135010 to STD 497B

Applications

- Telecommunications Equipment
- Data and Voice Lines
- Computer Modems
- Alarm Systems

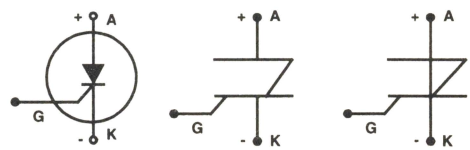
Description

Surgector transient surge protectors are designed to protect telecommunication equipment, data links, alarm systems, power supplies, and other sensitive electrical circuits from damage that could be caused by switching transients, lightning strikes, load changes, commutation spikes, and line crosses.

These devices are fast turn-on, high holding current thyristors. When coupled with a user supplied voltage level detector, they provide excellent voltage limiting even on very fast rise time transients. The high holding current allows this surgector to return to its high impedance off state after a transient.

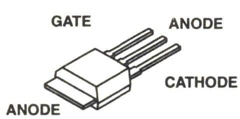
The surgector device's normal off-state condition in the forward blocking mode is a high impedance, low leakage state that prevents loading of the line.

Equivalent Schematic Symbols



Packaging

MODIFIED TO-202



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **1691.2**

Absolute Maximum Ratings $T_C = 25^oC$

		SGT10S10	SGT27S10	UNITS
Continuous Off State Voltage:				
V_{DM}		100	270	V
V_{RM}		1	1	V
Transient Peak Surge Current:	I_{TSM}			
1μs x 2μs (Note 1)		300	300	A
8μs x 20μs		200	200	A
10μs x 560μs		125	125	A
10μs x 1000μs		100	100	A
One Half Cycle, 1 every 30s	50Hz to 60Hz	60	60	A
One Second, Halfwave	50Hz to 60Hz	30	30	A
Operating Temperature (T_A)		-40 to 85		^oC
Storage Temperature Range (T_{STG})		-40 to 150		^oC

NOTE:

1. Unit designed not to fail open below 450A.

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications At Case Temperature, $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	SGT10S10			SGT27S10			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Off-State Current	I_{DM}	$V_{DM} = 100V$							
		$T_A = 25^oC$	-	-	50	-	-	-	nA
		$T_A = 85^oC$	-	-	10	-	-	-	μA
	I_{DM}	$V_{DM} = 270V$							
		$T_A = 25^oC$	-	-	-	-	-	100	nA
		$T_A = 85^oC$	-	-	-	-	-	50	μA
Off-State Current	I_{RM}	$V_{RM} = 1V$							
		$T_A = 25^oC$	-	-	1	-	-	1	mA
		$T_A = 85^oC$	-	-	10	-	-	10	mA
Breakover Voltage	V_{BO}	dv/dt = 100V/μs (Note 2)	-	-	100	-	-	285	V
Holding Current	I_H		100	-	-	100	-	-	mA
On-State Voltage	V_T	$I_T = 10A$	-	-	2	-	-	2	V
Gate-Trigger Current	I_{GT}		-	-	150	-	-	150	mA
Main Terminal Capacitance	C_O	$V_{DM} = 0V$	-	90	-	-	-	-	pF
		$V_{DM} = 50V$ at 1MHz	-	-	-	-	50	-	pF

NOTE:

2. External zener diode from anode to gate: 60V (SGT10S10); 270V (SGT27S10).

Performance Curves

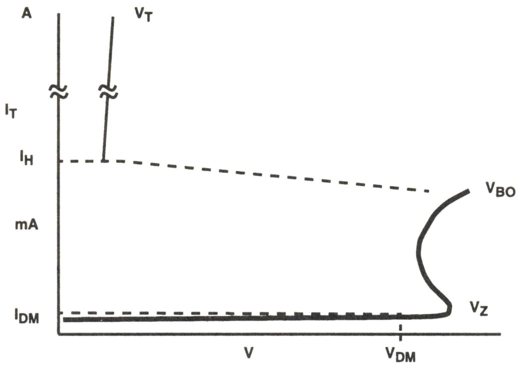


FIGURE 1. TYPICAL VOLT-AMPERE CHARACTERISTICS

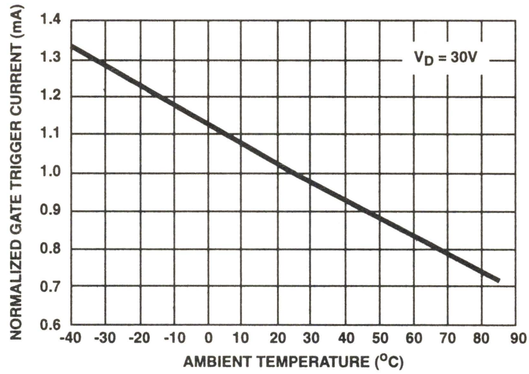


FIGURE 2. NORMALIZED GATE-TRIGGER CURRENT vs TEMPERATURE

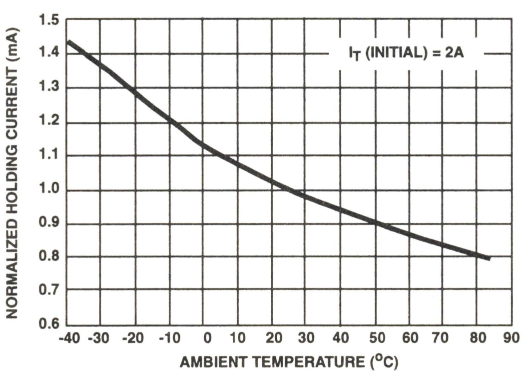


FIGURE 3. NORMALIZED HOLDING CURRENT vs TEMPERATURE

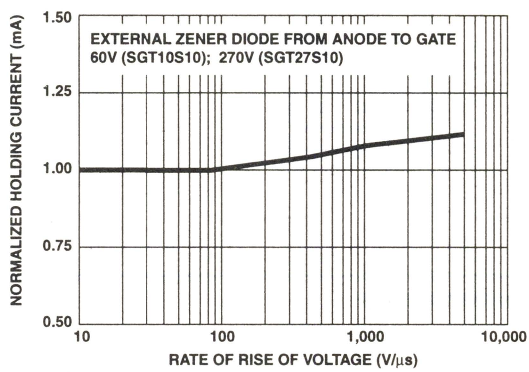


FIGURE 4. NORMALIZED V_{BO} vs dv/dt

Terms and Symbols

V_{DM} (Maximum Off-State Voltage) - Maximum off-state voltage (DC or peak) which may be applied continuously.

V_{RM} (Maximum Reverse Voltage) - Maximum reverse-blocking voltage (DC or peak) which may be applied.

I_{TSM} (Maximum Peak Surge Current) - Maximum nonrepetitive current which may be allowed to flow for the time state.

T_A (Ambient Operating Temperature) - Ambient temperature range permitted during operation in a circuit.

T_{STG} (Storage Temperature) - Temperature range permitted during storage.

I_{DM} (Off-State Current) - Maximum value of off-state current that results from the application of the maximum off-state voltage (V_{DM}).

I_{RM} (Reverse Current) - Maximum value of reverse current that results from the application of the maximum reverse voltage (V_{RM}).

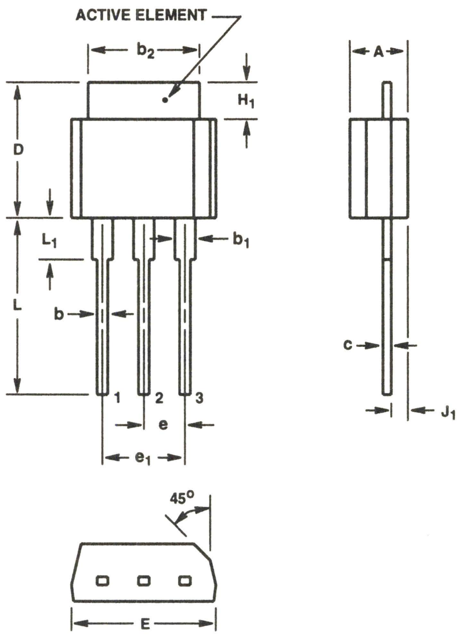
I_H (Holding Current) - Minimum on-state current that will hold the device in the on-state after it has been latched on.

V_T (On-State Voltage) - Voltage across the main terminals for a specified on-state current.

I_{GT} (Gate-Trigger Current) - Minimum gate current which will cause the device to switch from the off-state to the on-state.

C_O (Main Terminal Capacitance) - Capacitance between the main terminals at a specified off-state voltage.

Mechanical Dimensions



TO-202 Modified

3 LEAD JEDEC STYLE TO-202 SHORT TAB PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.130	0.150	3.31	3.81	-
b	0.024	0.028	0.61	0.71	2, 3
b_1	0.045	0.055	1.15	1.39	1, 2, 3
b_2	0.270	0.280	6.86	7.11	-
c	0.018	0.022	0.46	0.55	1, 2, 3
D	0.320	0.340	8.13	8.63	-
E	0.340	0.360	8.64	9.14	-
e	0.100 TYP		2.54 TYP		4
e_1	0.200 BSC		5.08 BSC		4
H_1	0.080	0.100	2.04	2.54	-
J_1	0.039	0.049	1.00	1.24	5
L	0.410	0.440	10.42	11.17	-
L_1	0.080	0.100	2.04	2.54	1

NOTES:

1. Lead dimension and finish uncontrolled in L_1.
2. Lead dimension (without solder).
3. Add typically 0.002 inches (0.05mm) for solder coating.
4. Position of lead to be measured 0.250 inches (6.35mm) from bottom of dimension D.
5. Position of lead to be measured 0.100 inches (2.54mm) from bottom of dimension D.
6. Controlling dimension: Inch.
7. Revision 3 dated 10-94.

Nomenclature

SGT 10 S 10

- 10 — Holding Current in mA divided by 10
- S — **Type of Surgector**
  - U: Unidirectional
  - B: Bidirectional
  - S: SCR
- 10 — Off-State Voltage Rating Divided by 10
- SGT — Surgector

SGT21B13, SGT21B13A, SGT22B13, SGT22B13A, SGT23B13, SGT23B13A, SGT27B13, SGT27B13A, SGT27B13B

Bidirectional Transient Surge Suppressors (Surgector)

January 1998

Features

- Clamping Voltage. 210V, 220V,
- 230V and 270V
- Peak Transient Surge Current 300A
- Minimum Holding Current. 130mA
- Continuous Protection
- Low On-State Voltage
- UL Recognized File #E135010 to STD 497B

Applications

- Data and Communication Links
- Computer Modems
- Alarm Systems

Description

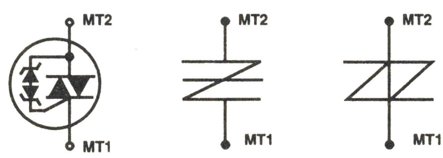
These surgector devices are designed to protect telecommunication equipment, data links, alarm systems, power supplies and other sensitive electrical circuits from damage by switching transients, lightning strikes, load changes, commutation spikes and line crosses.

Bidirectional surgector devices are constructed using two monolithic compound chips each consisting of a thyristor whose gate region contains a special diffused section which acts as a zener diode. This chips are connected in anti parallel, providing bidirectional protection. This zener diode section permits anode voltage turn on of the structure.

Initial clamping by the zener diode section, and fast turn on by the thyristor, provide excellent voltage limiting even on very fast rise time transients. The thyristor also features very high holding current, which allows the surgector to recover to its high impedance off state after a transient.

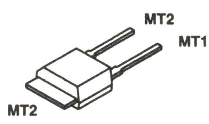
All these devices are supplied in a 2 lead, modified TO-202 VERSATAB package.

Equivalent Schematic Symbols



Packaging

MODIFIED TO-202



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

Absolute Maximum Ratings $T_C = 25^oC$

	SGT21B13 SGT21B13A	SGT22B13 SGT22B13A	SGT23B13 SGT23B13A	SGT27B13 SGT27B13A SGT27B13B	UNITS
Continuous Off State Voltage:					
V_{DM}	185	190	200	235	V
V_{RM}	185	190	200	235	V
Transient Peak Surge Current . . . . I_{TSM}					
1μs x 2μs (Note 1)	300	300	300	300	A
8μs x 20μs	200	200	200	200	A
10μs x 560μs	125	125	125	125	A
10μs x 1000μs	100	100	100	100	A
One Half Cycle . . . . 50Hz to 60Hz (Note 2)	60	60	60	60	A
One Second . . . . 50Hz to 60Hz, Halfwave	30	30	30	30	A
Operating Temperature (T_A)	-40 to 85		-40 to 85		^oC
Storage Temperature Range (T_{STG})	-40 to 150		-40 to 150		^oC

NOTES:

1. Unit designed not to fail open below: 450A.
2. One every 30s maximum.

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications At Case Temperature, $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Off-State Current	I_{DM}, I_{RM}	Maximum Rated V_{DM}, V_{RM}				
		$T_A = 25^oC$	-	-	200	nA
		$T_A = 85^oC$	-	-	100	μA
Clamping Voltage	V_Z	I_Z < 200μA				
SGT21B13			210	-	250	V
SGT21B13A			210	-	270	V
SGT22B13			220	-	260	V
SGT22B13A			220	-	270	V
SGT23B13			230	-	270	V
SGT23B13A			230	-	295	V
SGT27B13			270	-	325	V
SGT27B13A			270	-	340	V
SGT27B13B			270	-	355	V
Breakover Voltage	V_{BO}	dv/dt = 100V/μs				
SGT21B13			-	-	270	V
SGT21B13A			-	-	290	V
SGT22B13			-	-	280	V
SGT22B13A			-	-	290	V
SGT23B13			-	-	290	V
SGT23B13A			-	-	315	V
SGT27B13			-	-	345	V
SGT27B13A			-	-	360	V
SGT27B13B			-	-	375	V
Holding Current	I_H		130	-	-	mA
On-State Voltage	V_T	I_T = 10A	-	-	2	V
Main Terminal Capacitance	C_O	$V_{DM} = V_{RM}$ = 50V, Frequency = 1MHz	-	50	-	pF

Performance Curves

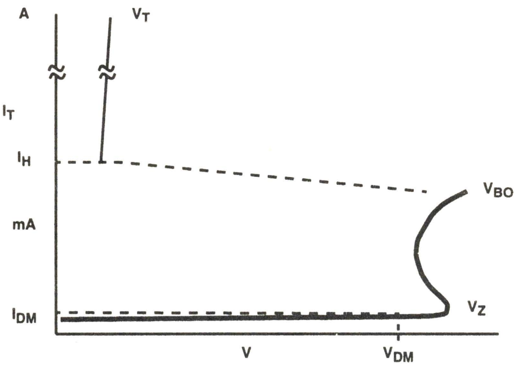


FIGURE 1. TYPICAL VOLT-AMPERE CHARACTERISTICS FOR ALL TYPES

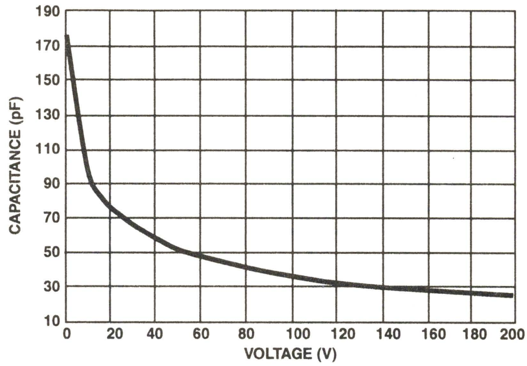


FIGURE 2. TYPICAL CAPACITANCE vs VOLTAGE FOR ALL TYPES

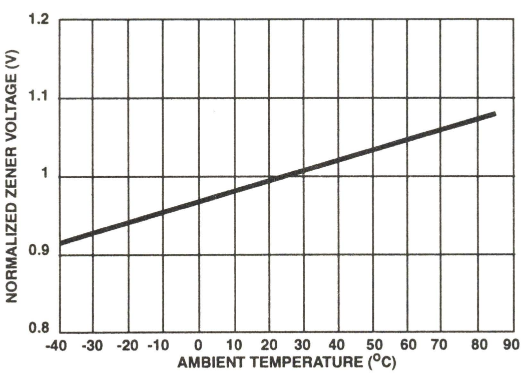


FIGURE 3. NORMALIZED ZENER VOLTAGE vs TEMPERATURE FOR ALL TYPES

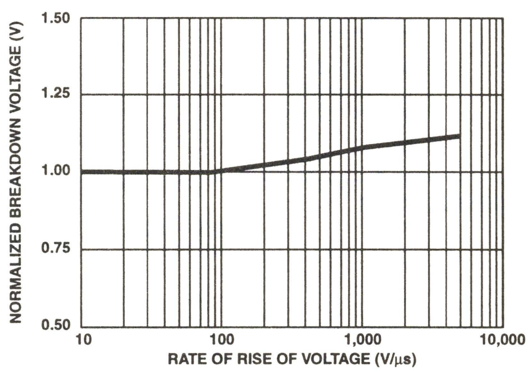


FIGURE 4. NORMALIZED V_{BO} vs dv/dt FOR ALL TYPES

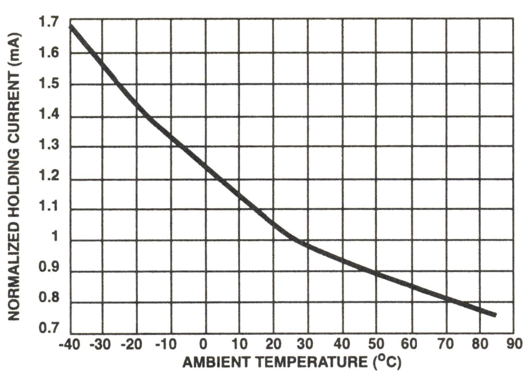
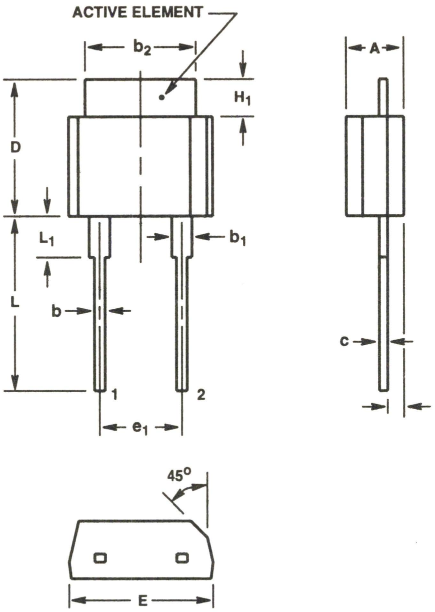


FIGURE 5. NORMALIZED HOLDING CURRENT vs TEMPERATURE FOR ALL TYPES

Mechanical Dimensions



TO-202 Modified

2 LEAD JEDEC STYLE TO-202 SHORT TAB PLASTIC PACKAGE

SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A	0.130	0.150	3.31	3.81	-
b	0.024	0.028	0.61	0.71	2, 3
b_1	0.045	0.055	1.15	1.39	1, 2, 3
b_2	0.270	0.280	6.86	7.11	-
c	0.018	0.022	0.46	0.55	1, 2, 3
D	0.320	0.340	8.13	8.63	-
E	0.340	0.360	8.64	9.14	-
e_1	0.200 BSC		5.08 BSC		4
H_1	0.080	0.100	2.04	2.54	-
J_1	0.039	0.049	1.00	1.24	5
L	0.410	0.440	10.42	11.17	-
L_1	0.080	0.100	2.04	2.54	1

NOTES:

1. Lead dimension and finish uncontrolled in L_1.
2. Lead dimension (without solder).
3. Add typically 0.002 inches (0.05mm) for solder coating.
4. Position of lead to be measured 0.250 inches (6.35mm) from bottom of dimension D.
5. Position of lead to be measured 0.100 inches (2.54mm) from bottom of dimension D.
6. Controlling dimension: Inch.
7. Revision 3 dated 10-94.

Nomenclature

SGT 22 B 13 X

- X — **V_Z/V_{BO} Variant**
  - Blank: Lower Value
  - A: Higher Value
- 13 — Holding Current in mA divided by 10
- B — **Type of Surgector**
  - U: Unidirectional S: SCR
  - B: Bidirectional
- 22 — Off-State Voltage Rating Divided by 10
- SGT — Surgector

Terms and Symbols

V_{DM} (Maximum Off-State Voltage) - Maximum off-state voltage (DC or peak) which may be applied continuously.

V_{RM} (Maximum Reverse Voltage) - Maximum reverse-blocking voltage (DC or peak) which may be applied.

I_{TSM} (Maximum Peak Surge Current) - Maximum nonrepetitive current which may be allowed to flow for the time state.

T_A (Ambient Operating Temperature) - Ambient temperature range permitted during operation in a circuit.

T_{STG} (Storage Temperature) - Temperature range permitted during storage.

I_{DM} (Off-State Current) - Maximum value of off-state current that results from the application of the maximum off-state voltage (V_{DM}).

I_{RM} (Reverse Current) - Maximum value of reverse current that results from the application of the maximum reverse voltage (V_{RM}).

V_Z (Clamping Voltage) - Off-state voltage at a specified current.

V_{BO} (Breakdown Voltage) - Voltage at which the device switches from the off-state to the on-state.

I_H (Holding Current) - Minimum on-state current that will hold the device in the on-state after it has been latched on.

V_T (On-State Voltage) - Voltage across the main terminals for a specified on-state current.

C_O (Main Terminal Capacitance) - Capacitance between the main terminals at a specified off-state voltage.

SGT27B27, SGT27B27A, SGT27B27B

HARRIS SEMICONDUCTOR

Bidirectional Transient Surge Suppressors (Surgector)

January 1998

Features

- Clamping Voltage . . . . . 230V or 270V
- Peak Transient Surge Current 600A
- Minimum Holding Current 270mA
- Continuous Protection
- Low On-State Voltage
- UL Recognized File #E135010 to STD 497B

Applications

- Data and Communication Links
- Computer Modems
- Alarm Systems

Description

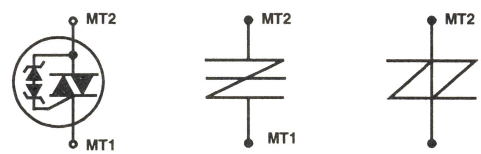
These surgector devices are designed to protect telecommunication equipment, data links, alarm systems, power supplies and other sensitive electrical circuits from damage by switching transients, lightning strikes, load changes, commutation spikes and line crosses.

Bidirectional surgector devices are constructed using two monolithic compound chips each consisting of a thyristor whose gate region contains a special diffused section which acts as a zener diode. This chips are connected in anti parallel, providing bidirectional protection. This zener diode section permits anode voltage turn on of the structure.

Initial clamping by the zener diode section, and fast turn on by the thyristor, provide excellent voltage limiting even on very fast rise time transients. The thyristor also features very high holding current, which allows the surgector to recover to its high impedance off state after a transient.

All these devices are supplied in a 2 lead, modified TO-202 VERSATAB package.

Equivalent Schematic Symbols

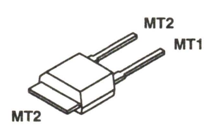


8

SURGECTOR PRODUCTS

Packaging

MODIFIED TO-202



File Number 3603.2

Absolute Maximum Ratings $T_C = 25^oC$

		SGT27B27, SGT27B27A SGT27B27B	UNITS
Continuous Off State Voltage:			
V_{DM}		235	V
V_{RM}		235	V
Transient Peak Surge Current	I_{TSM}		
1µs x 2µs (Note 1)		600	A
8µs x 20µs		400	A
10µs x 560µs		250	A
10µs x 1000µs		200	A
One Half Cycle	50Hz to 60Hz (Note 2)	60	A
One Second	50Hz to 60Hz, Halfwave	30	A
Operating Temperature (T_A)		-40 to 85	^oC
Storage Temperature Range (T_{STG})		-40 to 150	^oC

NOTES:

1. Unit designed not to fail open below: 900A.
2. One every 30s maximum.

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications At Case Temperature, $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Off-State Current	I_{DM}, I_{RM}	Maximum Rated V_{DM}, V_{RM}				
		$T_A = 25^oC$	-	-	200	nA
		$T_A = 85^oC$	-	-	100	µA
Clamping Voltage	V_Z	$I_Z < 200\mu A$				
SGT27B27			270	-	325	V
SGT27B27A			270	-	340	V
SGT27B27B			270	-	355	V
Breakover Voltage	V_{BO}	dv/dt = 100V/µs				
SGT27B27			-	-	345	V
SGT27B27A			-	-	360	V
SGT27B27B			-	-	375	V
Holding Current	I_H		270	-	-	mA
On-State Voltage	V_T	$I_T = 10A$	-	-	2	V
Main Terminal Capacitance	C_O	$V_{DM} = V_{RM} = 50V$, Frequency = 1MHz	-	80	-	pF

Performance Curves

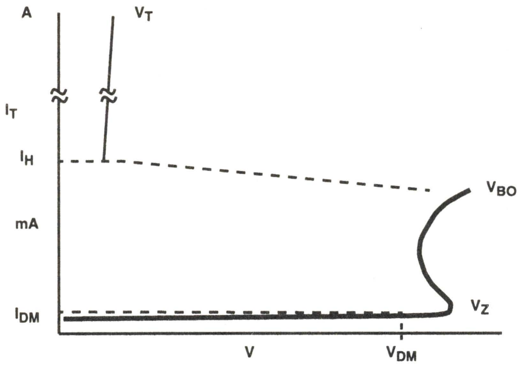


FIGURE 1. TYPICAL VOLT-AMPERE CHARACTERISTICS FOR ALL TYPES

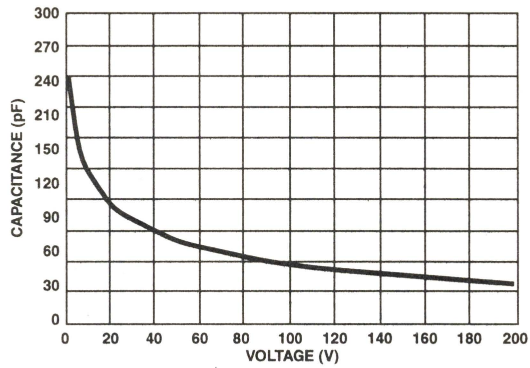


FIGURE 2. TYPICAL CAPACITANCE vs VOLTAGE FOR ALL TYPES

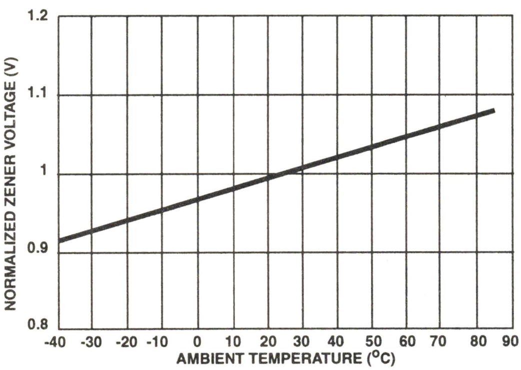


FIGURE 3. NORMALIZED ZENER VOLTAGE vs TEMPERATURE FOR ALL TYPES

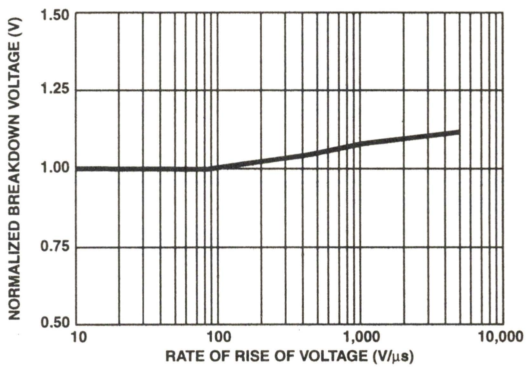


FIGURE 4. NORMALIZED V_{BO} vs dv/dt FOR ALL TYPES

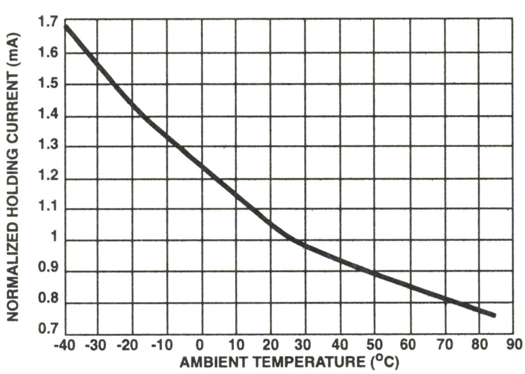


FIGURE 5. NORMALIZED HOLDING CURRENT vs TEMPERATURE FOR ALL TYPES

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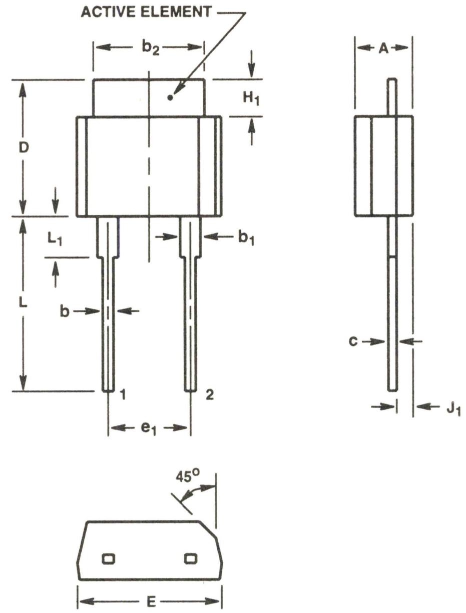
SURGECTOR PRODUCTS

Mechanical Dimensions



TO-202 Modified

2 LEAD JEDEC STYLE TO-202 SHORT TAB PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.130	0.150	3.31	3.81	-
b	0.024	0.028	0.61	0.71	2, 3
b_1	0.045	0.055	1.15	1.39	1, 2, 3
b_2	0.270	0.280	6.86	7.11	-
c	0.018	0.022	0.46	0.55	1, 2, 3
D	0.320	0.340	8.13	8.63	-
E	0.340	0.360	8.64	9.14	-
e_1	0.200 BSC		5.08 BSC		4
H_1	0.080	0.100	2.04	2.54	-
J_1	0.039	0.049	1.00	1.24	5
L	0.410	0.440	10.42	11.17	-
L_1	0.080	0.100	2.04	2.54	1

NOTES:

1. Lead dimension and finish uncontrolled in L_1.
2. Lead dimension (without solder).
3. Add typically 0.002 inches (0.05mm) for solder coating.
4. Position of lead to be measured 0.250 inches (6.35mm) from bottom of dimension D.
5. Position of lead to be measured 0.100 inches (2.54mm) from bottom of dimension D.
6. Controlling dimension: Inch.
7. Revision 3 dated 10-94.

Nomenclature

SGT 27 B 27 X

- X — **V_Z/V_{BO} Variant**
  - Blank: Lower Value
  - A, B: Higher Value
- 27 — Holding Current in mA divided by 10
- B — **Type of Surgector**
  - U: Unidirectional
  - S: SCR
  - B: Bidirectional
- 27 — Off-State Voltage Rating Divided by 10
- SGT — Surgector

Terms and Symbols

V_{DM} (Maximum Off-State Voltage) - Maximum off-state voltage (DC or peak) which may be applied continuously.

V_{RM} (Maximum Reverse Voltage) - Maximum reverse-blocking voltage (DC or peak) which may be applied.

I_{TSM} (Maximum Peak Surge Current) - Maximum nonrepetitive current which may be allowed to flow for the time state.

T_A (Ambient Operating Temperature) - Ambient temperature range permitted during operation in a circuit.

T_{STG} (Storage Temperature) - Temperature range permitted during storage.

I_{DM} (Off-State Current) - Maximum value of off-state current that results from the application of the maximum off-state voltage (V_{DM}).

I_{RM} (Reverse Current) - Maximum value of reverse current that results from the application of the maximum reverse voltage (V_{RM}).

V_Z (Clamping Voltage) - Off-state voltage at a specified current.

V_{BO} (Breakdown Voltage) - Voltage at which the device switches from the off-state to the on-state.

I_H (Holding Current) - Minimum on-state current that will hold the device in the on-state after it has been latched on.

V_T (On-State Voltage) - Voltage across the main terminals for a specified on-state current.

C_O (Main Terminal Capacitance) - Capacitance between the main terminals at a specified off-state voltage.

HARRIS SEMICONDUCTOR

SGT27S23

Gate Controlled Unidirectional Transient Surge Suppressor (Surgector)

January 1998

Features

- Blocking Voltage 270V
- Peak Transient Surge Current 300A
- Minimum Holding Current 230mA
- Subnanosecond Clamping Action
- Low On-State Voltage
- UL Recognize File # E135010 to STD 497B

Applications

- Telecommunications Equipment
- Data and Voice Lines
- Computer Modems
- Alarm Systems

Description

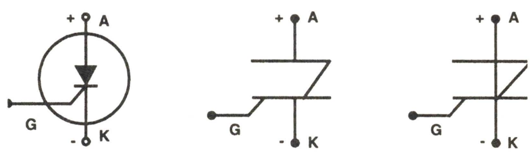
Surgector transient surge protectors are designed to protect telecommunication equipment, data links, alarm systems, power supplies, and other sensitive electrical circuits from damage that could be caused by switching transients, lightning strikes, load changes, commutation spikes, and line crosses.

These devices are fast turn-on, high holding current thyristors. When coupled with a user supplied voltage level detector, they provide excellent voltage limiting even on very fast rise time transients. The high holding current allows this surgector to return to its high-impedance off state after a transient.

The surgector device's normal off state condition in the forward blocking mode is a high impedance, low leakage state that prevents loading of the line.

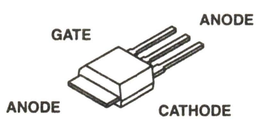
The SGT27S23 is supplied in a 3 lead, modified, TO-202 package.

Equivalent Schematic Symbols



Packaging

MODIFIED TO-202



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **2762.2**

Absolute Maximum Ratings $T_C = 25^oC$

	SGT27S23	UNITS
Continuous Off State Voltage:		
V_{DM}	270	V
V_{RM}	1	V
Transient Peak Surge Current: I_{TSM}		
1µs x 2µs (Note 1)	300	A
8µs x 20µs	200	A
10µs x 560µs	125	A
10µs x 1000µs	100	A
One Half Cycle . . . 50Hz to 60Hz (Note 2)	60	A
One Second . . . 50Hz to 60Hz, Halfwave	30	A
Operating Temperature (T_A)	-40 to 85	^oC
Storage Temperature Range (T_{STG})	-40 to 150	^oC

NOTES:

1. Unit designed not to fail open below: 450A.
2. One every 30s maximum.

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications
At Case Temperature, $T_C = 25^oC$, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Off-State Current	I_{DM}	$V_{DM} = 270V$ at $T_C = 85^oC$	- -	- -	100 50	nA µA
	I_{RM}	$V_{RM} = 1V$ at $T_C = 85^oC$	- -	- -	1 10	mA mA
Holding Current	I_H		230	-	-	mA
On-State Voltage	V_T	$I_T = 10A$	-	-	2	V
Gate Trigger Current	I_{GT}		-	-	175	mA
Main Terminal Capacitance	C_O	$V_{DM} = 0V$, Freq = 1MHz $V_{DM} = 50V$	- -	90 50	- -	pF pF

Performance Curves

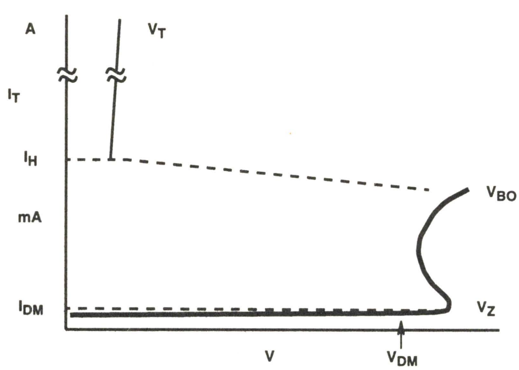


FIGURE 1. TYPICAL VOLT-AMPERE CHARACTERISTICS

Performance Curves

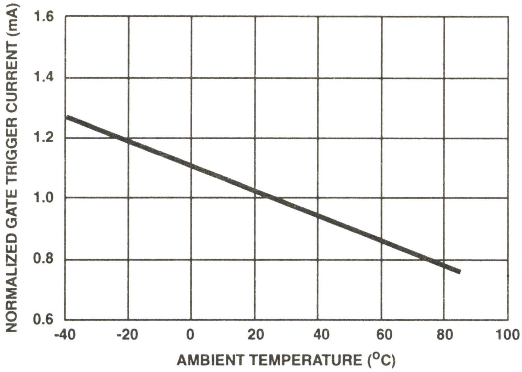


FIGURE 2. NORMALIZED GATE TRIGGER CURRENT vs TEMPERATURE

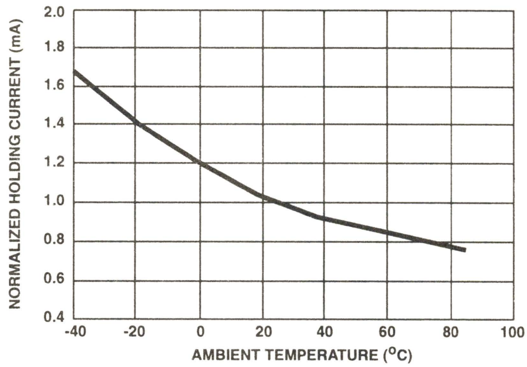


FIGURE 3. NORMALIZED HOLDING CURRENT vs TEMPERATURE

Terms and Symbols

V_{DM} **(Maximum Off-State Voltage) -** Maximum off-state voltage (DC or peak) which may be applied continuously.

V_{RM} **(Maximum Reverse Voltage) -** Maximum reverse-blocking voltage (DC or peak) which may be applied.

I_{TSM} **(Maximum Peak Surge Current) -** Maximum nonrepetitive current which may be allowed to flow for the time state.

T_A **(Ambient Operating Temperature) -** Ambient temperature range permitted during operation in a circuit.

T_{STG} **(Storage Temperature) -** Temperature range permitted during storage.

I_{DM} **(Off-State Current) -** Maximum value of off-state current that results from the application of the maximum off-state voltage (V_{DM}).

I_{RM} **(Reverse Current) -** Maximum value of reverse current that results from the application of the maximum reverse voltage (V_{RM}).

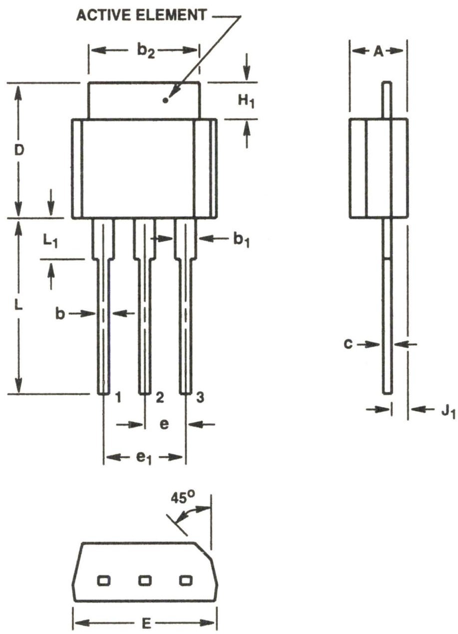
I_{GT} **(Gate-Trigger Current) -** Minimum gate current which will cause the device to switch from the off-state to the on-state.

I_H **(Holding Current) -** Minimum on-state current that will hold the device in the on-state after it has been latched on.

V_T **(On-State Voltage) -** Voltage across the main terminals for a specified on-state current.

C_O **(Main Terminal Capacitance) -** Capacitance between the main terminals at a specified off-state voltage.

Mechanical Dimensions



TO-202 Modified

3 LEAD JEDEC STYLE TO-202 SHORT TAB PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.130	0.150	3.31	3.81	-
b	0.024	0.028	0.61	0.71	2, 3
b_1	0.045	0.055	1.15	1.39	1, 2, 3
b_2	0.270	0.280	6.86	7.11	-
c	0.018	0.022	0.46	0.55	1, 2, 3
D	0.320	0.340	8.13	8.63	-
E	0.340	0.360	8.64	9.14	-
e	0.100 TYP		2.54 TYP		4
e_1	0.200 BSC		5.08 BSC		4
H_1	0.080	0.100	2.04	2.54	-
J_1	0.039	0.049	1.00	1.24	5
L	0.410	0.440	10.42	11.17	-
L_1	0.080	0.100	2.04	2.54	1

NOTES:

1. Lead dimension and finish uncontrolled in L_1.
2. Lead dimension (without solder).
3. Add typically 0.002 inches (0.05mm) for solder coating.
4. Position of lead to be measured 0.250 inches (6.35mm) from bottom of dimension D.
5. Position of lead to be measured 0.100 inches (2.54mm) from bottom of dimension D.
6. Controlling dimension: Inch.
7. Revision 3 dated 10-94.

Nomenclature

SGT 27 S 23

- 23 — Holding Current in mA divided by 10
- S — **Type of Surgector**
  - U: Unidirectional
  - B: Bidirectional
  - S: SCR
- 27 — Off-State Voltage Rating Divided by 10
- SGT — Surgector

TVS 9

ARRESTER PRODUCT SERIES

PAGE

Arrester Product Series Overview

The products in this section are primarily intended for the Lightning Arrester Market. Typically, the Arrester OEM will integrate one or more of the AS Series "blocks" within a cylindrical housing assembly. AS blocks are often stacked to achieve the specific MCOV rating required for high voltage, AC utility power distribution/transformer applications. The AS Series is characterized to specific parameters of the Arrester industry.

Transient Voltage Suppressor Device Selection Guide

MARKET SEGMENT	TYPICAL APPLICATIONS AND CIRCUITS EXAMPLES	DEVICE FAMILY OR SERIES	DATA BOOK SECTION	TECHNOLOGY	SURFACE MOUNT PRODUCT?
Low Voltage, Board Level Products	• Hand-Held/Portable Devices • EDP • Computer • I/O Port and Interfaces • Controllers • Instrumentation • Remote Sensors • Medical Electronics, etc.	CH	4	MOV	✓
		MA, ZA, RA	4	MOV	
		ML, MLE	5	Multilayer Suppressor	✓
		SP72X	6	SCR/Diode Array	✓ †
AC Line TVSS Products	• UPS • AC Panels • AC Power Taps • TVSS Devices • AC Appliance/Controls • Power Meters • Power Supplies • Circuit Breakers • Consumer Electronics	UltraMOV™ "C" III, LA, HA, RA	4	MOV	
		CH	4	MOV	✓
		GDT	7	Gas Discharge Tube	
Automotive Electronics	• ABS • EEC • Instrument Cluster • Air Bag • Window Control • Wiper Modules • Multiplex Bus • EFI	CH	4	MOV	✓
		ZA	4	MOV	
		AUML, ML	5	Multilayer Suppressor	✓
		SP72X	6	SCR/Diode Array	✓ †
Telecommunications Products	• Cellular/Cordless Phone • Modems • Secondary Phone Line Protectors • Data Line Connectors • Repeaters • Line Cards	CH	4	MOV	✓
		CP, CS, ZA	4	MOV	
		ML, MLE	5	Multilayer Suppressor	✓
		SP72X	6	SCR/Diode Array	✓ †
		GDT	7	Gas Discharge Tube	
		Surgector	8	Thyristor/Zener	
Industrial, High Energy AC Products	• High Current Relays • Solenoids • Motor Drives • AC Distribution Panels • Robotics • Large Motors	DA/DB, BA/BB, CA, HA, NA, PA	4	MOV	
		GDT	7	Gas Discharge Tube	
Arrester Products	• Lightning Arrester Assemblies for High Voltage AC Power Distribution Lines and Utility Transformers	**AS**	**9**	**MOV**	

† Available in both surface mount and through-hole packages.

HARRIS SEMICONDUCTOR

AS Series

High Energy Metal-Oxide Arrester Blocks

January 1998

Features

- Provided in Disc Form for Unique Packaging by Customer
- Electrode Finish Enables Pressure Contact for Stacking Application
- Available Disc Sizes: 32mm, 42mm and 60mm Diameter
- No Follow Current
- High Surge Current Capability
- Conforms to IEC 99-4 and ANSI/IEEE C62.11 Industry Standards
- Characterized for Lightning Arrester Parameters

Applications

- Lightning Protection of Electrical AC Distribution Transformers and Systems
- Arrester Assemblies of the Porcelain Polymeric, "Under-oil" and Metal Clad Variety

Description

The AS Series of Arrester blocks is primarily designed to be used as the surge suppression element within a lightning arrester assembly. These arrester blocks provide the high peak surge current and energy ratings required for the protection of high voltage AC power utility distribution systems. Typically, these devices are placed within a special arrester housing provided by the customer, and stacked to achieve the necessary continuous working voltage ratings for the specific application. (See the CA or NA series of Varistor discs for lower voltage and energy applications.)

Packaging

AS SERIES

9 ARRESTER PRODUCT SERIES

Absolute Maximum Ratings For ratings of individual members of a series, see Device Ratings and Specifications chart

	AS SERIES	UNITS
Rated Voltage		
AC Voltage Range	3.00 to 6.00	kV
Steady State Applied Voltage:		
AC Voltage (MCOV)	2.55 to 5.10	kV
Transient		
Peak Pulse Current (I_{TM}) for 4/10 μs Current Wave	65 to 100	kA
Energy Rating for 2ms Current Wave	2.2 to 12	kJ
Operating Ambient Temperature (T_A)	60	^oC

STORAGE AND HANDLING NOTES:

1. Arrester blocks should be stored in a moisture free environment at all times.
2. Use caution during handling to prevent damage or chipping of edges of the arrester blocks.

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Device Ratings and Specifications 25°C Unless Otherwise Specified

PARAMETER	PART NUMBER								UNITS
	V302AS32	V402AS32	V502AS32	V602AS32	V302AS42	V402AS42	V502AS42	V402AS60	
Rated Voltage (RMS)	3.0	4.0	5.0	6.0	3.0	4.0	5.0	4.0	kV
Maximum Continuous Operating Voltage (MCOV)	2.55	3.40	4.25	5.1	2.55	3.40	4.25	3.40	kV
Reference Current, I_{REF}	5.0	5.0	5.0	5.0	5.0	5.0	5.0	5.0	mA
Minimum Reference Voltage, V_{REF}	3.12	4.16	5.20	6.24	3.12	4.16	5.20	4.16	kV_{RMS}
Nominal Discharge Current, I_P (8/20μs)	5.0	5.0	5.0	5.0	10.0	10.0	10.0	10.0	kA
Residual Voltage (max) at I_P	9.8	13.1	16.3	19.6	10.0	13.3	16.7	12.5	kV
Energy Rating at 60°C (2ms)	2.2	2.9	3.6	4.3	3.5	4.7	5.8	12.0	kJ
Peak Current, 4/10μs at 60°C (Note 4)	65.0	65.0	65.0	65.0	100.0	100.0	100.0	100.0	kA
Maximum Steep Current Residual Voltage at 5kA (1/20μs)	11.3	15.0	18.8	22.5	-	-	-	-	kV
Maximum Steep Current Residual Voltage at 10kA (1/20μs)	-	-	-	-	11.5	15.3	19.2	14.4	kV
Maximum Dissipation Power at MCOV	0.23	0.30	0.38	0.45	0.36	0.48	0.60	0.50	W
Maximum Conduction Current at MCOV	75.0	75.0	75.0	75.0	110.0	110.0	110.0	140.0	μA

NOTES:

3. In addition to above standard types, custom ratings and dimensions can be provided.
4. Parts should be wrapped using a secondary insulating film or encased by polymeric housing.

Performance Curves

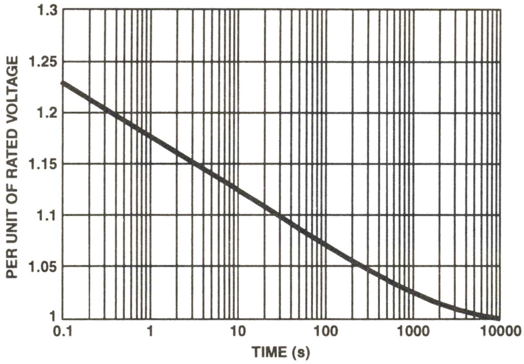


FIGURE 1. TEMPORARY OVERVOLTAGE CAPABILITY (TOV) FOR AS SERIES ARRESTERS

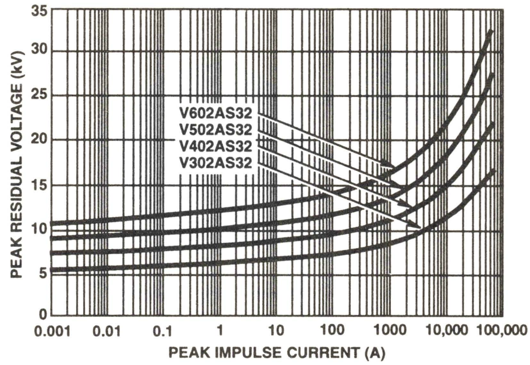


FIGURE 2. V-I CHARACTERISTIC AS32 SIZE

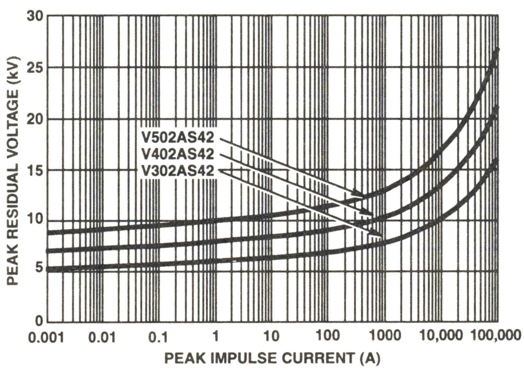


FIGURE 3. V-I CHARACTERISTIC AS42 SIZE

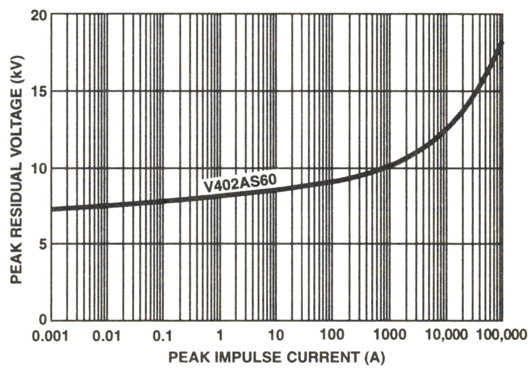
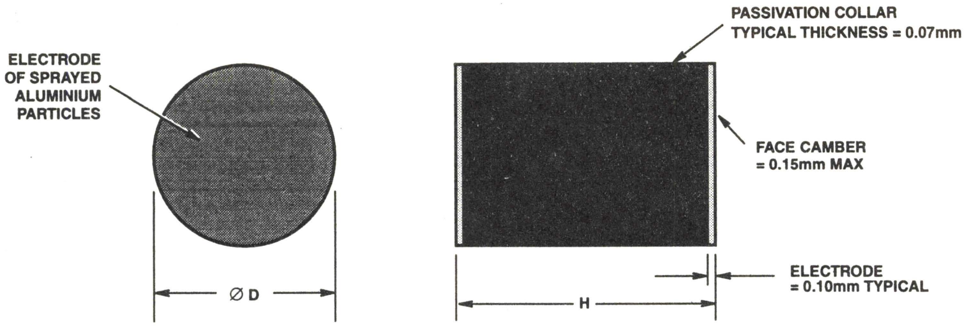


FIGURE 4. V-I CHARACTERISTIC AS60 SIZE

Dimensions

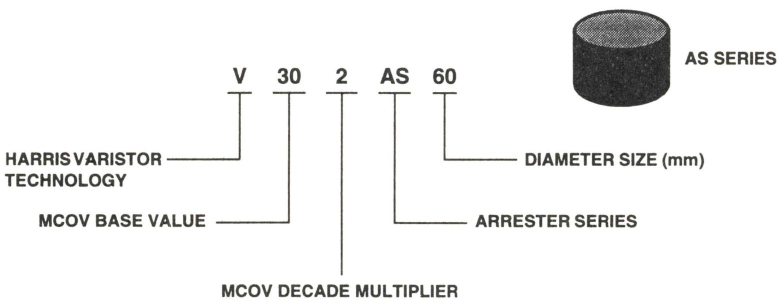


DIMENSIONS (IN MILLIMETERS)

PARAMETER	PART NUMBER								UNITS
	V302AS32	V402AS32	V502AS32	V602AS32	V302AS42	V402AS42	V502AS42	V402AS60	
Diameter (∅D) Min	32.3	32.3	32.3	32.3	40.9	40.9	40.9	60.0	mm
Max	33.7	33.7	33.7	33.7	42.3	42.3	42.3	62.0	mm
Height (H) Min	20.0	27.0	34.0	41.0	20.0	27.0	34.3	35.3	mm
Max	21.5	28.5	35.5	42.5	21.5	28.5	35.8	36.8	mm

Ordering Information

VXXX ASXX TYPES



TVS 10

HIGH RELIABILITY SERIES

High Reliability Varistors

High Reliability Series Mechanical and Environmental Testing for Aerospace, Military and High Reliability Applications

The high reliability Harris varistor is the latest step in increased product performance, and is available for applications requiring quality and reliability assurance levels consistent with military or other standards. (MIL-STD-19500, MIL-S-750, Method 202). Additionally, Harris varistors are inherently radiation hardened compared to silicon diode suppressors as illustrated in Figure 1.

This series of high-reliability varistors involve five categories:

- DESC Qualified Parts List (QPL) MIL-R-83530
  4 types presently available
- DESC Standard Military Drawings based on MIL-R-83530
  63 types presently available:
  - ZA Series - Drawing #87063
  - DB Series - Drawing #90065
- Harris high reliability series offers TX equivalents
  29 types presently available
- Custom types processed to customer-specific requirements - (SCD) or to standard military flow
- SP720 - High Reliability Electronic Protection Array

Credentials

Harris varistors and quality management systems are:

- DESC approved
- QPL listed
- CECC certified
- ISO approved
- UL listed
- CSA listed

DESC Qualified Parts List (QPL) MIL-R-83530

TABLE 1. MIL-R-83530/1 RATINGS AND CHARACTERISTICS

PART NUMBER M83530/	NOMINAL VARISTOR VOLTAGE (V)	TOLERANCE (%)	VOLTAGE RATING (V) (RMS)	(DC)	ENERGY RATING (J)	CLAMPING VOLTAGE AT 100A (V)	CAPACITANCE AT 1MHz (pF)	CLAMPING VOLTAGE AT PEAK CURRENT RATING (V)	I_{TM} (A)	NEAREST COMMERCIAL EQUIVALENT
1-2000B	200	±10	130	175	50	325	3800	570	6000	V130LA20B
1-2200D	220	+10, -5	150	200	55	360	3200	650	6000	V150LA20B
1-4300E	430	+5, -10	275	369	100	680	1800	1200	6000	V275LA40B
1-5100E	510	+5, -10	320	420	120	810	1500	1450	6000	V320LA40B

This series of varistors are screened and conditioned in accordance with MIL-R-83530 as outlined in Table 2. Manufacturing system conforms to MIL-I-45208; MIL-Q-9858.

MIL-R-83530 Inspections

TABLE 2. MIL-R-83530 GROUP A, B, AND C INSPECTIONS

INSPECTION		AQL (PERCENT DEFECTIVE)	MAJOR	MINOR	NUMBER OF SAMPLE UNITS	FAILURES ALLOWED
Group A	SUBGROUP 1					
	High Temperature Life (Stabilization Bake)	100%	-	-	-	-
	Thermal Shock	100%	-	-	-	-
	Power Burn-In	100%	-	-	-	-
	Clamping Voltage	100%	-	-	-	-
	Nominal Varistor Voltage	100%	-	-	-	-
	SUBGROUP 2					
	Visual and Mechanical Examination	-	1.0% AQL 7.6% LQ	25% AQL 13.0% LQ	Per Plan	-
	Body Dimensions	-			Per Plan	-
	Diameter and Length of Leads	-			Per Plan	-
	Marking	-			Per Plan	-
	Workmanship	-			Per Plan	-
	SUBGROUP 3					
	Solderability	-	-	-	Per Plan	-
Group B	SUBGROUP 1					
	Dielectric Withstanding Voltage	-	-	-	Per Plan	-
	SUBGROUP 2					
	Resistance to Solvents	-	-	-	Per Plan	-
	SUBGROUP 3					
	Terminal Strength (Lead Fatigue)	-	-	-	Per Plan	-
	Moisture Resistance	-	-	-	Per Plan	-
	Peak Current	-	-	-	Per Plan	-
	Energy	-	-	-	Per Plan	-
Group C	EVERY 3 MONTHS					
	High Temperature Storage	-	-	-	10	0
	Operating Life (Steady State)	-	-	-	10	0
	Pulse Life	-	-	-	10	0
	Shock	-	-	-	10	0
	Vibration	-	-	-	10	0
	Constant Acceleration	-	-	-	10	0
	Energy	-	-	-	10	0

DESC Standard Military Drawing # 87063

Based on MIL-R-83530

TABLE 3. ZA SERIES RATINGS AND SPECIFICATIONS

87063 DASH NO.	(SEE SECTION 4) NEAREST COMM. EQUIV.	(NOTE 1) SIZE	MAXIMUM RATINGS (85°C) CONTINUOUS RMS $V_{M(AC)}$ (V)	DC $V_{M(DC)}$ (V)	TRANSIENT ENERGY (10/1000µs) W_{TM} (J)	PEAK CURRENT (8/20µs) I_{TM} (A)	SPECIFICATIONS (25°C) VARISTOR VOLTAGE AT 1mA$_{DC}$ TEST CURRENT MIN (V)	$V_{N(DC)}$ (V)	MAX (V)	MAXIMUM CLAMPING VOLTAGE V_C AT TEST CURRENT (8/20µs) V_C (V)	I_C (A)	TYPICAL CAPACITANCE f = 1MHz (pF)
001	V22ZA05	1	14	18	0.2	35	18.7	22	26	51	2	400
002	V22ZA1	2	14	18	0.9	150	18.7	22	26	47	5	1600
003	V22ZA2	3	14	18	2.0	350	18.7	22	26	43	5	4000
004	V22ZA3	4	14	18	4.0	750	18.7	22	26	43	10	9000
005	V24ZA50	5	14	18	6.5	1500	19.2	24 (Note 2)	26	43	20	18000
006	V27ZA05	1	17	22	0.25	35	23	27	31.1	59	2	300
007	V27ZA1	2	17	22	1.0	150	23	27	31.1	57	5	1300
008	V27ZA2	3	17	22	2.5	350	23	27	31.1	53	5	3000
009	V27ZA4	4	17	22	5.0	750	23	27	31.1	53	10	7000
010	V27ZA60	5	17	22	8.0	1500	23	27 (Note 2)	31.1	50	20	15000
011	V33ZA05	1	20	26	0.3	35	29.5	33	38	67	2	250
012	V33ZA1	2	20	26	1.2	150	29.5	33	36.5	68	5	1100
013	V33ZA2	3	20	26	3.0	350	29.5	33	36.5	64	5	2700
014	V33ZA5	4	20	26	6.0	750	29.5	33	36.5	64	10	6000
015	V33ZA70	5	21	27	9.0	1500	29.5	33 (Note 2)	36.5	58	20	13000
016	V36ZA80	5	23	31	10.0	1500	32	36 (Note 2)	40	63	20	12000
017	V39ZA05	1	25	31	0.35	35	35	39	46	79	2	220
018	V39ZA1	2	25	31	1.5	150	35	39	43	79	5	900
019	V39ZA3	3	25	31	3.5	350	35	39	43	76	5	2200
020	V39ZA6	4	25	31	7.2	750	35	39	43	76	10	5000
021	V47ZA05	1	30	38	0.4	35	42	47	55	90	2	200
022	V47ZA1	2	30	38	1.8	150	42	47	52	92	5	800
023	V47ZA3	3	30	38	4.5	350	42	47	52	89	5	2000
024	V47ZA7	4	30	38	8.8	750	42	47	52	89	10	4500
025	V56ZA05	1	35	45	0.5	35	50	56	66	108	2	180

TABLE 3. ZA SERIES RATINGS AND SPECIFICATIONS (Continued)

87063 DASH NO.	(SEE SECTION 4) NEAREST COMM. EQUIV.	(NOTE 1) SIZE	MAXIMUM RATINGS (85°C) CONTINUOUS RMS		TRANSIENT ENERGY (10/1000μs)	PEAK CURRENT (8/20μs)	SPECIFICATIONS (25°C) VARISTOR VOLTAGE AT 1mA$_{DC}$ TEST CURRENT			MAXIMUM CLAMPING VOLTAGE V_C AT TEST CURRENT (8/20μs)		TYPICAL CAPACITANCE
			RMS	DC								
			$V_{M(AC)}$	$V_{M(DC)}$	W_{TM}	I_{TM}	MIN	$V_{N(DC)}$	MAX	V_C	I_C	f = 1MHz
			(V)	(V)	(J)	(A)	(V)	(V)	(V)	(V)	(A)	(pF)
026	V56ZA2	2	35	45	2.3	150	50	56	62	107	5	700
027	V56ZA3	3	35	45	5.5	350	50	56	62	103	5	1800
028	V56ZA8	4	35	45	10.0	750	50	56	62	103	10	3900
029	V68ZA05	1	40	56	0.6	35	61	68	80	127	2	150
030	V68ZA2	2	40	56	3.0	150	61	68	75	127	5	600
031	V68ZA3	3	40	56	6.5	350	61	68	75	123	5	1500
032	V68ZA10	4	40	56	13.0	750	61	68	75	123	10	3300
033	V82ZA05	1	50	66	1.2	70	73	82	97	145	2	120
034	V82ZA2	2	50	66	3.5	300	73	82	91	135	10	500
035	V82ZA4	3	50	66	7.3	750	73	82	91	135	25	1100
036	V82ZA12	4	50	66	13.0	1500	73	82	91	145	50	2500
037	V100ZA05	1	60	81	1.5	70	90	100	117	175	2	90
038	V100ZA3	2	60	81	4.3	300	90	100	110	165	10	400
039	V100ZA4	3	60	81	8.9	750	90	100	110	165	25	900
040	V100ZA15	4	60	81	16.0	1500	90	100	110	175	50	2000
041	V120ZA05	1	75	102	1.8	100	108	120	138	205	2	70
042	V120ZA1	2	75	102	5.3	400	108	120	132	205	10	300
043	V120ZA4	3	75	102	11.0	1000	108	120	132	200	25	750
044	V120ZA6	4	75	102	19.0	2000	108	120	132	210	50	1700
045	V150ZA05	1	92	127	2.3	100	135	150	173	240	2	60
046	V150ZA1	2	95	127	6.5	400	135	150	165	250	10	250
047	V150ZA4	3	95	127	13.0	1000	135	150	165	250	25	600
048	V150ZA8	4	95	127	23.0	2000	135	150	165	255	50	1400
049	V180ZA05	1	110	153	2.7	150	162	180	207	290	2	50
050	V180ZA1	2	115	153	7.7	500	162	180	198	295	10	200
051	V180ZA5	3	115	153	16.0	1500	162	180	198	300	25	500
052	V180ZA10	4	115	153	27.0	3000	162	180	198	300	50	1100

NOTES:

1. Size 1-5mm, 2-7mm, 3-10mm, 4-14mm, 5-20mm radial lead ZA Series varistors.
2. 10mA DC test current.

DESC Standard Military Drawing # 90065

Based on MIL-R-83530

TABLE 4. DB SERIES RATINGS AND SPECIFICATIONS

90065 DASH NO.	VOLTAGE RATING MAX. (RMS)	ENERGY MAX (J)	PEAK CURRENT (A)	NOMINAL VARISTOR VOLTAGE (V)		MAX CLAMPING VOLTAGE AT TEST CURRENT		TYPICAL CAPACITANCE (pF)
						(V)	(I)	
012	130	170	22500	200	+28, -16	345	200	10000
013	150	200	22500	240	±28	405	200	8000
014	250	270	22500	390	+39, -36	650	200	5000
015	275	300	22500	430	±43	730	200	4500
016	320	350	22500	510	+29, -48	830	200	3800
017	420	460	28800	680	+68, -70	1130	200	3000
018	480	510	28800	750	+74, -80	1240	200	2700
019	510	550	28800	820	+91, -85	1350	200	2500
020	575	600	28800	910	+95, -105	1480	200	2200
021	660	690	28800	1050	±110	1720	200	2000
022	750	810	28800	1200	±120	2000	200	1800

NOTE: See Section 4 (DB Series) for nearest equivalent commercial type.

Harris High Reliability Series TX Equivalents

TABLE 5. AVAILABLE TX MODEL TYPES

TX MODEL	MODEL SIZE	DEVICE MARK	(SEE SECTION 4) NEAREST COMMERCIAL EQUIVALENT
V8ZTX1	7mm	8TX1	V8ZA1
V8ZTX2	10mm	8TX2	V8ZA2
V12ZTX1	7mm	12TX1	V12ZA1
V12ZTX2	10mm	12TX2	V12ZA2
V22ZTX1	7mm	22TX1	V22ZA1
V22ZTX3	14mm	22TX3	V22ZA3
V24ZTX50	20mm	24TX50	V24ZA50
V33ZTX1	7mm	33TX1	V33ZA1
V33ZTX5	14mm	33TX5	V33ZA5
V33ZTX70	20mm	33TX70	V33ZA70
V68ZTX2	7mm	68TX2	V68ZA2
V68ZTX10	14mm	68TX10	V68ZA10
V82ZTX2	7mm	82TX2	V82ZA2
V82ZTX12	14mm	82TX12	V82ZA12

TX MODEL	MODEL SIZE	DEVICE MARK	(SEE SECTION 4) NEAREST COMMERCIAL EQUIVALENT
V130LTX2	7mm	130TX	V130LA2
V130LTX10A	14mm	130TX10	V130LA10A
V130LTX20B	20mm	130TX20	V130LA20A
V150LTX2	7mm	150TX	V150LA2
V150LTX10A	14mm	150TX10	V150LA10A
V150LTX20B	20mm	150TX20	V150LA20B
V250LTX4	7mm	250TX	V250LA4
V250LTX20A	14mm	250TX20	V250LA20A
V250LTX40B	20mm	250TX40	V250LA40B
V420LTX20A	14mm	420TX20	V420LA20A
V420LTX40B	20mm	420TX40	V420LA40B
V480LTX40A	14mm	480TX40	V480LA40A
V480LTX80B	20mm	480TX80	V480LA80B
V510LTX40A	14mm	510TX40	V510LA40A
V510LTX80B	20mm	510TX80	V510LA80B

The TX series of varistors are 100% screened and conditioned in accordance with MIL-STD-750. Tests are as outlined in Table 6.

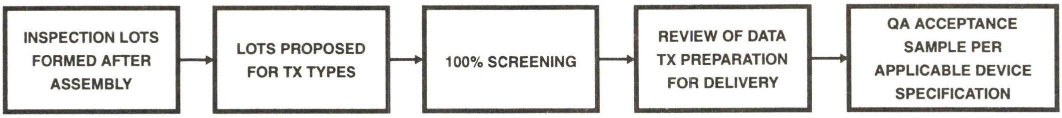


TABLE 6. TX EQUIVALENTS SERIES 100% SCREENING

SCREEN	MIL-STD-750 METHOD	CONDITION	TX REQUIREMENTS
High Temperature Life (Stabilization Bake)	1032	24 hours min. at max. rated storage temperature.	100%
Thermal Shock (Temperature Cycling)	1051	No dwell is required at 25°C. Test condition A1, 5 cycles -55°C to 125 °C (extremes). >10 minutes	100%
Humidity Life		85°C, 85% R.H., 168 hours.	100%
Interim Electrical $V_{N(DC)}$ V_C (Note 1)		As specified, but including delta parameter as a minimum.	100% Screen
Power Burn-In	1038	Condition B, 85°C, Rated $V_{M(AC)}$, 72 hours min	100%
Final Electrical +$V_{N(DC)}$ V_C (Note 1)		As specified — All parameter measurements must be completed within 96 hours after removal from burn-in conditions.	100% Screen
External Visual Examination	2071	To be performed after complete marking.	100%

NOTE:

1. Delta Parameter - $V_{N(DC)}$
   Maximum allowable shift ±10% Max.
   Applicable lot PDA - 10% Max.
   Peak current and energy ratings are derated by 10% and 30%, respectively, from standard parts.

TABLE 7. QUALITY ASSURANCE ACCEPTANCE TEST

	MIL-STD-105		LTPD
	LEVEL	AQL	
Electrical (Bidirectional) $V_{N(DC)}$, V_C (Per Specifications Table)	II	0.1	-
Dielectric Withstand Voltage MIL-STD-202, Method 301, 2500V min. at 1.0µA_{DC}	-	-	15
Solderability MIL-STD-202, Method 208, no aging, non-activated	-	-	15

Custom Types

In addition to our comprehensive high-reliability series as referenced above, Harris can screen and condition to customer-specific requirements.

Additional mechanical and environmental capabilities are defined in Table 8.

TABLE 8. MECHANICAL AND ENVIRONMENTAL CAPABILITIES (TYPICAL CONDITIONS)

TEST NAME	TEST METHOD	DESCRIPTION
Terminal Strength	MIL-STD-750-2036	3 Bends, 90° Arc, 16oz. Weight
Drop Shock	MIL-STD-750-2016	1500g's, 0.5ms, 5 Pulses, X_1, V_1, Z_1
Variable Frequency Vibration	MIL-STD-750-2056	20g's, 100-2000Hz, X_1, V_1, Z_1
Constant Acceleration	MIL-STD-750-2006	V_2, 20,000g's Min
Salt Atmosphere	MIL-STD-750-1041	35°C, 24 hrs, 10-50g/m^2 Day
Soldering Heat/Solderability	MIL-STD-750-2031/2026	260°C, 10s, 3 Cycles, Test Marking
Resistance to Solvents	MIL-STD-202-215	Permanence, 3 Solvents
Flammability	MIL-STD-202-111	15s Torching, 10s to Flameout
Flammability	UL1414	3 x 15s Torching
Cyclical Moisture Resistance	MIL-STD-202-106	10 Days
Steady-State Moisture Resistance		85/85 96 Hrs.
Biased Moisture Resistance		Not Recommended for High-Voltage Types
Temperature Cycle	MIL-STD-202-107	-55°C to 125°C, 5 Cycles
High-Temperature Life (Nonoperating)	MIL-STD-750-1032	125°C, 24 Hrs.
Burn-In	MIL-STD-750-1038	Rated Temperature and V_{RMS}
Hermetic Seal	MIL-STD-750-1071	Condition D

Radiation Hardness

For space applications, an extremely important property of a protection device is its response to imposed radiation effects.

Electron Irradiation

A Harris MOV and a silicon transient suppression diode were exposed to electron irradiation. The V-I Curves, before and after test, are shown in Figure 1.

It is apparent that the Harris MOV was virtually unaffected, even at the extremely high dose of 10^8 rads, while the silicon transient suppression diode showed a dramatic increase in leakage current.

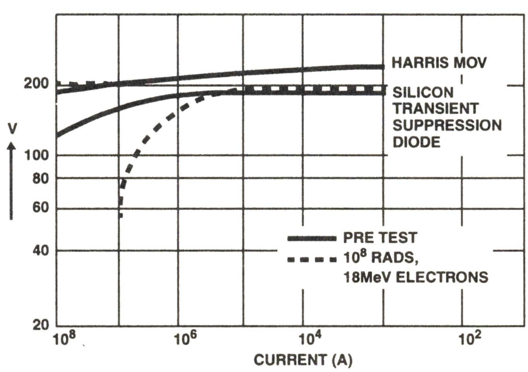


FIGURE 1. RADIATION SENSITIVITY OF HARRIS V130LA1 AND SILICON TRANSIENT SUPPRESSION DIODE

10 HIGH RELIABILITY SERIES

Neutron Effects

A second MOV-Zener comparison was made in response to neutron fluence. The selected devices were equal in area.

Figure 2 shows the clamping voltage response of the MOV and the zener to neutron irradiation to as high as 10^{15} N/cm^2. It is apparent that in contrast to the large change in the zener, the MOV is unaltered. At higher currents where the MOV's clamping voltage is again unchanged, the zener device clamping voltage increases by as much as 36%.

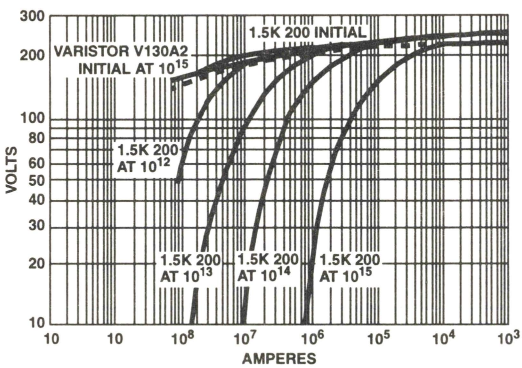


FIGURE 2. V-I CHARACTERISTIC RESPONSE TO NEUTRON IRRADIATION FOR MOV AND ZENER DIODE DEVICES

Counterclockwise rotation of the V-I characteristics is observed in silicon devices at high neutron irradiation levels; in other words, increasing leakage at low current levels and increasing clamping voltage at higher current levels.

The solid and open circles for a given fluence represent the high and low breakdown currents for the sample of devices tested. Note that there is a marked decrease in current (or energy) handling capability with increased neutron fluence.

Failure threshold of silicon semiconductor junctions is further reduced when high or rapidly increasing currents are applied. Junctions develop hot spots, which enlarge until a short occurs if current is not limited or quickly removed.

The characteristic voltage current relationship of a PN-Junction is shown in Figure 3.

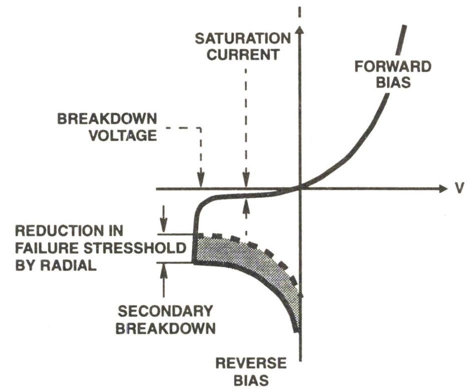


FIGURE 3. V-I CHARACTERISTIC OF PN-JUNCTION

At low reverse voltage, the device will conduct very little current (the saturation current). At higher reverse voltage V_{BO} (breakdown voltage), the current increases rapidly as the electrons are either pulled by the electric field (Zener effect) or knocked out by other electrons (avalanching). A further increase in voltage causes the device to exhibit a negative resistance characteristic leading to secondary breakdown.

This manifests itself through the formation of hotspots, and irreversible damage occurs. This failure threshold decreases under neutron irradiation for zeners, but not for Zinc Oxide Varistors.

Gamma Radiation

Radiation damage studies were performed on type V130LA2 varistors. Emission spectra and V-I characteristics were collected before and after irradiation with 10^6 rads Co^{60} gamma radiation.

Both show no change, within experimental error, after irradiation.

HARRIS SEMICONDUCTOR

SP720MD-8, SP720MD, SP720MM-8, SP720MM

High Reliability Electronic Protection Array for ESD and Overvoltage Protection

February 1998

Features

- The SP720MD-8 and SP720MM-8 are Harris Class B "Equivalent" Parts with Back-End Conformance to MIL-STD-883 for Final Assembly, Electrical Testing, Burn-In and QC Inspection
- ESD Interface Capability for HBM Standards
  - Modified MIL STD 3015.7 .... 15kV
  - MIL STD 3015.7 .... 6kV
  - IEC 1000-4-2, Direct Discharge,
    Single Input........................ 4kV (Level 2)
    Two Inputs in Parallel................ 8kV (Level 4)
  - IEC 1000-4-2, Air Discharge......... 15kV (Level 4)
- High Peak Current Capability
  - IEC 1000-4-5 .... +3A
  - Single Pulse, 100μs Pulse Width .... ±2A
  - Single Pulse, 4μs Pulse Width .... ±5A
- Designed to Provide Over-Voltage Protection
  - Single-Ended Voltage Range to .... +30V
  - Differential Voltage Range to .... ±15V
- Fast Switching .... 2ns Risetime
- Low Input Leakages............ 1nA at 25°C Typical
- Low Input Capacitance .... 3pF Typical
- An Array of 14 SCR/Diode Pairs
- Military Temperature Range .... -55°C to 125°C

Applications

- Microprocessor/Logic Input Protection
- Data Bus Protection
- Analog Device Input Protection
- Voltage Clamp

Description

The SP720 is a High Reliability Array of SCR/Diode bipolar structures for ESD and over-voltage protection to sensitive input circuits. The SP720 has 2 protection SCR/Diode device structures at each IN input. A total of 14 available IN inputs can be used to protect up to 14 external signal or bus lines. Over voltage protection is from the IN to V+ or V-. The SCR structures are designed for fast triggering at a threshold of one $+V_{BE}$ diode threshold above V+ or at a $-V_{BE}$ diode threshold below V-. From an IN input, a clamp to V+ is activated if a transient pulse causes the input to be increased to a voltage level greater than one V_{BE} above V+. A similar clamp to V- is activated if a negative pulse, one V_{BE} less than V-, is applied to an IN input.

The SP720MD-8 and SP720MM-8 Class B "Equivalent" Parts conform to MIL-STD-883 through final assembly, electrical test, burn-in and QC Inspection. The SP720MD and SP720MM are High Reliability Ceramic Packaged ICs.

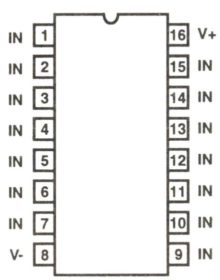
Refer to Application Note AN9304 for general application information and to AN9612 for further information on ESD and transient rating capabilities of the SP720.

Ordering Information

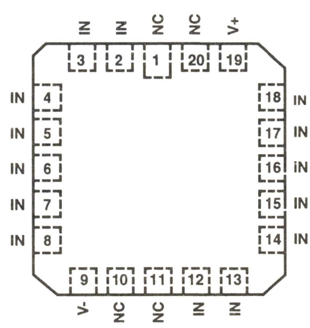
PART NO.	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
SP720MD-8	-55 to 125	16 Ld SBDIP	D16.3
SP720MD	-55 to 125	16 Ld SBDIP	D16.3
SP720MM-8	-55 to 125	20 Pad CLCC	J20.A
SP720MM	-55 to 125	20 Pad CLCC	J20.A

Pinouts

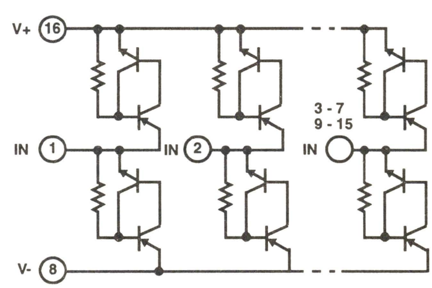
SP720MD (SBDIP) TOP VIEW



SP720MM (CLCC) TOP VIEW



Functional Block Diagram (SP720MD)



NOTE: The design of the SP720MD-8, SP720MD, SP720MM-8, and SP720MM SCR/Diode ESD Diode Protection Arrays is covered by Harris patent 4567500.

File Number **3683.6**

Absolute Maximum Ratings

Continuous Supply Voltage, [(V+) - (V-)] . . . . . . +35V
Max. DC Input Current, I_{IN} . . . . . . ±70mA
Input Peak Current, I_{IN} (Refer to Figure 3) . . . . . . ±2A, 100μs
ESD Capability, Refer to "ESD Capability" and Table 1, Figure 1

Operating Conditions

Operating Voltage Range, Single Supply . . . . . . +2V to +30V
Operating Voltage Range, Split Supply . . . . . . ±1V to ±15V
Typical Quiescent Supply Current 50nA
Operating Temperature Range . . . . . . -55°C to 125°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
16 Ld SBDIP Package	80	18
20 Pad CLCC Package	70	16

Maximum Storage Temperature Range . . . . . . -65°C to 150°C
Maximum Junction Temperature . . . . . . 175°C
Maximum Lead Temperature (Soldering 10s) . . . . . . 265°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

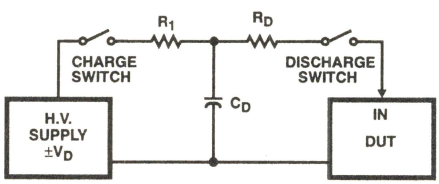
1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications T_A = -55°C to 125°C, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage Range	V_{SUPPLY}	V_{SUPPLY} = [(V+) - (V-)]	0	2 to 30	35	V
Peak Forward/Reverse Voltage Drop						
IN to V- (with V- Reference)	V_{IN} - (V-)	I_{IN} = -1A (1ms Peak Pulse)	-	-2	-	V
IN to V+ (with V+ Reference)	V_{IN} - (V+)	I_{IN} = +1A (1ms Peak Pulse)	-	+2	-	V
DC Forward/Reverse Voltage Drop						
IN to V- (with V- Reference)	V_{IN} - (V-)	I_{IN} = -100mA to V-	-1.5	-	-	V
IN to V+ (with V+ Reference)	V_{IN} - (V+)	I_{IN} = +100mA to V+	-	-	+1.5	V
Input Leakage Current	I_{IN}	V- < V_{IN} < V+, V_{SUPPLY} = 30V	-15	5	+15	nA
Quiescent Supply Current	$I_{QUIESCENT}$	V- < V_{IN} < V+, V_{SUPPLY} = 30V	-	50	150	nA
Equivalent SCR ON Threshold		Note 3	-	1.1	-	V
Equivalent SCR ON Resistance		V_{FWD}/I_{FWD} (Note 3)	-	1	-	Ω
Input Capacitance	C_{IN}		-	3	-	pF
Input Switching Speed	t_{ON}		-	2	-	ns

NOTES:

2. In automotive and battery operated systems, the power supply lines should be externally protected for load dump and reverse battery. When the V+ and V- pins are connected to the same supply voltage source as the device or control line under protection, a current limiting resistor should be connected in series between the external supply and the SP720 supply pins to limit reverse battery current to within the rated maximum limits. Bypass capacitors of typically 0.01μF or larger from the V+ and V- pins to ground are recommended.
3. Refer to the Figure 3 graph for definitions of equivalent "SCR ON Threshold" and "SCR ON Resistance". These characteristics are given here for thumb-rule information to determine peak current and dissipation under EOS conditions.



IEC 1000-4-2: R_1 50 to 100MΩ
MIL STD 3015.7: R_1 1 to 10MΩ

FIGURE 1. ELECTROSTATIC DISCHARGE TEST

TABLE 1. ESD TEST CONDITIONS

STANDARD	TYPE/MODE	R_D	C_D	±V_D
MIL STD 3015.7	Modified HBM	1.5kΩ	100pF	15kV
	Standard HBM	1.5kΩ	100pF	6kV
IEC 1000-4-2	HBM, air discharge	330Ω	150pF	15kV (Level 4)
	HBM, direct discharge	330Ω	150pF	4kV (Level 2)
	HBM, direct discharge, two parallel input pins	330Ω	150pF	8kV (Level 4)
EIAJ IC121	Machine Model	0kΩ	200pF	1kV

ESD Capability

ESD capability is dependent on the application and defined test standard. The evaluation results for various test standards and methods based on Figure 1 are shown in Table 1.

For the "Modified" MIL-STD-3015.7 condition that is defined as an "in-circuit" method of ESD testing, the V+ and V- pins have a return path to ground and the SP720 ESD capability is typically greater than 15kV from 100pF through 1.5kΩ. By strict definition of MIL-STD-3015.7 using "pin-to-pin" device testing, the ESD voltage capability is greater than 6kV. The MIL-STD-3015.7 results were determined from AT&T ESD Test Lab measurements.

The HBM capability to the IEC 1000-4-2 standard is greater than 15kV for air discharge (Level 4) and greater than 4kV for direct discharge (Level 2). Dual pin capability (2 adjacent pins in parallel) is well in excess of 8kV (Level 4).

For ESD testing of the SP720 to EIAJ IC121 Machine Model (MM) standard, the results are typically better than 1kV from 200pF with no series resistance.

Peak Transient Current Capability

The peak transient current capability rises sharply as the width of the current pulse narrows. Destructive testing was done to fully evaluate the SP720's ability to withstand a wide range of transient current pulses.

The test circuit shown in Figure 2 provides a positive pulse input. For a negative pulse input, the (-) current pulse input goes to an SP720 'IN' input pin and the (+) current pulse input goes to the SP720 V- pin. The V+ to V- supply of the SP720 must be allowed to float. (i.e. It is not tied to the ground reference of the current pulse generator.) Figure 3 shows the point of over-stress as defined by increased leakage in excess of the data sheet published limits.

The maximum peak input current capability is dependent on the V+ to V- voltage supply level, improving as the supply voltage is reduced. Values of 0, 5, 15 and 30 voltages are shown. The safe operating range of the transient peak current should be limited to no more than 75% of the measured over-stress level for any given pulse width as shown in Figure 3.

When adjacent input pins are paralleled, the sustained peak current capability is increased to nearly twice that of a single pin. For comparison, tests were run using dual pin combinations 1+2, 3+4, 5+6, 7+9, 10+11, 12+13 and 14+15. The over-stress curve is shown in Figure 3 for a 15V supply condition. The dual pins are capable of 10A peak current for a 10μs pulse and 4A peak current for a 1ms pulse. The complete curve for single pulse peak current vs. pulse width time ranging up to 1 second is shown in Figure 3.

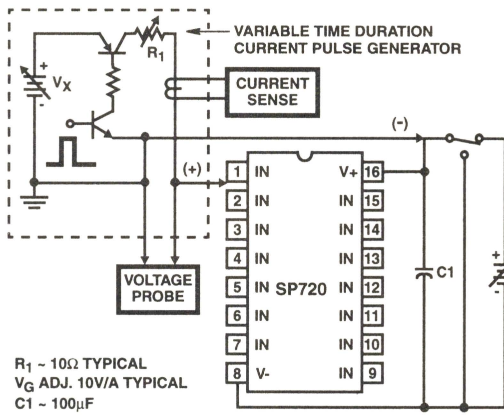


FIGURE 2. TYPICAL SP720 PEAK CURRENT TEST CIRCUIT WITH A VARIABLE PULSE WIDTH INPUT

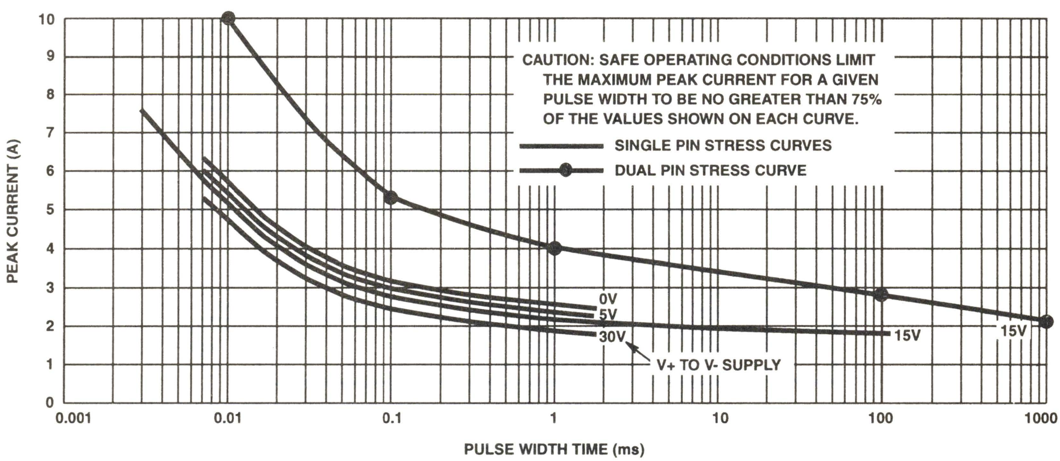


FIGURE 3. TYPICAL SINGLE PULSE PEAK CURRENT CURVES SHOWING THE MEASURED POINT OF OVER-STRESS IN AMPERES vs PULSE WIDTH TIME IN MILLISECONDS, ($T_A = 25^oC$)

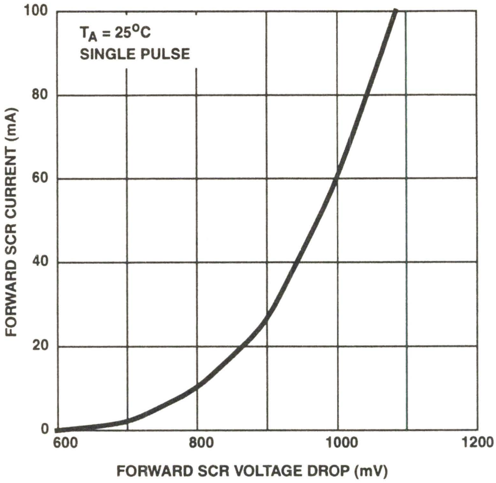


FIGURE 4. LOW CURRENT SCR FORWARD VOLTAGE DROP CURVE

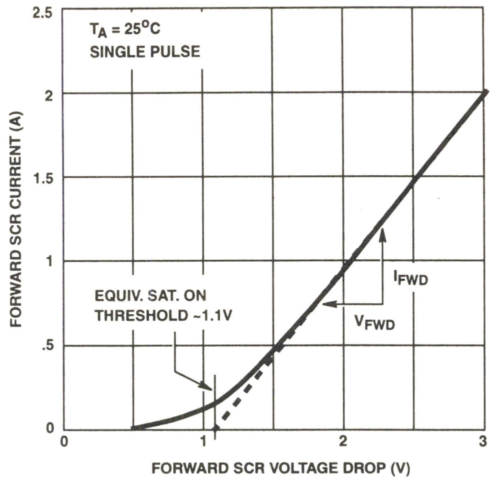


FIGURE 5. HIGH CURRENT SCR FORWARD VOLTAGE DROP CURVE

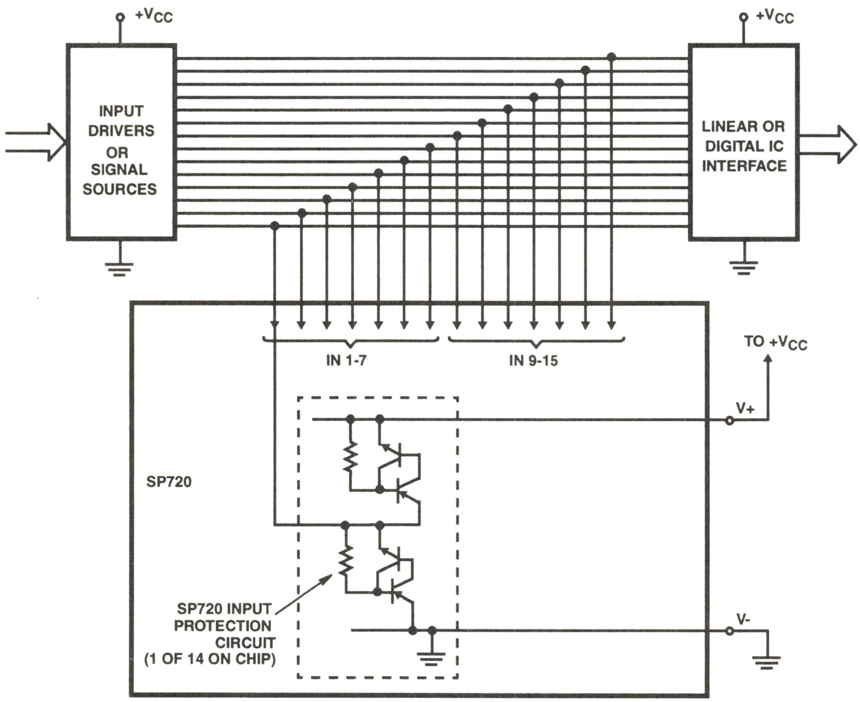


FIGURE 6. TYPICAL APPLICATION OF THE SP720 AS AN INPUT CLAMP FOR OVER-VOLTAGE, GREATER THAN $1V_{BE}$ ABOVE V+ OR LESS THAN $-1V_{BE}$ BELOW V-. PINOUT SHOWN IS FOR THE SP720MD SBDIP PACKAGE.

Power Dissipation Derating Curves

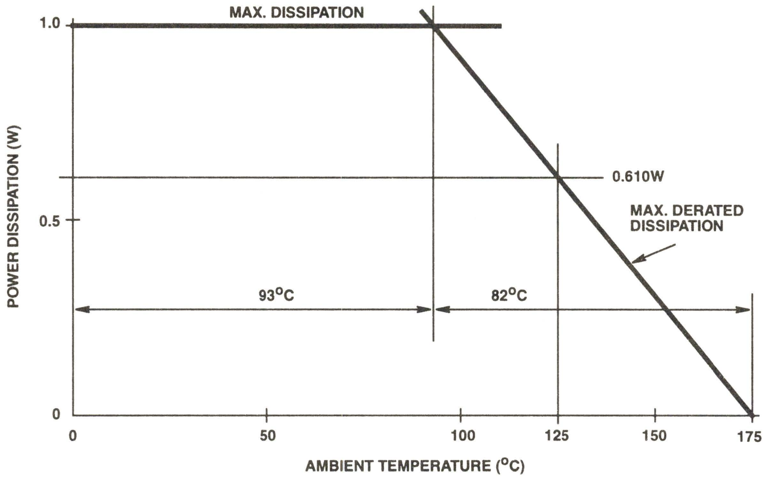


FIGURE 7. SP720MD DERATING CURVE FOR THE 82°C/W THERMAL RESISTANCE OF THE SIDEBRAZE 16 LEAD CERAMIC PACKAGE, DERATED 12.2mW/°C FROM A MAXIMUM P_D OF 1.0W AT 93°C

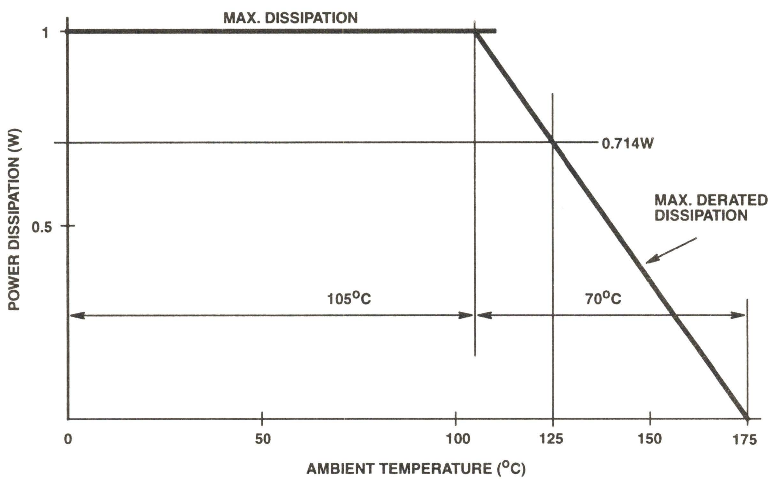
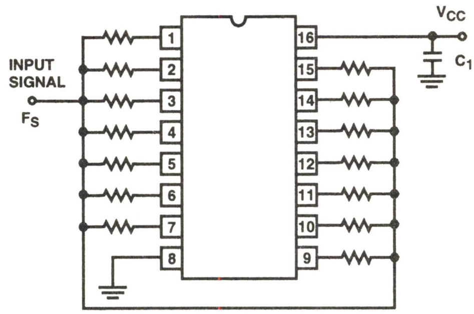


FIGURE 8. SP720MM DERATING CURVE FOR THE 70°C/W THERMAL RESISTANCE OF THE 20 PAD CERAMIC LCC PACKAGE, DERATED 14.3mW/°C FROM A MAXIMUM P_D OF 1.0W AT 105°C

SP720MD-8 and SP720MM-8 Dynamic Burn-In Circuits

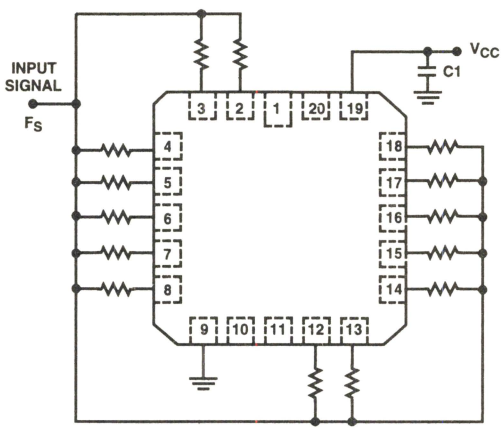
16 LEAD CERAMIC SBDIP

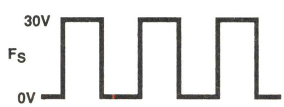


NOTES:

4. All resistors 1kΩ ±10%
5. V_{CC} = 30V ±1%
6. F_S = 0V to 30V ±1%, 50% Duty Cycle
7. C_1 = 22μF Min. Tantalum, 50WV (33WV at 125°C)
8. T_{AMB} = 125°C

20 PAD CLCC





Die Characteristics

DIE DIMENSIONS:
51 x 84 x 14 ±1mils

METALLIZATION:
Type: Al
Thickness: 17.5kÅ ±2.5kÅ

PASSIVATION:
Type: SiO_2
Thickness: 13kÅ ±2.6kÅ

SUBSTRATE POTENTIAL (POWERED UP):
V-

WORST CASE CURRENT DENSITY:
$9.18 \times 10^4 A/cm^2$ at 70mA

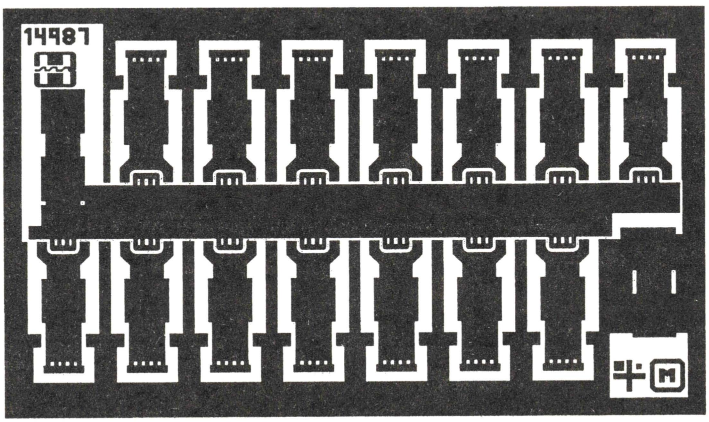
PROCESS:
Bipolar

Metallization Mask Layout

SP720MD-8, SP720MD, SP720MM-8, SP720MM

V_{CC} (16)

9

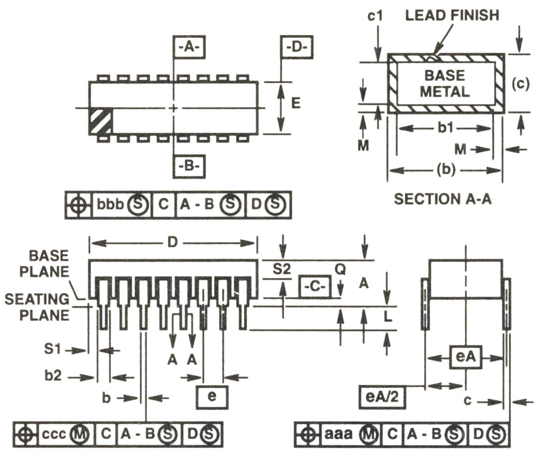


1

GND (8)

(SBDIP PINOUT)

Ceramic Dual-In-Line Metal Seal Packages (SBDIP)



D16.3 MIL-STD-1835 CDIP2-T16 (D-2, CONFIGURATION C)
16 LEAD CERAMIC DUAL-IN-LINE METAL SEAL PACKAGE

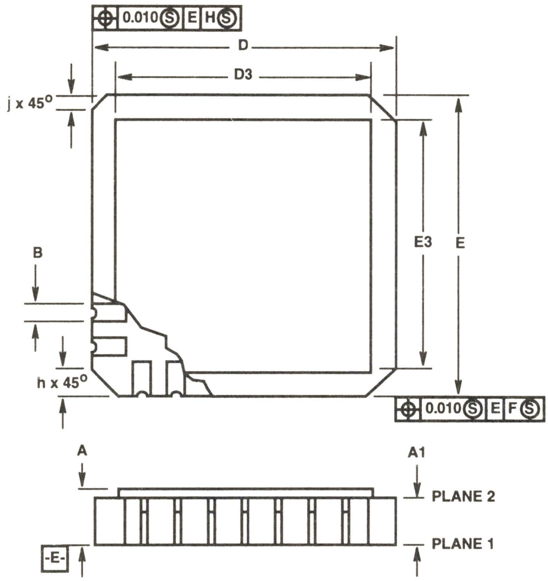
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.840	-	21.34	-
E	0.220	0.310	5.59	7.87	-
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	5
S1	0.005	-	0.13	-	6
S2	0.005	-	0.13	-	7
α	90^{o}	105^{o}	90^{o}	105^{o}	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2
N	16		16		8

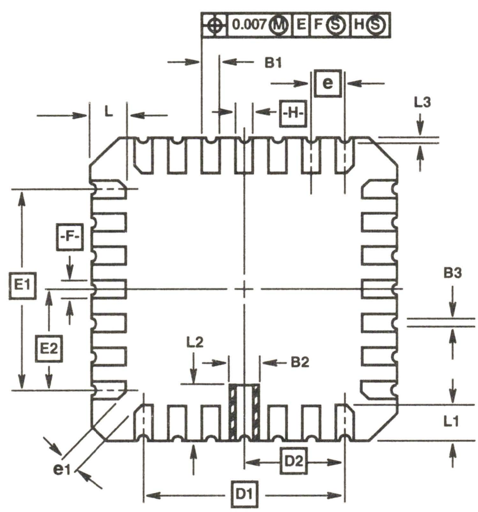
Rev. 0 4/94

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. Dimension Q shall be measured from the seating plane to the base plane.
6. Measure dimension S1 at all four corners.
7. Measure dimension S2 from the top of the ceramic body to the nearest metallization or lead.
8. N is the maximum number of terminal positions.
9. Braze fillets shall be concave.
10. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
11. Controlling dimension: INCH.

Ceramic Leadless Chip Carrier Packages (CLCC)





J20.A MIL-STD-1835 CQCC1-N20 (C-2)
20 PAD CERAMIC LEADLESS CHIP CARRIER PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.060	0.100	1.52	2.54	6, 7
A1	0.050	0.088	1.27	2.23	-
B	-	-	-	-	-
B1	0.022	0.028	0.56	0.71	2, 4
B2	0.072 REF		1.83 REF		-
B3	0.006	0.022	0.15	0.56	-
D	0.342	0.358	8.69	9.09	-
D1	0.200 BSC		5.08 BSC		-
D2	0.100 BSC		2.54 BSC		-
D3	-	0.358	-	9.09	2
E	0.342	0.358	8.69	9.09	-
E1	0.200 BSC		5.08 BSC		-
E2	0.100 BSC		2.54 BSC		-
E3	-	0.358	-	9.09	2
e	0.050 BSC		1.27 BSC		-
e1	0.015	-	0.38	-	2
h	0.040 REF		1.02 REF		5
j	0.020 REF		0.51 REF		5
L	0.045	0.055	1.14	1.40	-
L1	0.045	0.055	1.14	1.40	-
L2	0.075	0.095	1.91	2.41	-
L3	0.003	0.015	0.08	0.38	-
ND	5		5		3
NE	5		5		3
N	20		20		3

Rev. 0 5/18/94

NOTES:

1. Metallized castellations shall be connected to plane 1 terminals and extend toward plane 2 across at least two layers of ceramic or completely across all of the ceramic layers to make electrical connection with the optional plane 2 terminals.
2. Unless otherwise specified, a minimum clearance of 0.015 inch (0.38mm) shall be maintained between all metallized features (e.g., lid, castellations, terminals, thermal pads, etc.)
3. Symbol "N" is the maximum number of terminals. Symbols "ND" and "NE" are the number of terminals along the sides of length "D" and "E", respectively.
4. The required plane 1 terminals and optional plane 2 terminals (if used) shall be electrically connected.
5. The corner shape (square, notch, radius, etc.) may vary at the manufacturer's option, from that shown on the drawing.
6. Chip carriers shall be constructed of a minimum of two ceramic layers.
7. Dimension "A" controls the overall package thickness. The maximum "A" dimension is package height before being solder dipped.
8. Dimensioning and tolerancing per ANSI Y14.5M-1982.
9. Controlling dimension: INCH.

TVS 11

APPLICATION NOTES

Application Notes (Continued)

Recommendations for Soldering Terminal Leads to MOV Varistor Discs

Introduction

The CA and NA series of MOV varistor discs with silver electrodes are specifically designed for custom assembly and packaging. To take advantage of the excellent performance and reliability of Harris varistor technology, it is important that the correct materials and processes be used when soldering terminal leads to the disc.

Solder Fixtures

Where varistor discs are custom assembled and packaged, fixturing is normally employed to maintain disc and terminal alignment during solder reflow. Soldering fixtures should be of lightweight design to reduce their thermal mass and, hence, the time necessary to bring them to reflow temperature.

Disc and terminal lead should be pressed together lightly during the whole soldering process to help expel flux residues and excess solder from the interface. Trapped flux residue can result in bubbling of the solder, which leaves voids between silver electrode and terminal. Excess solder will enhance the tendency of the silver electrode to leach.

Soldering Ovens

Box, convection, and conveyor belt ovens are suitable for reflow solder processes using fixtures.

Box ovens should have forced air circulation with sufficient ventilation to remove flux vapors. It is important that every fixture position in the oven be subjected to the same heating conditions. Therefore, fixture positions should be limited to locations within the oven where uniform air flow and temperature can be maintained.

Convection ovens employ carefully designed exit baffles to facilitate close control of the soldering environment. Air is the best environment for soldering varistors. An inert gas (nitrogen) or reducing atmosphere is sometimes employed to reduce oxidation in these ovens, but neither of these is recommended for the processing of unpassivated varistors.

A very repeatable temperature profile can be achieved with a conveyor belt oven. The profile is determined by the temperature of the heated zone(s) and the speed of the belt. A fixed loading pattern also helps in achieving uniform results.

Fluxes

Fluxes are used for chemical cleaning of disc and terminal surfaces. There are three basic types:

R - These unactivated fluxes are less effective than the others in reducing oxides of copper, nickel, or palladium/silver metallizations, but are the ones recommended for MOV varistors. All other fluxes increase leakage, reduce long term reliability, and can promote leaching of the silver electrode. Non-charring, non-activated R type fluxes such as Alpha 100 or its equivalent are best.

RMA - These are mildly activated fluxes, and the most commonly used in the mounting of electronic components. They may be used with varistors, but are not recommended.

RA - These fully activated fluxes are corrosive, difficult to remove, and can lead to varistor failure. They must not be used to flux varistor discs.

Solders and Solder Temperature

Solders in the form of pastes or preforms can be used with varistors. Preforms are solder shapes premanufactured to specific sizes. Upon melting, they provide highly reproducible volumes of solder for joining. Preforms can be prefluxed, eliminating the need for any additional fluxing.

Heat should not be applied to a varistor too quickly, as the flux will not have sufficient time to activate and clean the joining surfaces. The result will be poor solderability. On the other hand, no varistor should be held longer than necessary at an elevated temperature. If heat is applied too slowly or maintained above reflow temperature for too long, leaching of the silver electrode into the solder will occur, reducing the disc to terminal bond strength. To avoid leaching, only solders with at least 2% silver content (e.g., 62Sn/36Pb/2Ag or equivalent) should be used; see Table 1.

It is equally important to observe processing time and temperature limits. Failure to do so can result in excessive leakage and alterations of the varistor's VI characteristic.

Cleaning and Cleaning Fluids

Cleaning is an important step in the soldering process. It prevents electrical faults such as the high current leakage caused by ionic contamination, absorbed organic material, dirt films, and resins.

A wide variety of cleaning processes can be applied to varistors, including water based, solvent based or a mixture of both, tailored to specific applications. Harris recommends 1.1.1 trichloroethane for the removal of flux residues after soldering.

Defluxing in a solvent bath with ultrasonic agitation, followed by a solvent vapor wash, is a very effective cleaning process. After cleaning, the low boiling point solvent completely evaporates from the disc, and will not harm solder joints.

TABLE 1. SILVER BEARING SOLDERS (ALPHA METALS)

ALLOY	MELTING TEMPERATURE
62Sn/36Pb/2AG	179°C
96.5Sn/3.5Ag	221°C
96Sn/5 Ag	221°C - 245°C
10Sn/88Pb/2Ag	268°C - 302°C
5Sn/92.5Pb/2.5Ag	280°C
97.5Pb/2.5Ag	305°C

No. AN9108.3 January 1998

Harris Suppression Products

Harris "ML" Multilayer Surface Mount Surge Suppressors

Harris produces three families of multilayer suppressors: the ML, MLE, and AUML. While much of the information presented here is generic to all three, this note focuses on the ML version.

Introduction

Sensitivity of Components

Modern electronic circuits can be vulnerable to damage from voltage transient overstresses. The progress in the development of faster ICs with higher levels of integration can be accompanied by an increase in vulnerability. Figure 1 shows relative damage susceptibility of some commonly used components, including discrete semiconductors and integrated circuits [1, 2].

The voltage, current, or power seen by a device must be below the failure threshold of the device. The magnitude of any voltage transient is determined by the nature of the source, the characteristic impedance of the circuit and the resistance and inductance between the source of the transient and the device.

The Transient Threat

Transients exist in every AC or DC system, or any wire connecting two pieces of equipment or components. The sources of the transient can be lightning, nuclear electromagnetic pulse, high energy switching and high voltage sparkover, or electrostatic discharge. These transients may be found wherever the energy stored in inductances, capacitors, or mechanical devices, such as motors and generators, is returned to a circuit. Stray capacitance and inductance may also set off oscillations, making the problem even worse.

While a direct hit from lightning is not of real concern for a printed circuit board user, what may be of concern is the level of the transient which is "let through" by the primary suppressor. This "follow on current" may be up to 50A and it will last for a number of microseconds. If this current is above the failure threshold of a device in the circuit, it will be destroyed.

The two most likely types of transients from which a circuit must be protected are electrostatic discharge (ESD), and the switching of reactive loads. ESD will result when two

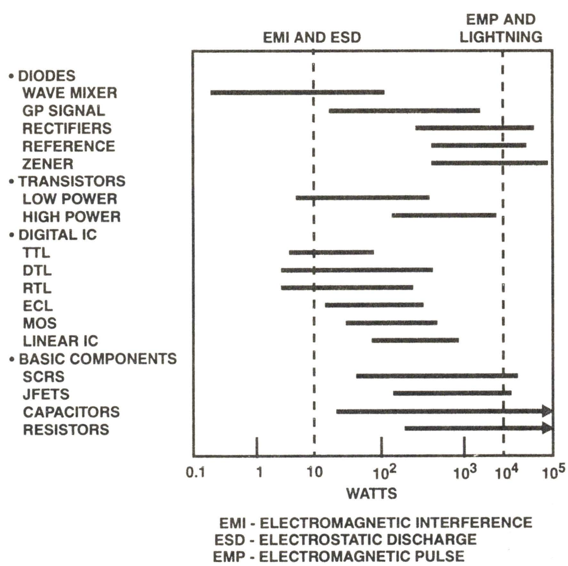


FIGURE 1. RELATIVE DAMAGE SUSCEPTIBILITY OF ELECTRONIC COMPONENTS (FOR 1μs PULSE)

conducting materials are brought close to one another and a voltage discharge occurs. The resulting voltage discharge can be as high as 25kV and will last up to 50ns. Transients can also be generated when an inductive load is disconnected and the existing energy is discharged back into the circuit. The arc generated from the opening of mechanical relay switches is another common source of switching transients.

Whatever the cause of the transient, natural or man-made, the damage potential is real and cannot be casually dismissed if reliable operation of equipment is to be expected. To properly select a transient suppressor, the frequency of occurrence of transients, the open-circuit voltage, the short circuit-current, and the source impedance of the circuit must be known.

Multilayer Surge Suppressor Description

The Harris multilayer (ML) series of transient voltage surge suppressors represents a breakthrough in the area of semiconducting ceramic processing. The ML suppressor is a compact, surface mountable chip that is voltage dependent, non-linear, and bi-directional. It has an electrical behavior similar to that of a back-to-back diode, i.e. it is inherently fully symmetrical, offering protection in both forward and reverse directions. The sharp, symmetrical breakdown characteristics of the device provides excellent protection from damaging voltage transients (Figure 2). When exposed to high voltage transients, the ML impedance changes many orders of magnitude from a near open circuit to a highly conductive state.

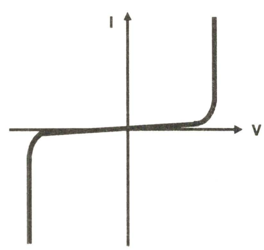


FIGURE 2. SHARP SYMMETRICAL BREAKDOWN OF MULTILAYER SUPPRESSOR

Construction

The ML is constructed by forming a combination of alternating electrode plates and semiconducting ceramic layers into a block. Each alternate layer of electrode is connected to opposite end terminations (Figure 3). The interdigitated block formation greatly enhances the available cross-sectional area for active conduction of transients. This paralleled arrangement of the inner electrode layers represents significantly more active surface area than the small outline of the package may suggest. This increased active surface area results in proportionally higher peak energy capability.

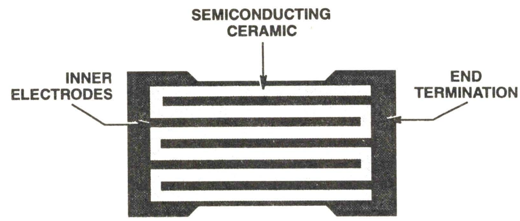


FIGURE 3. MULTILAYER INNER ELECTRODES & SEMICONDUCTING CERAMIC (CROSS-SECTION)

Another advantage of this type of construction is that the breakdown voltage of the device is dependent on the dielectric thickness between the electrode layers and not the overall thickness of the device. Increasing or decreasing the dielectric thickness will change the breakdown voltage of the device.

Energy handling capability can be significantly increased with a larger overall package outline. The energy handling capability doubles from 0.6J (10/1000μs waveform) for a 0.120 inch by 0.06 ("1206") inch device to 1.2J for a 0.120 inch by 0.100 ("1210") inch device.

The crystalline structure of the ML transient voltage suppressor (TVS) consists of a matrix of fine, conductive grains separated by uniform grain boundaries, forming many P-N junctions (Figure 4). These boundaries are responsible for blocking conduction at low voltages, and are the source of the nonlinear electrical conduction at higher voltages. Conduction of the transient energy takes place between these P-N junctions. The uniform crystalline grains act as heat sinks for the energy absorbed by the device in a transient condition, and ensures an even distribution of the transient energy (heat) throughout the device. This even distribution results in enhanced transient energy capability and long term reliability.

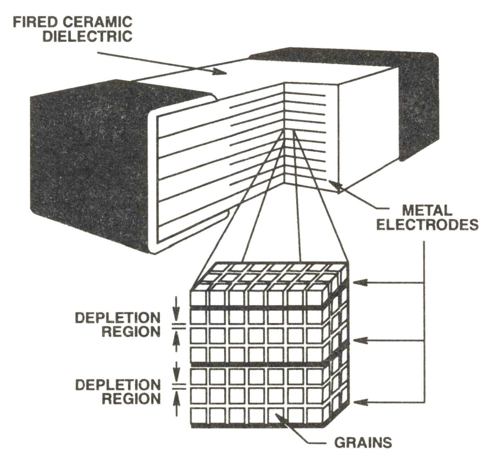


FIGURE 4. MULTILAYER TRANSIENT VOLTAGE SUPPRESSOR

Package Outline

The ML surge suppressor is a leadless chip device that is much smaller in size than the components it is designed to protect. The present size offerings are "0603", "0805", "1206", "1210", "1812" and "2220" EIA chip sizes. See the Harris ML, MLE and AUML data sheets for detailed device information and size offering. Since the device is inherently bi-directional, symmetrical orientation for placement on a printed circuit board is not a concern. Its robust construction makes it ideally suitable to endure the thermal stresses encountered in the soldering, assembling and manufacturing steps involved in surface mount applications. As the device is inherently passivated by the fired ceramic material, it will not support combustion and is thus immune to any risk of flammability which may be present in the plastic or epoxy molded parts used in industry standard packages.

Characteristics

Speed of Response

The clamping action of the ML suppressor depends on a conduction mechanism similar to that of other semiconductor devices. The response time of the zinc oxide material itself has been shown to be less than 500ps [3, 4, 5]. The apparent slow response time often associated with zinc oxide is due to parasitic inductance in the package and leads. Thus, the single most critical element affecting the response time of any suppressor is its lead length and, hence, the inductance in the leads. As the ML suppressor is a true surface mount device, with no leads or external packaging, it has virtually zero inductance. In actual applications, the estimation of voltage overshoot is of more practical relevance than that of speed of response. As a multilayer suppressor has essentially zero inductance it has little or no voltage overshoot. The actual response time of a ML surge suppressor is 1ns to 5ns. This response time is more than sufficient for the transients which are likely to be encountered by a component on a printed circuit board.

Clamping Voltage

The clamping voltage of a suppressor is the peak voltage appearing across the device when measured under the conditions of a specified pulse current and specified waveform. The industry recommended waveform for clamping voltage is the 8/20μs pulse which has been endorsed by UL, IEEE and ANSI. The clamping voltage of the ML should be the level at which a transient must be suppressed to ensure that system or component failure does no occur. Shunt-type suppressors like the ML are used in parallel to the systems they protect. The effectiveness of shunt suppressors can be increased by understanding the important influence that source and line impedance play in a system, such as is shown in Figure 5.

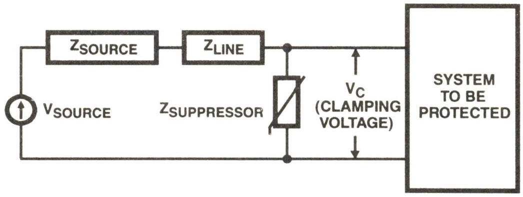


FIGURE 5. VOLTAGE DIVISION BETWEEN SOURCE, LINE AND SUPPRESSOR IMPEDANCE

To obtain the lowest clamping voltage (V_C) possible, it is desirable to use the lowest suppressor impedance ($Z_{SUPPRESSOR}$) and the highest line impedance (Z_{LINE}). The suppressor impedance is an inherent feature of the device, but the line impedance can become an important factor, by selecting location of the suppressor, or by adding resistances or inductances in series.

$$V_C = \frac{V_{SUPPRESSOR} \times V_{SOURCE}}{Z_{SUPPRESSOR} + Z_{LINE} + Z_{SOURCE}}$$

Temperature Dependence

In the off state, the V-I characteristics of the ML suppressor approaches a linear (ohmic) relationship and shows a temperature dependent affect (Figure 6). The suppressor is in a high resistance mode (approaching $10^6\Omega$) and appears as a near open circuit. This is equivalent to the leakage region in a traditional zener diode. Leakage currents at maximum rated voltage are in the microamp range. When clamping transients at higher currents (at and above the milliamp range), the ML suppressor approaches a near short circuit. Here the temperature variation in the characteristics of the ML becomes minimal throughout the full peak current and energy range (Figure 7). The clamping voltage of a multilayer transient voltage suppressor is the same at 25°C and at 125°C.

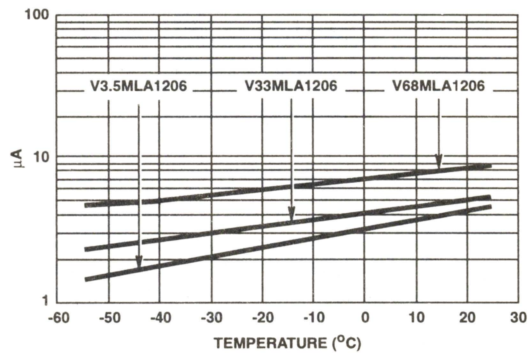


FIGURE 6. TEMPERATURE DEPENDENCE AT LOWER VOLTAGE

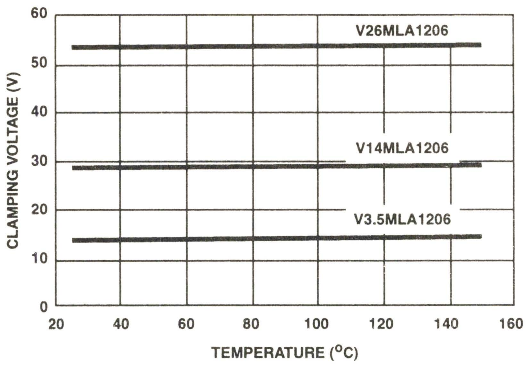


FIGURE 7. CLAMPING VOLTAGE VARIATION OVER TEMPERATURE

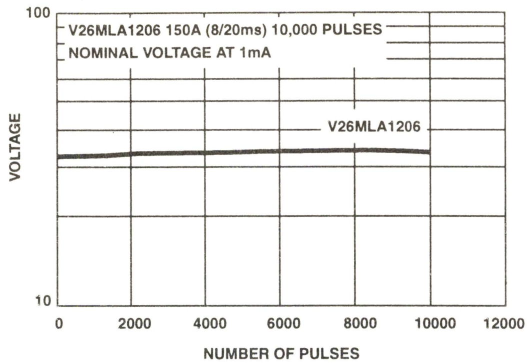


FIGURE 9. REPETITIVE PEAK PULSE CAPABILITY

Peak Current Capability

The peak current handling capability, and hence its ability to dissipate transient energy, is one of the ML suppressor's best features. This is achieved by the interdigitated construction of the ML, which ensures that a large volume of suppressor material is available to absorb the transient energy. This structure ensures that the peak temperatures generated by the transient is kept low, because all of the package is available to absorb all the energy.

(Figure 8). Because of the low peak temperatures, the ML will experience very low thermal stress, both during heating and cooling.

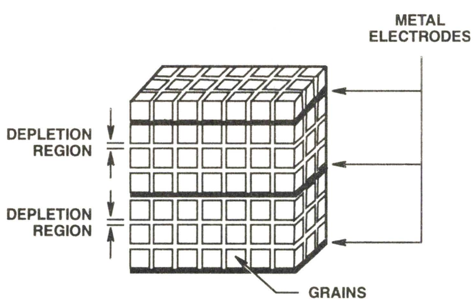


FIGURE 8. INTERDIGITATED CONSTRUCTION

Repetitive pulsing on the ML suppressors (Figure 9) show negligible shift in the nominal voltage at one milliamp (less than 3%). There was also a minimal change in the leakage current of these devices. The Harris ML suppressor can also operate up to 125°C without any need for derating.

Capacitance

The ML suppressor is constructed by building up a composite assembly of alternate layers of ceramic material and metal electrode. Since capacitance is proportional to area, and inversely proportional to thickness, the lower voltage ML's have a higher capacitance. See the Harris data sheets for specific values which range from less than 100 to 6000 picofarads. Typical values of capacitance vs frequency are shown in Table 1 (for two types).

TABLE 1. TYPICAL CAPACITANCE VALUES vs FREQUENCY

CAPACITANCE (pF)				
	FREQUENCY (AT BIAS = $1V_{P-P}$)			
DEVICE TYPE	1kHz	10kHz	100kHz	1MHz
V5.5MLA1206	6250	5680	5350	5000
V68MLA1206	190	170	160	150

Size

A principal benefit of the new ML suppressor is their compact size in comparison to other surface mount components. Additionally, the solder mounting pads required for ML are much smaller, resulting in even more circuit board area savings.

As stated, the present offering of multilayer suppressor size ranges from 0603 to 2220, depending upon the series type.

Surface mounted surge suppressors include leaded gull-wing and j-bend zener diodes or a relatively large surface mount metal oxide varistor. In such cases a large area of the PC board is needed for mounting. Electrically equivalent ML suppressors are much smaller, resulting in significant surface mount PC board area savings (Figure 10). Additional board area savings are realized with the smaller solder mounting area required by the ML as compared to the gull-wing or j-bend packages (Figure 11).

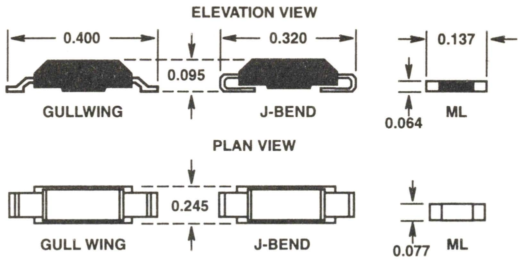
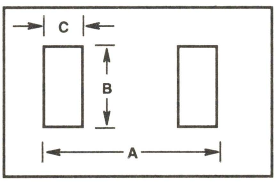


FIGURE 10. COMPARATIVE SURFACE MOUNT SURGE SUPPRESSORS



	DIMENSIONS		
	A	B	C
ML1206	0.203	0.103	0.065
Gull Wing	0.410	0.125	0.050
J-Bend	0.330	0.125	0.070

FIGURE 11. SOLDERING LAND PAD REQUIREMENTS

Applications

Protection of Integrated Circuits and Low Voltage Circuits

Protection against the coupling of transients are mainly required at two locations on the printed circuit board. The first is at the input/output port which affords protection of sensitive inputs to line drivers and receivers. The second location is at the power input to the integrated circuits at the input side of the board. This location will serve to keep the transient threat from transmitting throughout the rest of the board.

In the past, IC's have been protected by means of decoupling capacitors across the input power supply lines. The capacitors suppressed transients and supplied peak current for high speed switching operations. Unfortunately, the energy stored in the capacitor, and with it it's suppression capability, is very small: $E = 1/2 * C * V^2$.

Large electrolytic capacitors are usually placed on the output of the 5V supply. These capacitors are bulky and somewhat ineffective because of their poor high frequency response. Crowbars are also used to sense overvoltages. The crowbar functions such that an overvoltage shorts the output until the input fuse or circuit breaker opens, thereby turning the system off. Other concerns to consider as well as the power supplies and supply circuitry, are the input and output terminals carrying information. As long as the interconnections are short, transients do not seem to be a problem. However, when connections from board-to-board, system-to-system, or system-to-sensor are considered transients must be controlled (see Figure 12). [7]

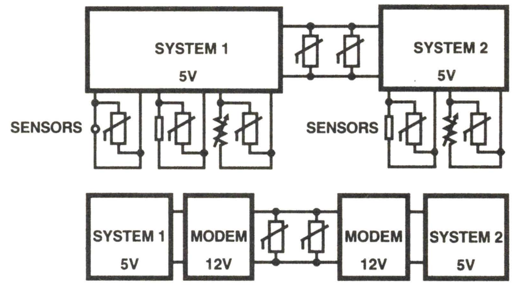


FIGURE 12. SYSTEM-TO-SYSTEM AND SYSTEM-TO-SENSOR PROTECTION

If the distances become long or interconnections between systems result in transient pick-up, then transient suppression is a pre-requisite. Devices that are more effective than resistors and capacitors are needed to provide the necessary protection. Small spark gaps and silicon suppressors have been used quite effectively, but spark gaps still need a zener diode to reduce the initial voltage rise that triggers the spark gaps.

Silicon suppressors, with their almost ideal V-I characteristics, are used quite extensively. However, zeners have low current-surge capabilities and are of limited value as a transient suppressor when a relatively high magnitude transient is encountered. Surge capability is low because the thermal mass of the silicon chip, where all the energy of the transients is to be converted into heat, is so small. Peak temperatures can become so high that part of the silicon will melt, and the device will fail. On the other hand, there are zener diodes specifically designed for transient suppression. The thermal mass of these devices is increased by attaching more copper to the silicon pellet. This approach helps, but it does not eliminate the basic problem. The transient energy is still converted into heat in the silicon pellet. The heat travels somewhat faster to the surrounding mass of copper. However, the large temperature differentials still exist. The mismatch of the thermal coefficient of expansion between the silicon and copper will create shearing forces that may lead to failures due to thermal fatigue.

The low voltage V5.5MLA1206 may be used to protect integrated circuits requiring 5V on the input, e.g. all integ- rated circuits, systems containing low voltage IC's, memories, test equipment, data processing equipment, etc. The suppressor should be connected upstream from the IC to be protected. The maximum clamping voltage of the suppressor depends on the maximum transient current. If the clamping voltage is too high and the signal currents are low, a hybrid arrangement of a multilayer suppressor and a series impedance (an inductor or resistor) may be an effective and low cost solution. The series impedance should be as large as possible without

distorting or attenuating the signal appreciably. The clamping voltage of the suppressor should be low, but high enough to prevent attenuation or distortion of the signal.

CMOS Protection

Latch-up is a phenomenon inherent in the basic CMOS structure. It is initiated by external conditions, is present only momentarily, and once induced is difficult to reverse, except by complete removal of power to the chip. Latch-up results in large current flow from V_{CC} to ground. It can be triggered by an increasing voltage across the power terminal, such as an excessive voltage at the V_{CC} pin (normally well above the maximum V_{CC} rating of the device). This can be prevented by connecting a low voltage ML transient suppressor across V_{CC}.

Unfortunately, even if the systems power supply variations are kept small, individual inputs can still vary widely. Latch-up is also known to occur in CMOS systems when voltage supplied to an input exceeds the supply voltage. Again, transients can be the culprit; the wrong sequence in power-up or power-down may have the same effect. A ML suppressor connected from V_{CC} to ground will eliminate most of the latch-up problems caused by input over voltage. Additionally an ML suppressor connected from input to ground will help to protect the input from damaging transients such as electrostatic discharge (Figure 13).

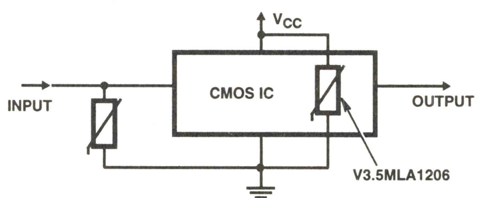


FIGURE 13. PROTECTION OF CMOS DEVICES

Here, the Harris V3.5MLA1206 for example, represents a method of protecting 3.5V CMOS logic.

Discrete MOSFET Protection

There has been an increasing migration from bipolar technology to MOSFET technology. A MOSFET gate could be more susceptible to damage from electrostatic discharges than a bipolar transistor. Also, the consequence of fast MOSFET switching time can be a "ringing" from wiring inductances. This could result in the MOSFET and adjacent components being subjected to short duration transient voltages. MLs can clamp these transients to a safe level.

It is important when using a ML suppressor to connect it as close as possible to the drain and source leads of the MOSFET, in order to minimize the loop inductance. As the ML suppressor is a true surface mount package and has no lead inductance, this ensures that the MOSFET does not suffer the additional transient voltage overshoot associated with leaded suppressors.

To protect the output of the MOSFET, the ML suppressor is connected between the drain and source (Figure 14). This ML must have a steady state voltage capability ($V_{M(DC)}$) which exceeds the worst case possible maximum supply voltage. Its clamping voltage at a peak transient current must be less than the minimum breakdown voltage of the MOSFET. For example, to protect against transients on a 28V ±10% supply, the V33MLA1206 ML suppressor with $V_{M(DC)}$ of 33V can be used. According to the transient V-I curves of the ML data sheet, this will protect a MOSFET with a 60V minimum breakdown from an approximate 10A transient pulse.

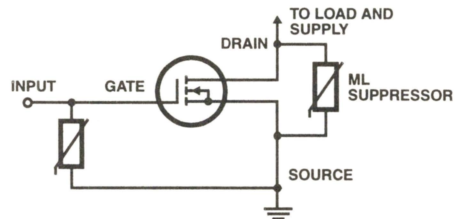


FIGURE 14. DISCRETE MOSFET PROTECTION

Additionally an ML suppressor can be used to protect the input of a discrete MOSFET from the threat of an ESD transient. In the protection of a MOSFET driven with a 10V gate drive, the V14MLA1206 or V14MLA1210 suppressor should be connected from gate to source. These devices will protect against ESD pulses of 2kV to 25kV.

The ML can also be used to protect MOSFETs (and bipolar transistors) from the transients generated when switching inductive loads. In this case, the ML selected must be able to dissipate the energy generated by the repetitive nature of these inductive load transient pulses (the average power of these transients must not exceed 0.25W).

Automotive System Protection

The increased use of surface mount technology in the automotive industry has resulted in the need for smaller, more densely packed boards with devices which have the performance capabilities of traditional through hole components.

The transient conditions which may occur in the automobile is one of the best documented, and best understood transient environments. A load dump transient will develop when an alternator charging a flat battery is suddenly removed from the system. Peak voltages up to 125V may develop and can last for 200ms-400ms. Another common transient phenomena is a jump start which is generated when using a 24V truck battery to start a car. This overvoltage may be applied for up to 3 to 5 minutes. Other transients result from relays and solenoids switching on and off, and from fuses blowing.

Table 3 shows some sources, amplitudes, polarity, and energy levels of generated transients in the automotive electrical system [8].

TABLE 3. TYPICAL AUTOMOTIVE SUPPLY TRANSIENT SUMMARY

LENGTH OF TRANSIENT	CAUSE	ENERGY CAPABILITY / VOLTAGE AMPLITUDE	FREQUENCY OF OCCURRENCE
Steady State	Failed Voltage Regulator	∞ +18V	Infrequent
3-5 Minutes	Jump Starts with 24V Battery	∞ ±24V	Infrequent
200ms to 400ms	Load Dump; Disconnection to Battery While at High Charging	>10J <125V	Infrequent
<320ms	Inductive-Load Switching Transient	<1J -300V to +80V	Often
200ms	Alternator Field Decay	< 1J -100V to -40V	Each Turn-Off
90ms	Ignition Pulse, Battery Disconnected	<0.5J <75V	<500Hz Several Times in Vehicle Life
1ms	Mutual Coupling in Harness	<1J <200V	Often
15µs	Ignition Pulse, Normal	<0.001J 3V	<500Hz Continuous
	Accessory Noise	<1.5V	50Hz to 10kHz
	Transceiver Feedback	≅20mV	R.F.
50ns	ESD	<10mJ 15kV	Infrequent

Extension of Contact Life

When relays or mechanical switches are used to control inductive loads, it is often necessary to derate the contacts to 50% of their resistive load rating due to the wear caused by the arcing of the contents. This arcing is caused by the stored energy in the inductive load. Each time the current in the inductive coil is interrupted by the mechanical contacts, the voltage across the contacts increases until the contacts arc. When the contacts arc, the voltage across the arc decreases and the current in the coil can increase somewhat. The extinguishing of the arc causes an additional voltage transient which can again cause the contacts to arc. It is not unusual for restriking to occur several times with the total energy in the arc several times that which was originally stored in the inductive load. It is this repetitive arcing that is so destructive to the contacts. An ML can be used to prevent initiation of the arc.

Knowing the energy absorbed per pulse, the pulse repetition rate and the maximum operating voltage is sufficient to select the correct size ML suppressor. It is necessary to ensure that the device selected is capable of dissipating the power generated in the coil [9].

The part number of the ML device gives the following basic information:

Description of ML Ratings and Characteristics

Maximum Continuous DC Working Voltage ($V_{M(DC)}$): This is the maximum continuous dc voltage which may be applied up to the maximum operating temperature (125°C) of the ML. This voltage is also used as the reference test point for leakage current. This voltage is always less than the breakdown voltage of the device.

Maximum Continuous AC RMS Working Voltage ($V_{M(AC)}$): This is the maximum continuous sinusoidal rms voltage which may be applied. This voltage may be applied at any temperature up to 125°C.

Maximum Non-Repetitive Surge Current (I_{TM}): This is the maximum peak current which may be applied for an 8/20µs impulse (Figure 15), with the $V_{M(DC)}$ or $V_{M(AC)}$ voltage also applied, without causing device failure. This pulse can be applied to the ML suppressor in either polarity.

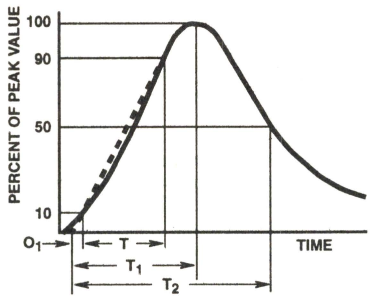
Maximum Non-Repetitive Surge Energy (W_{TM}): This is the maximum rated transient energy which may be dissipated for a single current pulse of 10/1000µs, with the rated $V_{M(DC)}$ or $V_{M(AC)}$ voltage applied, without causing device failure.

Maximum Clamping Voltage (V_C): This is the peak voltage appearing across the ML suppressor when measured for an 8/20µs impulse and specified pulse current. The clamping voltage is shown for a current range of 1mA to 50A in the maximum transient V-I characteristic curves.

Leakage Current (I_L): This is the amount of current drawn by the ML in its non-operational mode, i.e., when the voltage applied across the ML does not exceed the rated $V_{M(DC)}$ or $V_{M(AC)}$ voltage.

Nominal Voltage ($V_{N(DC)}$): This is the voltage at which the ML begins to enter its conduction state and suppress transients. This is the voltage defined at the 1mA point and has a minimum and maximum voltage specified.

Capacitance (C): This is the capacitance of the ML when measured at a frequency of 1MHz with $1V_{P-P}$ voltage bias applied.



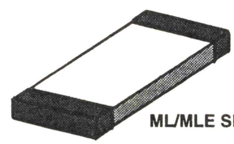
O_1 = Virtual Origin of Wave
T = Time From 10% to 90% of Peak
T_1 = Virtual Front time = 1.25 • t
T_2 = Virtual Time to Half Value (Impulse Duration)

Example: For an 8/20µs Current Waveform:
8µs = T_1 = Virtual Front Time
20µs = T_2 = Virtual Time to Half Value

FIGURE 15. CURRENT TEST WAVEFORM

Part Number Nomenclature VXXML Suppression Types

V 18 ML X 1206 X X X



ML/MLE SERIES

DEVICE FAMILY
Harris TVSS Device

MAXIMUM DC WORKING VOLTAGE

MULTILAYER DESIGNATOR

PERFORMANCE DESIGNATOR
A: STD
E: ESD

DEVICE SIZE:
i.e., 120 mil x 60 mil

CAPACITANCE OPTION
No Letter: Standard
L: Low Capacitance Version

END TERMINATION OPTION
No Letter: Ag/Pt (Standard)
W: Ag/Pd
N: Ni/Sn

PACKING OPTIONS
A: <100 pc Bulk Pak
H: 7in (178mm) Diameter Reel (Note)
T: 13in (330mm) Diameter Reel (Note)

NOTE: Quantity per reel depends upon device size.

Soldering Recommendations

The principal techniques used for the soldering of components in surface mount technology are Infra Red (IR) Reflow, Vapour Phase Reflow, and Wave Soldering. When wave soldering, the ML suppressor is attached to the circuit board by means of an adhesive. The assembly is then placed on a conveyor and run through the soldering process to contact the wave. With IR and Vapour Phase Reflow, the device is placed in a solder paste on the substrate. As the solder paste is heated, it reflows and solders the unit to the board.

With the ML suppressor, the recommended solder is a 62/36/2 (Sn/Pb/Ag), 60/40 (Sn/Pb), or 63/37 (Sn/Pb). Harris also recommends an RMA solder flux.

Wave soldering is the most strenuous of the processes. To avoid the possibility of generating stresses due to thermal shock, a preheat stage in the soldering process is recommended, and the peak temperature of the solder process should be rigidly controlled.

When using a reflow process, care should be taken to ensure that the ML chip is not subjected to a thermal gradient steeper than 4 degrees per second; the ideal gradient being 2 degrees per second. During the soldering process, preheating to within 100 degrees of the solders peak temperature is essential to minimize thermal shock. Examples of the soldering conditions for the ML series of suppressors are given in the tables below.

Once the soldering process has been completed, it is still necessary to ensure that any further thermal shocks are avoided. One possible cause of thermal shock is hot printed circuit boards being removed from the solder process and subjected to cleaning solvents at room temperature. The boards must be allowed to gradually cool to less than 50°C before cleaning.

Termination Options

Harris offers three types of termination finish on the Multilayer product series:

1. Silver/Platinum (standard)
2. Silver/Palladium (optional)
3. Nickel/Tin (optional)

(The ordering information section describes how to designate them.)

The Nickel/Tin plated termination can provide certain solder process application benefits such as:

- A better match to Tin/Lead solders resulting in improved solder wetting and solder fillet height (typically 70% of component height).
- An enhanced resistance to solder leaching permits greater flexibility/latitude in the design and control of solder processes. (See the temperature-time graph below.)
- An alternative material when silver end terminations are restricted.

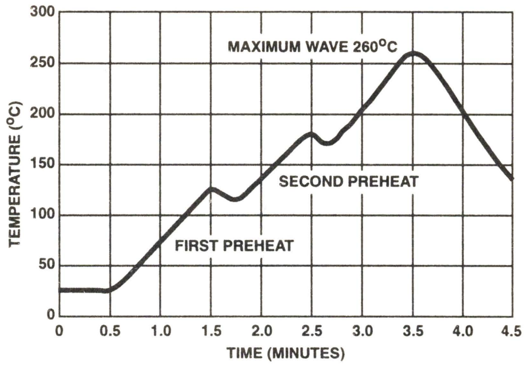


FIGURE 16. WAVE SOLDER PROFILE

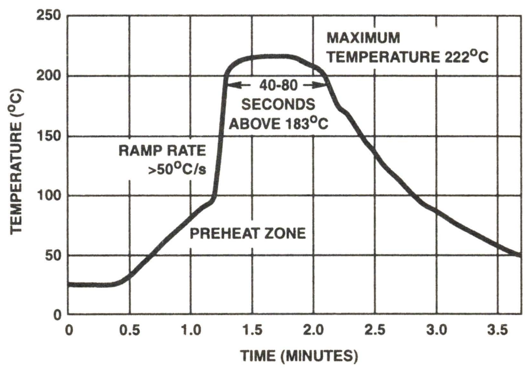


FIGURE 17. VAPOR PHASE SOLDER PROFILE

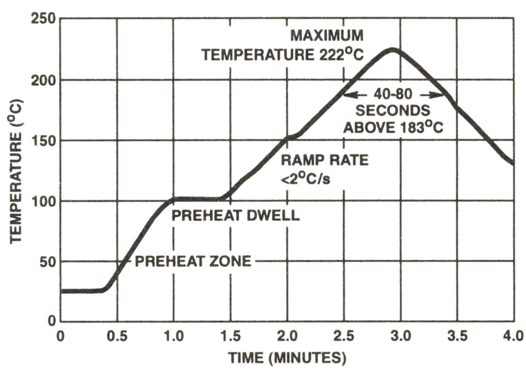


FIGURE 18. REFLOW SOLDER PROFILE

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http://www.semi.harris.com/
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No. AN9211.1 January 1998

Harris Suppression Products

Soldering Recommendations for Surface Mount Metal Oxide Varistors and Multilayer Transient Voltage Suppressors

Authors: Marty Corbett and Neil McLoughlin

Introduction

In recent years, electronic systems have migrated towards the manufacture of increased density circuits, with the same capability obtainable in a smaller package or increased capability in the same package. The accommodation of these higher density systems has been achieved by the use of surface mount technology (SMT). Surface mount technology has the advantages of lower costs, increased reliability and the reduction in the size and weight of components used. With these advantages, surface mount technology is fast becoming the norm in circuit design.

The increased circuit densities of modern electronic systems are much more vulnerable to damage from transient overvoltages than were the earlier circuits, which used relays and vacuum tubes. Thus, the progress in the development of faster and denser integrated circuits has been accompanied by an increase in system vulnerability. Transient protection of these sensitive circuits is highly desirable to assure system survival. Surface mount technology demands a reliable transient voltage protection technology, packaged compatibly with other forms of components used in surface mount technology.

Harris Semiconductor has led the field in the introduction of surface mount transient voltage suppressors. These devices encompass voltages from $3.5V_{DC}$ to $275V_{AC}$ and have a wide variety of applications. Their size, weight and inherent protection capability make them ideal for use on surface mount printed circuit boards.

There are two technologies of Harris surface mount surge suppressors. The CH Series metal oxide varistors which encompass voltages from $14V_{DC}$ to $275V_{AC}$ and the ML, MLE, and AUML Series Suppressors which cover a voltage range from $3.5V_{DC}$ to $120V_{DC}$.

Metal Oxide Varistors

A metal oxide varistor (MOV) is a non-linear device which has the property of maintaining are relatively small voltage change across its terminals while a disproportionately large surge current flows through it (Figure 1). When the MOV is connected in parallel across a line its non-linear action serves to divert the current of the surge and hold the voltage to a value that protects the equipment connected to the line. Since the voltage across the MOV is held at some level higher than the normal line voltage while surge current flows, there is energy deposited in the varistor during its surge diversion function.

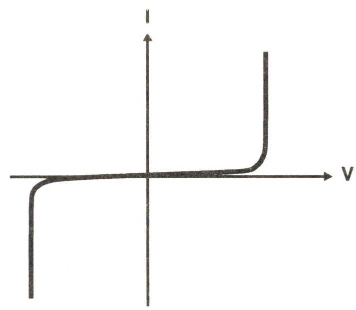


FIGURE 1. V-I CHARACTERISTICS OF A MOV

The basic conduction mechanism of a MOV results from semiconductor junctions (P-N junctions) at the boundaries of the zinc oxide grains. A MOV is a multi junction device with millions of grains acting as a series parallel combination between the electrical terminals. The voltage drop across a single grain in nearly constant and is independent of grain size.

The CH series of surface mount metal oxide varistors are of a monolayer construction in a 5mm by 8mm package size. They are fully symmetrical and are passivated both top and bottom (Figure 2). The main advantage of this technology is its high operating voltage capability ($68V_{DC}$ to $275V_{AC}$). The CH Series of metal oxide varistors are supplied in both 7" and 13" tape and reels.

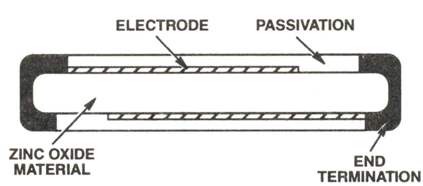


FIGURE 2. CROSS-SECTION OF THE "CH" SERIES OF METAL OXIDE VARISTORS

Multilayer Transient Voltage Suppressors

The Harris multilayer (ML) series of surface mount surge suppressors are of a multilayer construction. This technology, represents a recent breakthrough in its application to transient voltage suppression.

The ML, MLE, and AUML are constructed by forming a combination of alternating electrode plates and semiconducting ceramic layers into a block. Each alternate layer of electrode is connected to opposite end terminations (Figure 3). The interdigitated block formation greatly enhances the available cross-sectional area for active conduction of transients. This paralleled arrangement of the inner electrode layers represents significantly more active surface area than the small outline of the package may suggest. The increased active surface area results in proportionally higher peak energy capability.

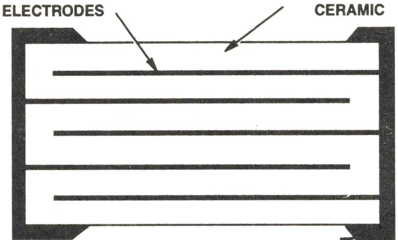


FIGURE 3. INTERNAL CONSTRUCTION OF THE HARRIS MULTILAYER TRANSIENT VOLTAGE SUPPRESSOR

A further advantage of this type of construction is that the breakdown voltage of the device is dependent on the thickness between the electrode layers (dielectric thickness) and not the overall thickness of the device.

These suppressors are often much smaller in size than the components they are designed to protect. The present size offerings are 0603, 0805, 1206, 1210, 1812 and 2220, with voltage ranges form $3.5V_{DC}$ to $120V_{DC}$. Its robust construction makes it ideally suitable to endure the thermal stresses involved in the soldering, assembling and manufacturing steps involved in surface mount technology. As the device is inherently passivated by the fired ceramic material, it will not support combustion and is thus immune to any risk of flammability which may be present in the plastic or epoxy molded parts used in industry standard packages.

Substrates

There are a wide choice of substrate materials available for use as printed circuit boards in a surface mount application. The main factors which determine the choice of material to use are:

1. Electrical Performance
2. Size and Weight Limitations
3. Thermal Characteristics
4. Mechanical Characteristics
5. Cost

When choosing a substrate material, the coefficient of thermal expansion of a Harris surface mountable suppressor of 6ppm/^{o}C is an important consideration. Non-organic materials (ceramic based substrates), like aluminum or berillia, which have coefficients of thermal expansion of 5-7ppm^{o}C, are a good match for the CH and ML series devices. Table 1 outlines some of the other materials used, and also their more important properties pertinent to surface mounting.

While the choice of substrate material should take note of the coefficient of expansion of the devices. This may not be the determining factor in whether a device can be used or not. Obviously the environment of the finished circuit board will determine what level of temperature cycling will occur. It is this which will dictate the criticality of the match between device and PCB. Currently for most applications, both the CH and ML series use FR4 boards without issue.

TABLE 1. SUBSTRATE MATERIAL PROPERTIES

SUBSTRATE STRUCTURE	MATERIAL PROPERTIES		
	GLASS TRANSITION TEMPERATURE (^{o}C)	XY COEFFICIENT OF THERMAL EXPANSION (ppm/^{o}C)	THERMAL CONDUCTIVITY (W/M^{o}C)
Epoxy Fiberglass-FR4	125	14-18	0.16
Polyamide Fiberglass	250	12-16	0.35
Epoxy Aramid Fiber	125	6-8	0.12
Fiber/Teflon Laminates	75	20	0.26
Aluminium-Beryillia (Ceramic)	Not Available	5-7	21.0

Fluxes

Fluxes are used for the chemical cleaning of the substrate surface. They will completely remove any surface oxides, and will prevent re-oxidation. They contain active ingredients such as solvents for removing soils and greases. Nonactivated fluxes ("R" type) are relatively effective in reducing oxides of copper, nickel or palladium/silver metallizations and are recommended for use with the Harris surface mount range.

Mildly activated fluxes ("RMA" type) have natural and synthetic resins, which reduce oxides to metal or soluble salts. These "RMA" fluxes are generally not conductive nor corrosive at room temperature and are the most commonly used in the mounting of electronic components.

The "RA" type (fully activated) fluxes are corrosive, difficult to remove, and can lead to circuit failures and other problems. Other non-resin fluxes depend on organic acids to reduce oxides. They are also corrosive after soldering and also can damage sensitive components. Water soluble types in particular must be thoroughly cleaned from the assembly.

Environmental concerns, and the associated legislation, has led to a growing interest in fluxes with residues that can be removed with water or water and detergents (semi-aqueous cleaning). Many RMA fluxes can be converted to water soluble forms by adding saponifiers. There are detergents and semi-aqueous cleaning apparatus available that effectively remove most RMA type fluxes. Semi-aqueous cleaning also tends to be less expensive than solvent cleaning in operations where large amounts of cleaning are needed.

For the Harris Semiconductor range of surface mount varistors, nonactivated "R" type fluxes such as Alpha 100 or equivalent are recommended.

Land Pad Patterns

Land pad size and patterns are one of the most important aspects of surface mounting. They influence thermal, humidity, power and vibration cycling test results. Minimal changes (even as small as 0.005 inches) in the land pad pattern have proven to make substantial differences in reliability.

This design/reliability relationship has been shown to exist for all types of designs such as in J lead, quadpacks, chip resistors, capacitors and small outline integrated circuit (SOIC) packages. Recommended land pad dimensions are provided for some surface mounted devices along with formulae which can be applied to different size varistors. Figure 4 gives recommended land patterns for the direct mount ML and CH series devices.

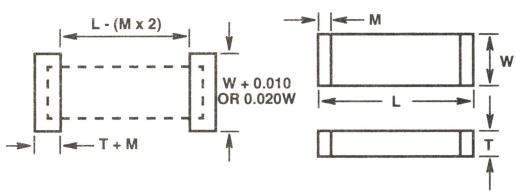


FIGURE 4. FORMULA FOR SURFACE MOUNTABLE VARISTOR FOOTPRINTS

TABLE 2. RECOMMENDED MOUNTING PAD OUTLINE

SUPPRESSOR FAMILY	DIMENSION		
	T + M	L-(M X 2)	0.020W (W + 0.010)
5 X 8 CH Series	2.21 (0.087)	5.79 (0.228)	5.50 (0.216)
0603 ML/MLE Series	1.12 (0.044)	0.56 (0.02)	1.62 (0.064)
0805 ML/MLE Series	1.48 (0.058)	0.69 (0.027)	2.13 (0.084)
1206 ML/MLE Series	1.65 (0.065)	1.85 (0.073)	2.62 (0.103)
1210 ML/AUML Series	1.85 (0.073)	1.85 (0.073)	3.73 (0.147)
1812 AUML Series	1.85 (0.073)	3.20 (0.126)	4.36 (0.172)
2220 AUML Series	1.84 (0.073)	4.29 (0.169)	6.19 (0.240)

Solder Materials and Soldering Temperatures

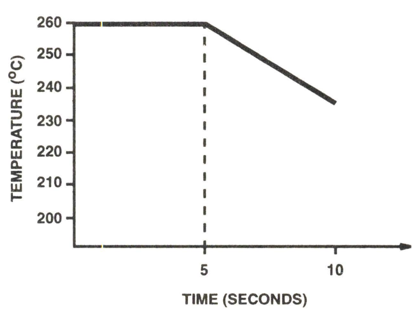


FIGURE 5. RECOMMENDED MAXIMUM TIME AND SOLDER TEMPERATURE RELATIONSHIP OF HARRIS MOVs

No varistor should be held longer than necessary at an elevated temperature. The termination materials used in both the CH and ML series devices are enhanced silver based materials. These materials are sensitive to exposure time and peak temperature conditions during the soldering process (Figure 5). The enhanced silver formulation contains either platinum, palladium or a mixture of both, which have the benefit of significantly reducing any leaching effects during soldering. To further ensure that there is no leeching of the silver electrode on the varistor, solders with at least 2% silver content are recommended (62 Sn / 36 Pb / 2 Ag). Examples of silver bearing solders and their associated melting temperatures are as follows:

TABLE 3. SILVER BEARING SOLDERS (ALPHA METALS)

ALLOY	MELTING TEMPERATURE	
	^{o}F	^{o}C
62 Sn / 36 Pb / 2 Ag	355	179
96.5 Sn / 3.5 Ag	430	221
95 Sn / 5 Ag	430-473	221-245
20 Sn / 88 Pb / 2 Ag	514-576	268-302
5 Sn / 92.5 Pb / 2.5 Ag	536	280

Soldering Methods

There are a number of different soldering techniques used in the surface mount process. The most common soldering processes are infrared reflow, vapor phase reflow and wave soldering.

With the Harris surface mount range, the solder paste recommended is a 62/36/2 silver solder. While this configuration is best, other silver solder pastes can also be used. In all soldering applications, the time at peak temperature should be kept to a minimum. Any temperature steps employed in the solder process must, in broad terms, not exceed 70°C to 80°C. In the preheat stage of the reflow process, care should be taken to ensure that the chip is not subjected to a thermal gradient of greater than 4 degrees per second; the ideal gradient being 2 degrees per second. For optimum soldering, preheating to within 100 degrees of the peak soldering temperature is recommended; with a short dwell at the preheat temperature to help minimize the possibility of thermal shock. The dwell time at this preheat temperature should be for a time greater than $10T^2$ seconds, where T is the chip thickness in millimeters. Once the soldering process has been completed, it is still necessary to protect against further effects of thermal shocks. One possible cause of thermal shock at the post solder stage is when the hot printed circuit boards are removed from the solder and immediately subjected to cleaning solvents at room temperature. To avoid this thermal shock affect, the boards must first be allowed to cool to less than 50°C prior to cleaning.

Two different resistance to solder heat tests are routinely performed by Harris Semiconductor to simulate any possible effects that the high temperatures of the solder processes may have on the surface mount chip. These tests consist of the complete immersion of the chip in to a solder bath at 260°C for 5 seconds and also in to a solder bath at 220°C for 10 seconds. These soldering conditions were chosen to replicate the peak temperatures expected in a typical wave soldering operation and a typical reflow operation.

Reflow Soldering

There are two major reflow soldering techniques used in SMT today:

1. InfraRed (IR) Reflow
2. Vapor Phase Reflow

The only difference between these two methods is the process of applying heat to melt the solder. In each of these methods precise amounts of solder paste are applied to the circuit board at points where the component terminals will be located. Screen or stencil printing, allowing simultaneous application of paste on all required points, is the most commonly used method for applying solder for a reflow process. Components are then placed in the solder paste. The solder pastes are a viscous mixture of spherical solder powder, thixotropic vehicle, flux and in some cases, flux activators.

During the reflow process, the completed assembly is heated to cause the flux to activate, then heated further, causing the solder to melt and bond the components to the board. As reflow occurs, components whose terminations displace more weight, in solder, than the components weight will float in the molten solder. Surface tension forces work toward establishing the smallest possible surface area for the molten solder. Solder surface area is minimized when the component termination is in the center of the land pad and the solder forms an even fillet up the end termination. Provided the boards pads are properly designed and good wetting occurs, solder surface tension works to center component terminations on the boards connection pads. This centering action is directly proportional to the solder surface tension. Therefore, it is often advantageous to engineer reflow processes to achieve the highest possible solder surface tension, in direct contrast to the desire of minimizing surface tension in wave soldering.

In designing a reflow temperature profile, it is important that the temperature be raised at least 20°C above the melting or liquidus temperature to ensure complete solder melting, flux activation, joint formation and the avoidance of cold melts. The time the parts are held above the melting point must belong enough to alloy the alloy to wet, to become homogenous and to level, but not enough to cause leaching of solder, metallization or flux charring.

A fast heating rate may not always be advantageous. The parts or components may act as heat sinks, decreasing the rate of rise. If the coefficients of expansion of the substrate and components are too diverse or if the application of heat is uneven, fast breaking or cooling rates may result in poor solder joints or board strengths and loss of electrical conductivity. As stated previously, thermal shock can also damage components. Very rapid heating may evaporate low boiling point organic solvents in the flux so quickly that it causes solder spattering or displacement of devices. If this occurs, removal of these solvents before reflow may be required. A slower heating rate can have similar beneficial effects.

InfraRed (IR) Reflow

InfraRed (IR) reflow is the method used for the reflowing of solder paste by the medium of a focused or unfocused infrared light. Its primary advantage is its ability to heat very localized areas.

The IR process consists of a conveyor belt passing through a tunnel, with the substrate to be soldered sitting on the belt. The tunnel consists of three main zones; a non-focused pre-

heat, a focused reflow area and a cooling area. The unfocused infrared areas generally use two or more emitter zones, thereby providing a wide range of heating profiles for solder reflow. As the assembly passes through the oven on the belt, the time/temperature profile is controlled by the speed of the belt, the energy levels of the infrared sources, the distance of the substrate from the emitters and the absorptive qualities of the components on the assembly.

The peak temperature of the infrared soldering operation should not exceed 220°C. The rate of temperature rise from the ambient condition to the peak temperature must be carefully controlled. It is recommended that no individual temperature step is greater than 80°C. A preheat dwell at approximately 150°C for 60 seconds will help to alleviate potential stresses resulting from sudden temperature changes. The temperature ramp up rate from the ambient condition to the peak temperature should not exceed 4°C per second; the ideal gradient being 2°C per second. The dwell time that the chip encounters at the peak temperature should not exceed 10 seconds. Any longer exposure to the peak temperature may result in deterioration of the device protection properties. Cooling of the substrate assembly after solder reflow is complete should be by natural cooling and not by forced air.

The advantages of IR Reflow are its ease of setup and that double sided substrates can easily be assembled. Its biggest disadvantage is that temperature control is indirect and is dependent on the IR absorption characteristics of the component and substrate materials.

On emergence from the solder chamber, cooling to ambient should be allowed to occur naturally. Natural cooling allows a gradual relaxation of thermal mismatch stresses in the solder joints. Forced air cooling should be avoided as it can induce thermal breakage.

The recommended temperature profile for the IR reflow soldering process is as Table 4 and Figure 6.

TABLE 4. RECOMMENDED TEMPERATURE PROFILE FOR IR REFLOW SOLDER PROCESS

INFRARED (IR) REFLOW	
TEMPERATURE (°C)	TIME (SECONDS)
25-60	60
60-120	60
120-155	30
155-155	60
155-220	60
220-220	10
220-50	60

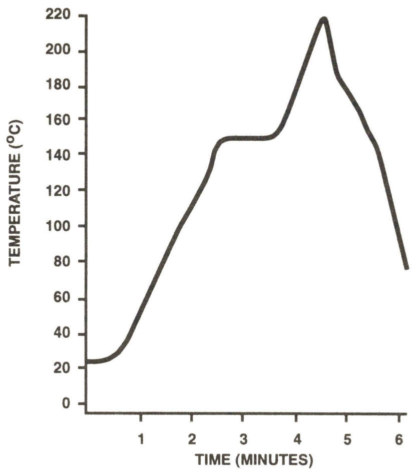


FIGURE 6. TYPICAL TEMPERATURE PROFILE

Vapor Phase Reflow

Vapor phase reflow soldering involves exposing the assembly and joints to be soldered to a vapor atmosphere of an inert heated solvent. The solvent is vaporized by heating coils or a molten alloy, in the sump or bath. Heat is released and transferred to the assembly where the vapor comes in contact with the colder parts of the substrate and then condenses. In this process all cold areas are heated evenly and no areas can be heated higher than the boiling point of the solvent, thus preventing charring of the flux. This method gives a very rapid and even heating affect. Further advantages of vapor phase soldering is the excellent control of temperature and that the soldering operation is performed in an inert atmosphere.

The liquids used in this process are relatively expensive and so, to overcome this a secondary less expensive solvent is often used. This solvent has a boiling temperature below 50°C. Assemblies are passed through the secondary vapor and into the primary vapor. The rate of flow through the vapors is determined by the mass of the substrate. As in the case of all soldering operations, the time the components sit at the peak temperature should be kept to a minimum. The dwell time is a function of the circuit board mass but should be kept to a minimum.

On emergence from the solder system, cooling to ambient should be allowed to occur naturally. Natural cooling allows a gradual relaxation of thermal mismatch stresses in the solder joints. Forced air cooling should be avoided as it can induce thermal breakage.

The recommended temperature profile for the vapor phase soldering process is as Table 5 and Figure 7.

TABLE 5. RECOMMENDED TEMPERATURE PROFILE FOR VAPOR PHASE REFLOW PROCESS

VAPOR PHASE REFLOW	
TEMPERATURE (^oC)	TIME (SECONDS)
25-90	8
90-150	13
150-222	3
222-222	10
222-80	7
80-25	10

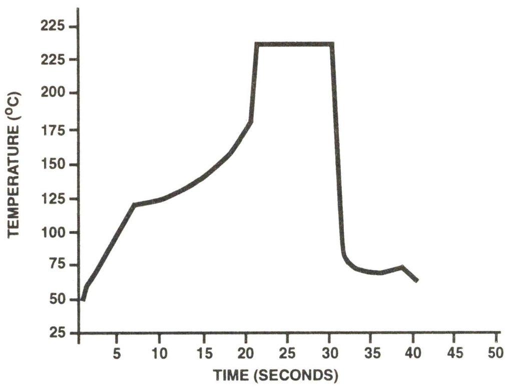


FIGURE 7. TYPICAL TEMPERATURE PROFILE

Wave Solder

This technique, while primarily used for soldering thru hole or leaded devices inserted into printed circuit boards, has also been successfully adapted to accommodate a hybrid technology where leaded, inserted components and adhesive bonded surface mount components populate the same circuit board.

The components to be soldered are first bonded to the substrate by means of a temporary adhesive. The board is then fluxed, preheated and dipped or dragged through two waves of solder. The preheating stage serves many functions. It evaporates most of the flux solvent, increases the activity of the flux and accelerates the solder wetting. It also reduces the magnitude of the temperature change experienced by the substrate and components.

The first wave in the solder process is a high velocity turbulent wave that deposits large quantities of solder on all wettable surfaces it contacts. This turbulent wave is aimed at solving one of the two problems inherent in wave soldering surface mount components, a defect called voiding (i.e. skipped areas). One disadvantage of the high velocity turbulent wave is that it gives rise to a second defect known as bridging, where the excess solder thrown at the board by the turbulent wave spans between adjacent pads or circuit elements thus creating unwanted interconnects and shorts.

The second, smooth wave accomplishes a clean up operation, melting and removing any bridges created by the turbulent wave. The smooth wave also subjects all previous soldered and wetted surfaces to a sufficiently high temperature to ensure good solder bonding to the circuit and component metallizations.

In wave soldering, it is important that the solder have low surface tension to improve its surface wetting characteristics. Therefore, the molten solder bath is maintained at temperatures above its liquid point.

On emergence from the solder wave, cooling to ambient should be allowed to occur naturally. Natural cooling allows a gradual relaxation of thermal mismatch stresses in the solder joints. Forced air cooling should be avoided as it can induce thermal breakage.

The recommended temperature profile for the wave soldering process is as Table 6:

TABLE 6. RECOMMENDED TEMPERATURE PROFILE FOR WAVE SOLDER PROCESS

WAVE SOLDER	
TEMPERATURE (^oC)	TIME (SECONDS)
25-125	60
125-180	60
180-260	60
260-260	5
260-180	60
180-80	60
80-25	60

Termination Options

Harris offers three types of termination finish on the Multilayer product series:

1. Silver/Platinum (standard)
2. Silver/Palladium (optional)
3. Nickel/Tin (optional)

The Nickel/Tin plated termination can provide certain solder process application benefits such as:

- A better match to Tin/Lead solders resulting in improved solder wetting and solder fillet height (typically 70% of component height).
- An enhanced resistance to solder leaching permits greater flexibility/latitude in the design and control of solder processes. (See the temperature-time graph below.)
- An alternative material when silver end terminations are restricted.

Solder Process Time Advantages for Nickel/Tin Terminated Multilayer Suppressors

Certain surface mount soldering processes require long duration or multiple soldering cycles for top and bottom side assemblies and/or for reworking rejected product. In these instances, devices with a Nickel/Tin finish offer greater dwell time, for example, when end termination leaching is of concern. The Solder Temperature-Time Curve shown can be used as a guideline when designing process variables and rework operations and illustrates the greater latitude afforded with this material.

Since end termination leaching is a function of the cumulative molten dwell time, then the molten time duration allowed at subsequent operations is reduced by the percentage of time used by the initial operation. Using the curve for the applicable material,

$$\frac{\text{Total Time at Initial Temp - Actual Time at Initial Temp}}{\text{Total Time at Initial Temp}}$$

$$\times \text{Total Time Permitted at the Subsequent Temp}$$

For example, if the initial process is for 20 seconds at 220°C and the next process is at 260°C, then the maximum time allowed at 260°C is:

For Nickel/Tin Termination:

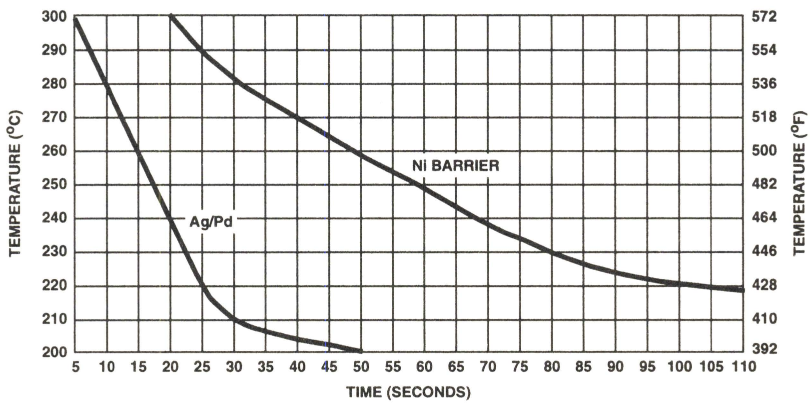
$$\frac{100-20}{100} \times 48 = 38.4 \text{ seconds}$$

For Ag/Pd Termination:

$$\frac{25-20}{25} \times 15 = 3.0 \text{ seconds}$$

Also, if the initial soldering process is for 10 seconds at 280°C, the Nickel/Tin termination can withstand a further 20 seconds at 280°C or an equivalent percentage of time at a subsequent temperature. For example, If the next soldering process is at 230°C, the total time allowed at this temperature is:

$$\frac{30-10}{30} \times 80 = 53 \text{ seconds}$$



NOTES:

1. Comparative Temperature-Time data for Silver/Palladium and Nickel/Tin terminated Multilayer Suppressors.
2. The curves indicate the point at which 5% leaching of the termination will occur after immersion in a static solder bath for an 0805 size device.
3. Static solder bath = Sn/Pb (63/67). RMA no clean flux.

FIGURE 8. SOLDER TEMPERATURE-TIME CURVE

Cleaning Methods and Cleaning Fluids

The objective of the cleaning process is to remove any contamination from the board, which may affect the chemical, physical or electrical performance of the circuit in its working environment.

There are a wide variety of cleaning processes which can be used, including aqueous based, solvent based or a mixture of both, tailored to meet specific applications. After the soldering of surface mount components there is less residue to remove than in conventional through hole soldering. The cleaning process selected must be capable of removing any contaminants from beneath the surface mount assemblies. Optimum cleaning is achieved by avoiding undue delays between the cleaning and soldering operations; by a minimum substrate to component clearance of 0.15mm and by avoiding the high temperatures at which oxidation occurs.

Harris recommends 1, 1, 1 trichloroethane solvent in an ultrasonic bath, with a cleaning time of between two and five minutes. Other solvents which may be better suited to a particular application and can also be used may include one or more of the following:

TABLE 7. CLEANING FLUIDS

Water	Acetone
Isopropyl Alcohol	Fluorocarbon 113
Fluorocarbon 113 Alcohol Blend	N-Butyl
1, 1, 1 Trichloroethane Alcohol Blend	Trichloroethane
Toluene	Methane

Solder Defects

Non-Wetting:

This defect is caused by the formation of oxides on the termination of the components. The end termination has been exposed to the molten solder material but the solder has not adhered to the surface; base metal remains exposed. The accepted criterion is that no more than 5% of the terminated area should remain exposed after an immersion of 5 seconds in a static solder bath at 220^{o}C, using a nonactive flux.

Leaching:

This is the dissolving of the chip termination into the molten solder. It commences at the chip corners, where metal coverage is at a minimum. The result of leaching is a weaker solder joint. The termination on the Harris surface mount suppressors consist of a precious metal alloy which increases the leach resistance capability of the component. Leach resistance defined as the immersion time at which a specified proportion of the termination material is visibly lost, under a given set of soldering conditions.

De-Wetting:

This condition results when the molten solder has coated the termination and then receded, leaving irregularly shaped mounds of solder separated by areas covered with a thin solder film. The base metal is not exposed.

References

For Harris documents available on the web, see http://www.semi.harris.com/
Harris AnswerFAX (407) 724-7800.

[1] "Transient Voltage Suppression Devices", Harris Semiconductor DB450.

[2] CANE SMT 2588, Syfer Technology Limited, UK.

ESD and Transient Protection Using the SP720

Author: Wayne Austin

The need for transient protection in integrated circuits is driven by the quest for improved reliability at lower cost. The primary efforts for improvement are generally directed toward the lowest possible incidence of over-voltage related stresses. While electrical over-stress (EOS) is always a potential cause for failure; a discipline of proper handling, grounding and attention to environmental causes can reduce EOS causes for failure to a very low level. However, the nature of hostile environments cannot always be predicted. Electrostatic Discharge (ESD) in some measure, is always present and the best possible ESD interface protection may still be insufficient. As the technology of solid state progresses, the occurrence of ESD related IC failures is not uncommon. There is a continuing tendency for both ESD and EOS failures, due in part, to the smaller geometries of today's VLSI circuits.

The solid state industry has generally acknowledged a standard for the level of capability in LSI designs of ±2000V for the Human Body Model where the defined capacitance is 100pF and the series resistance is 1500Ω. However, this level of protection may not be adequate in many applications and can be difficult to achieve in some VLSI technologies. Normal precautions against ESD in the environment of broad based manufacturing are often inadequate. The need for a more rugged IC interface protection will continue to be an established goal.

Historically, it should be recognized that early IC development began to address the ESD problem when standards for handling precautions did not exist. High energy discharges were a common phenomena associated with monitor and picture tube (CRT) applications and could damage or destroy a solid state device without direct contact. It was recognized that all efforts to safe-guard sensitive devices were not totally sufficient. Small geometry signal processing circuits continued to sustain varying levels of damage through induced circulating currents and direct or indirect exposure in handling. These energy levels could be substantially higher than the current standard referenced in MIL-STD-3015.7; also referred to as the Human Body Model.

The recognized need for improved ESD protection was first precipitated under harsh handling conditions; particularly in applications that interfaced to human contact or from the interaction of mechanical parts in motion. The popular features of component and modular electronic equipment have continued to generate susceptibility to IC damage while in continuing use. These market items include computers and peripherals, telecommunication equipment and consumer electronic systems. While some IC's may only see the need for ESD protection while in manufacturing assembly or during service in the field, the most common cause for ESD failures can still be related to a human contact. Moreover, educational efforts have improved today's manufacturing environment substantially reduce failures that relate to the mechanical handling. The ESD failure causes that relate to mechanical handling now have a test standard referred to as a Machine Model which relates to the source of the generated energy.

While the electrical model for an energy source is generally accepted as a capacitor with stored charge and a series resistance to represent the charge flow impedance, the best means to handle the high energy discharge is not so clearly evident. The circuit of Figure 1 illustrates the basic concept that is applied as a method of ESD testing for the Human Body Model. The ESD energy source is shown as a charged capacitor C_D and series connected, source impedance, resistor R_D. The point of contact or energy discharge is shown, for test purposes, as a switch external to the IC. A protection structure is often included on an IC to prevent damage from an ESD energy source. To properly protect the circuit on the IC the on-chip switch, S_S, is closed when a discharge is sensed and shunts the discharge energy through a low impedance resistor (R_S) to ground. It is imperative that the resistance of the discharge path be as low as practical to limit dissipation in the protection structure. It is not essential that the ground be the chip substrate or the package frame. The energy may be shunted via the shortest path external to the chip to an AC or DC ground.

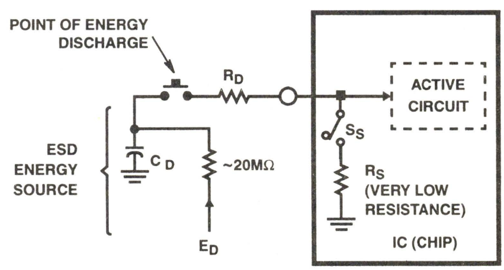


FIGURE 1. ESD TEST FOR AN ON-CHIP PROTECTION CIRCUIT USING THE MIL-STD-883, METHOD 3015.7 (HUMAN BODY MODEL)

This conceptual method has been used in many IC designs employing a wide variation of structures, depending the IC technology and degree of protection needed. The switch, S_S is generally a threshold sensitive turn-ON at some voltage level above or below the normal signal range; however, it must be within the a safe operating range of the device being protected. The resistance, R_S is shown as the inherent series resistance of the protection structure when it is discharging (dumping) the ESD energy. In its simplest forms, the protection structures may be diodes and zeners, where the sensing threshold is the forward turn-ON or zener threshold of the device. The inherent resistance becomes the bulk resistance of the diode structure when it is conducting. Successful examples of two such protection structures that have been used to protect sensitive inputs to MOS devices are shown in Figure 2. The back-to-back zener structure shown for the dual-gate MOSFET was employed in the 3N - dual gate MOS devices before IC technology was firmly established. The series poly and stacked diode structure used to shunt ESD energy followed several variations for use in CMOS technology and was employ in the CD74HC/HCT - High Speed CMOS family of logic devices. This CMOS protection structure is capable of meeting the 2000V requirements of MIL-STD-883, Method 3015.7; where the R_D in Figure 1 is 1500Ω and C_D is 100pF.

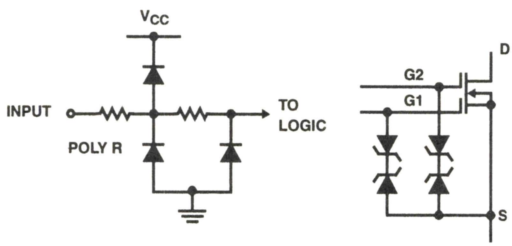


FIGURE 2. ESD AND TRANSIENT PROTECTION EFFECTIVELY USED IN MOS AND CMOS DEVICES

Due to greater emphasis on Reliability under harsh application conditions, more ruggedized protection structure have been developed. A variety of circuit configurations have been evaluated and applied to use in production circuits. A limited introduction to this work was published in various papers by L. Avery (See Bibliography). To provide the best protection possible within economic constraints, it was determined that SCR latching structures could provide very fast turn-ON, a low forward on resistance and a reliable threshold of switching. Both positive and negative protection structures were readily adapted to bipolar technology. Other defining aspects of the protection network included the capability to be self-protecting to a much higher level than the signal input line being protected. Ideally, when a protection circuit is not otherwise needed, it should have no significant loading effect on the operating circuit. As such, it should have very little shunt capacitance and require minimal series resistance to be added to the signal line of the active circuit. Also, where minimal capacitance loading is essential for a fast turn-ON speed, the need for a simpler structure is indicated.

The switching arrangement for a basic and simple protection structure is shown in Figure 3. Each high side and low side protection structure (R_S and S_S) is an embedded device, taking advantage of the P substrate and epitaxial N material used in bipolar technology. Each cell contains an SCR with a series dropping resistor to sense an over-voltage turn-ON condition and trip the SCR (Switch S_S) into latch. The ON-resistance (R_S) of the latched SCR is much lower than R_D and, depending on the polarity of the ESD voltage, dumps energy from the input signal line through the positive or negative switch to ground. The return to ground for either ESD polarity is not limited by voltage supply definition, but may be to positive or negative supply lines, if this suits the needs of the application. When the energy is dissipated and forward current no longer flows, the SCR automatically turns-OFF.

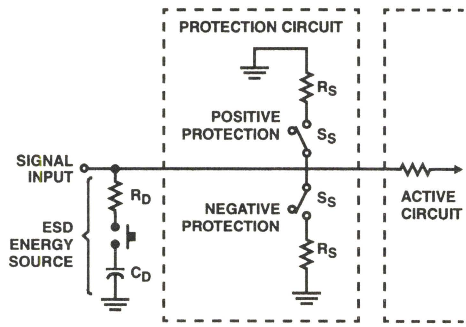


FIGURE 3. ESD AND TRANSIENT PROTECTION CIRCUIT

Figure 4 shows the diagram of a positive and negative cell protection circuit as it applies to the SP720. The PNP and NPN transistor pairs are used as the equivalent SCR structures. Protection in this structure allows forward turn-ON to go marginally above the +V supply to turn-ON the high-side SCR or marginally below the -V supply to turn-ON the low-side SCR. The signal line to the active device is protected in both directions and does not add series impedance to the signal input line. A shunt resistance is used to forward bias the PNP device for turn-ON but is not directly connected to the signal line. As an on-chip protection cell, this structure may be next to the input pad of the active circuit; which is the best location for a protection device. However, for many applications, the technology of the active chip may not be compatible to structures of the type indicated in Figure 4. This is particularly true in the high speed CMOS where the substrates are commonly N type and connected to the positive supply of the chip. The protection cell structure shown in Figure 4 is not required to be on the active chip because it does not sense series input current to the active device. The sense mechanism is voltage threshold referenced to the V+ and V- bias voltages.

The cell structure of the SCR pair of Figure 4 are shown in the layout sketch and profile cutouts of Figure 5. It should be noted that the layout and profiles shown here are equivalent structures intended for tutorial information. The structures are shown on opposite sides of the 'IN" chip bonding pad, as is the case for the SP720. As needed for a preferred layout, the structures are adjacent to the pad and as close to the positive and negative supply lines as possible. The common

and best choice for effective layout is to provide a ground ring (V-) around the chip and to layout with minimum distance paths to the positive supply (V+). In the SP720 the V- line is common to the substrate and frame ground of the IC.

The equivalent circuit diagram of the SP720 is shown in Figure 6. Each switch element is an equivalent SCR structure where 14 positive and negative pairs as shown in Figure 4 are provided on a single chip. Each positive switching structure has a threshold reference to the V+ terminal, plus one V_{BE} (based-to-emitter voltage equal to one diode forward voltage drop). Similarly, each negative switching pair is referenced to the V- terminal minus one V_{BE}.

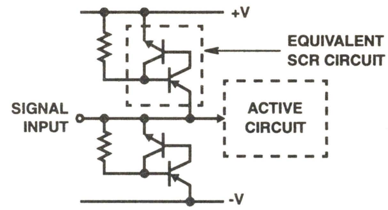


FIGURE 4. PROTECTION CELLS OF THE SP720 SCR ARRAY

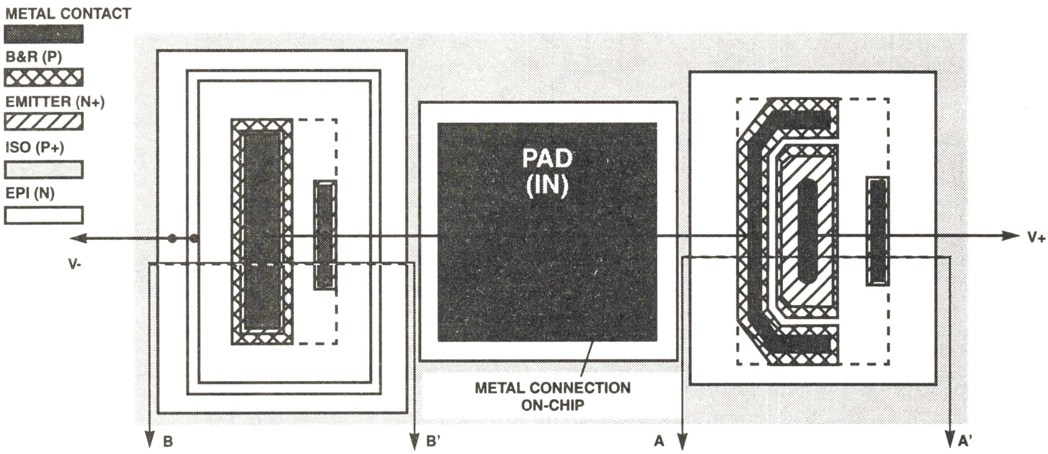


FIGURE 5A. HIGH AND LOW CELL PAIR LAYOUT; SHOWN WITHOUT PROTECT, METAL AND FIELD OXIDE LEVELS (NOT TO SCALE)

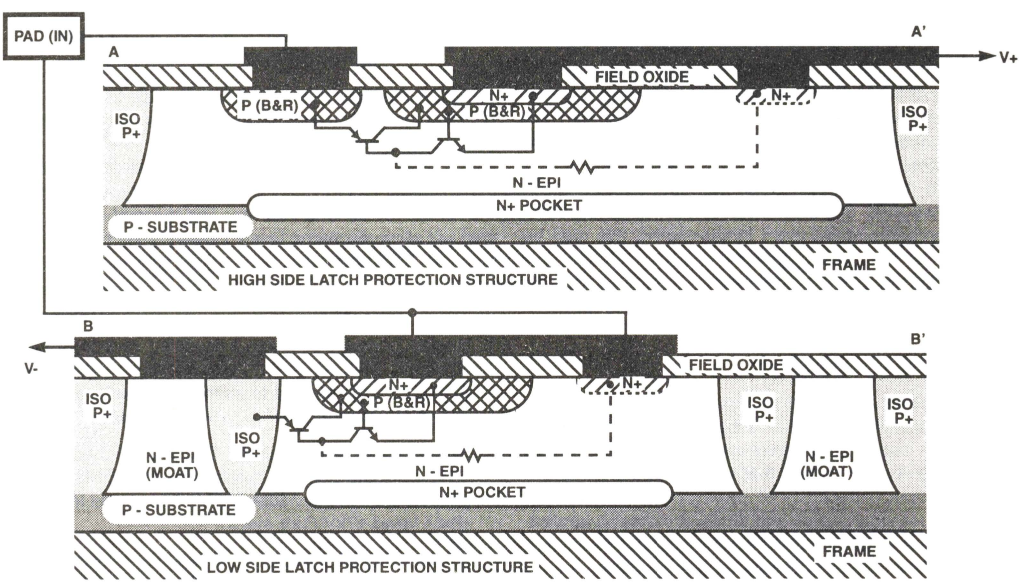


FIGURE 5B. PROFILES OF THE HIGH AND LOW SIDE SP720 SCR PROTECTION PAIR (NOT TO SCALE)

The internal protection cells of the SP720 are directly connect to the on-chip power supply line (+V) and the negative supply line (-V), which are substantial in surface metal content to provide low dropping resistance for the high peak currents encountered. Since both positive or negative transients can be expected, the SCR switches direct the positive voltage energy to V+ and the negative voltage sourced energy to V- (substrate) potential to provide fast turn-ON with low ON resistance to protect the active circuit.

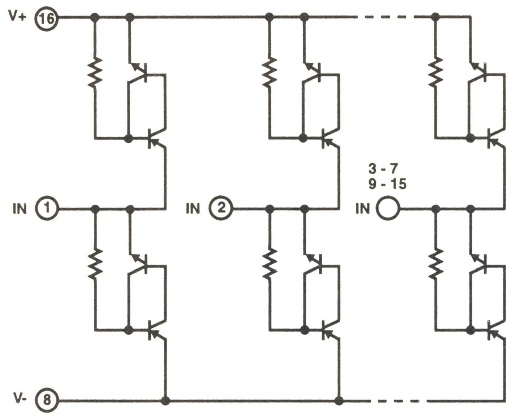


FIGURE 6. EQUIVALENT CIRCUIT DIAGRAM OF THE SP720

The V+ and V- supply lines of the SP720 are not required to be the same as those of the circuit to be protected. However, over-voltage protection is referenced to the V+ and V- supply voltages for all of the signal input terminals, IN1-IN7 and IN9-IN15. The V+ and V- supply voltages to the SP720 may be changed to suite the needs of the circuit under protection. The range of voltage may be power supply levels ranging from 4.5V up to the 35V maximum rating of the SP720. Lower levels of voltage are possible but with some degradation of the switching speed which is nominally 2ns. Also, the input capacitance which is nominally 3pF can be expected to increase. There is no significant quiescent current in the SP720 other than reverse diode junction current which nominally less than 50nA over the rated -40°C to 105°C operating temperature. At room temperatures, this may be as low as a few nanoamperes. Because of the low dissipation of the SP720, the chip temperature can be expected to be close to the environment of the physical location where it is applied to use.

Protection Levels of the SP720

For a given level of voltage or power, there is a defined degree of protection compatible to that need. For the SP720, the protection circuits are designed to clamp over-voltage within a range of peak current that will substantially improve the survival input expectancy of average monolithic silicon circuits used for small signal and digital processing applications. Within itself, the SP720 should be expected to survival peak current and voltage surges within the maximum ratings defined in the data sheet. For voltage, the static DC and short duration transient capability is essentially the same. The process capability is typically better than 45V, allowing maximum continuous DC supply ratings to be conservatively rated at 35V. The current capability of any one SCR section is rated at 2A peak but is duration limited by the transient heating effect on the chip. As shown in Figure 7, the resistance of the SCR, when it is latched, is approximately 0.96Ω and the SCR latch threshold has 1.08V of offset. For EOS, the peak dissipation can be calculated as follows:

For: 2A Peak Current, $R_D = 1500\Omega$,

Then: $V_{IN(PK)} = 1.08V \text{ (Offset)} + (0.96\Omega \times 2A) = 3V$

The peak dissipation is $P_D = 3V \times 2A = 6W$

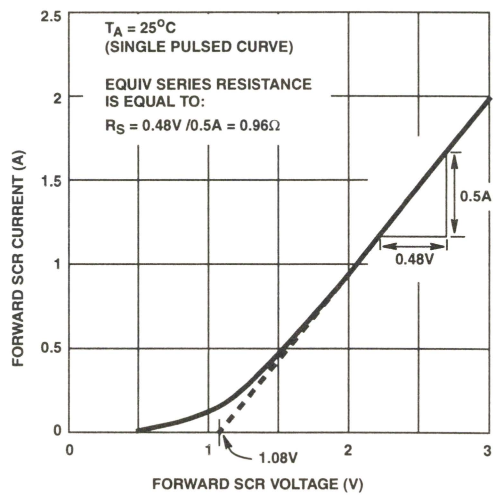


FIGURE 7. SCR FORWARD CURRENT vs VOLTAGE CHARACTERISTICS

While 2A through 1500Ω is 3000V, which is not an exceptionally high ESD level of voltage, it does represent the EOS capability, provided the time duration for the 6W of dissipation is limited to a few milliseconds. The dissipation of the 16 pin DIP and 16 pin SOIC packages are typically less than 1W for steady state conditions. The thermal capacity of the chip will allow discharge levels several times higher than this because ESD normally has a much shorter duration. The actual results for ESD tests on the SP720 as an isolated device are as follows:

1. Human Body Model using a modified version of the MIL-STD-883, Method 3015.7; with V+ and V- grounded and ESD discharge applied to each individual IN pin - Passed all test levels from ±9kV to ±16kV (1kV steps).
2. Human Body Model using the MIL-STD-883, Method 3015.7 (with V- only grounded) and ESD discharge applied to each individual IN pin - Passed all test levels to ±6kV, failed ±7kV (1kV steps).
3. Machine Model using EIAJ IC121 ($R_D = 0\Omega$); discharge applied to IN pins with all others grounded - Passed all test levels to ±1kV, failed ±1.2kV; (200V steps).

4. While there are many potential uses for the SP720, the circuit of Figure 8 shows a normal configuration for protecting input lines to a sensitive digital IC. Each line is connected to an IN- Input of the SP720 in a shunt connection. As a test model a 2μ digital ASIC CMOS IC was used to evaluate the ESD level of capability provided by the SP720. Without external protection, the ESD level of capability of the CMOS process was typically no better than ±2.5kV. When the SP720 was applied to use as shown in Figure 8, the ESD resistance to damage was better than ±10.2kV. (Higher levels were not evaluated at the time due to high voltage limitations.)

It should be noted that the MIL-STD-883, Method 3015.7 test allows for one pin as a reference when testing. While this cannot be disputed as handling limitation, it is not a test for all aspects of applied use. To properly apply the SP720 to use in the application specifically requires that the V- pin be connected to a negative supply or ground and the V+ pin be connected to a positive supply. The SP720 was designed to be used with the supply terminals bias and, as such, has better than ±16kV of ESD capability. For this reason, the modified test method as described, with the V+ pin connected via a ground return, is correct when the circuit is assembled for use.

SP720 CMOS Protection Model

Where the need to provide ESD protection for CMOS circuits is the primary interest for the application of the SP720, interface characteristics of the device to be protected may lead to some specific problems. Application related issues and precautions are discussed here to assist the circuit designer in achieving maximum success in EOS/ESD protection.

CMOS Input Protection

CMOS logic has limited on-chip protection and may contain circuit elements that add difficulty to the task of providing external protection. Consider the case where the input structure of a CMOS device has on-chip protection but only to the extent that it will withstand Human Body Model minimum requirement for ESD when tested under the MIL-STD-883, Method 3015.7. This is normally ±2kV where the charged capacitor is 100pF and the series resistor to the device under test is 1500Ω. The circuit of Figure 9 shows the typical network for an HC logic circuit where the input polysilicon resistor, R_P is typically 120Ω.

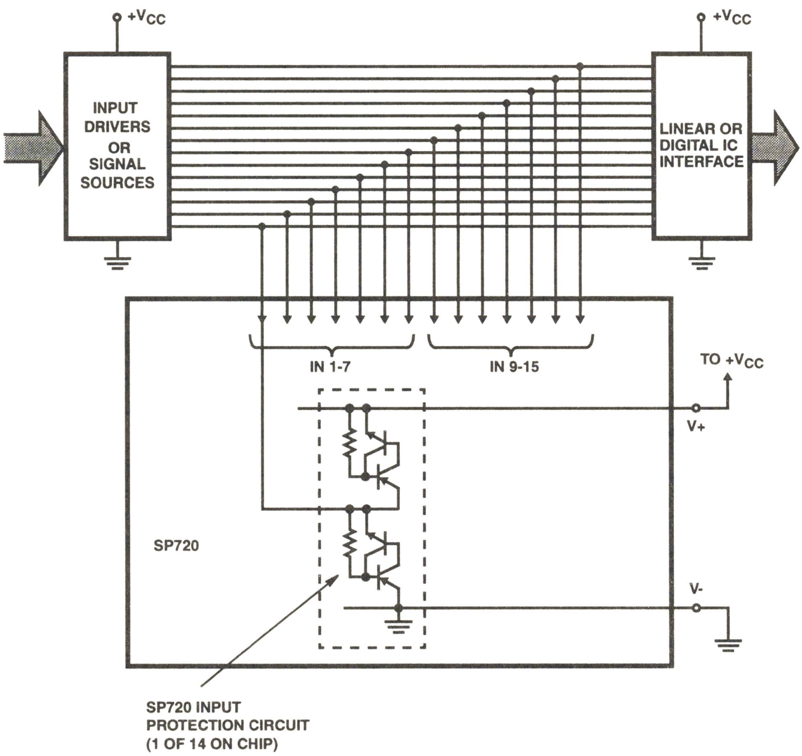


FIGURE 8. PRACTICAL APPLICATION AND TEST EVALUATION CIRCUIT

When there is a surge or ESD voltage applied to the input structure, the diodes shunt current to V_{CC} or GND to protect the logic circuits on the chip. The on-chip series resistors limit peak currents. If there is a positive transient voltage, $V_{CS}(t)$, applied to the input of the CMOS device, the diode, D_1 will conduct when the forward voltage threshold exceeds the power supply voltage, V_{CC} plus the forward diode voltage drop of D_1, V_{FWD1}. As the voltage at the input is further increased, the CMOS current, I_{CS} is shunted through R_P and D_1 to V_{CC} such that the transient input voltage is

$$V_{CS}(t) = I_{CS}(t) \bullet R_P + V_{FWD1} + V_{CC} \quad \text{[for Pos. } V_{CS}(t)] \qquad \text{(EQ. 1)}$$

or

$$I_{CS}(t) = [V_{CS}(t) - (V_{FWD1} + V_{CC})]/R_P \qquad \text{(EQ. 1A)}$$

Similarly, when there is a negative transient, current initially conducts at the negative threshold of diode D_2, V_{FWD2} to shunt negative current at the input, i.e.

$$V_{CS}(t) = I_{CS}(t) \bullet R_P + V_{FWD2} \quad \text{[for Neg. } V_{CS}(t)] \qquad \text{(EQ. 2)}$$

or

$$I_{CS}(t) = [V_{CS}(t) - V_{FWD2}]/R_P \qquad \text{(EQ. 2A)}$$

While the circuit of Figure 9 is specifically that of the HC logic family (one cell of the Hex Inverter, 74HCU04), many CMOS devices have a similar or an equivalent internal protection circuit. When compared to the SCR structure of the SP720, the on-chip diodes of the protection network in Figure 9 have lower conduction thresholds.

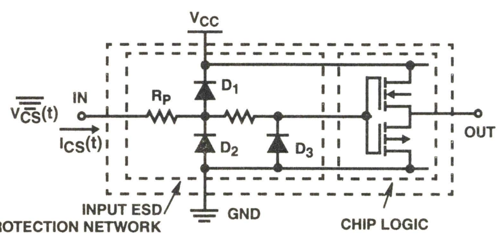


FIGURE 9. TYPICAL CMOS IC INPUT PROTECTION CIRCUIT

SP720 to CMOS Interface

Figure 10 shows the SCR cell structures of one protection pair in the SP720. In this example, the V+ of the SP720 is connected to the V_{CC} logic supply and the V- is connected to logic GND. The IN terminal of the SP720 is connected to the CMOS logic device input through a resistor R_I. When a negative transient voltage is applied to the input circuit of Figure 10, the Reverse SCR Protection Circuit turns on when voltage reaches the forward threshold of the PNP device and current conducts through the SCR resistor to forward bias the PNP transistor. The PNP device then supplies base current to forward bias and turn on the NPN device. Together, the PNP and NPN transistors form an SCR which is latched on to shunt transient current from IN to V-. The Forward SCR Protection Circuit has the same sequence for turn on when a positive transient voltage is applied to the input and conducts to shunt transient current from IN to V+ (V_{CC}).

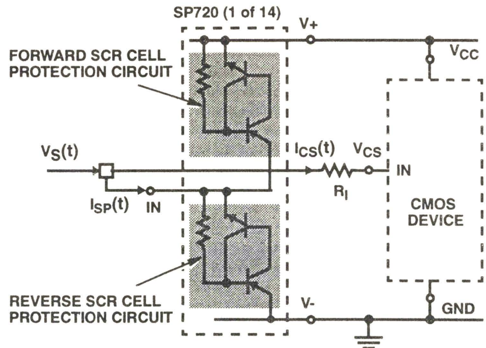


FIGURE 10. SP720 SCR INTERFACE TO A CMOS INPUT WITH R_I ADDED TO ILLUSTRATE MORE EFFECTIVE ESD PROTECTION FOR CMOS DEVICES

The Voltage-Current characteristic of the SCR is similar to a diode at low currents but changes to low saturated on resistance at high currents. As shown in the SP720 data sheet, the forward SCR (latched on) voltage is ~1V at 60mA which is ~0.2V higher than a typically junction diode. The fully saturated turn on approaches 0.5A at 1.5V. When the SCR is paralleled with the a CMOS device input having an on-chip protection circuit equivalent to Figure 9, some of the current necessary to latch the SCR is shunted into the CMOS input. For some devices this may be sufficient for an ESD discharge to damage the CMOS input structure before the SP720 is latched on.

The trade-off for achieving a safe level of ESD protection is switching speed. The most effective method is the addition of the series resistor, R_I as shown in Figure 10. The series input resistor, as shown, is a practical method to limit current into the CMOS chip during the latch turn on of the SP720 SCR network. The value of R_I is dependent on the safe level of current that would be allowed to flow into the CMOS input and the loss of switching speed that can be tolerated. The level of transient current, I_{CS} that is shunted into the CMOS device is determined by the series resistor, R_I and the voltage developed across the CMOS protection devices, R_P and D_1 or D_2, plus some contribution from the path of diode, D_3 for negative transients.

As shown in Figure 11, the voltage across the SP720 SCR element is determined by its turn on threshold, V_{TH} and the saturated resistance, R_S when latched. The empirically derived equation for the voltage drop across the SP720 voltage is

$$V_{SP}(t) = I_{SP}(t) \bullet R_S + V_{TH} \qquad \text{(EQ. 3)}$$

or

$$I_{SP}(t) = [V_{SP}(t) - V_{TH}]/(R_S) \qquad \text{(EQ. 3A)}$$

where $V_{TH} \sim \pm 1.1V$ and $R_S \sim 1\Omega$.

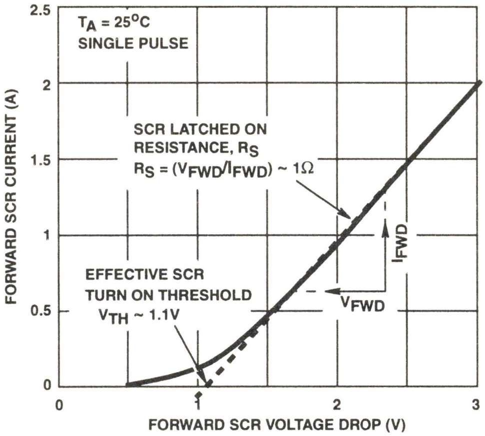


FIGURE 11. FORWARD TURN ON CHARACTERISTIC OF AN SP720 SCR CELL

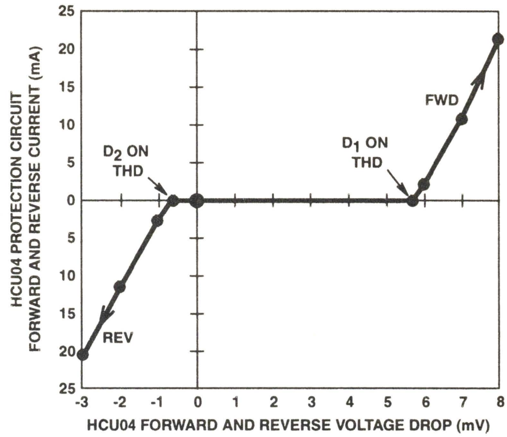


FIGURE 12. FORWARD AND REVERSE PROTECTION CIRCUIT INPUT VOLTAGE-CURRENT CHARACTERISTIC OF THE HCU04 SHOWN FOR V_{CC} = 5V, (i.e., D_1 THD ~ 5V + 0.7V)

where current conduction in the SP720 may be positive or negative, depending on the polarity of the transient. For the circuit of Figure 10, $V_S(t)$ is also the input voltage to the resistor, R_I in series to the input of the CMOS device. When latched on, the impedance of the SP720 is much less than the input impedance of either R_I or the CMOS input protection circuit. Therefore, the CMOS loop current can be determined by the voltage, $V_S(t)$ and the known conditions from Equation 3.

For a **negative** transient input to the CMOS HCU04, the loop equation is

$$V_S(t) = I_{CS}(t) \bullet (R_I + R_P) + V_{FWD2} \qquad \text{(EQ. 4)}$$

or

$$I_{CS}(t) = [V_S(t) - V_{FWD2}]/(R_I + R_P) \qquad \text{(EQ. 4A)}$$

An equation solution for an input transient may be more directly solved by empirical methods because of the non-linear characteristics. Given a transient voltage, $V_S(t)$ at the input, a value for R_I can be determined for a safe level of peak current into a CMOS device. The input Voltage-Current characteristic of CMOS device should be known. As a first order approximation, the CMOS V-I curve tracer input characteristics of the 74HCU04 are shown in Figure 12. As indicated in Figure 12, the voltage drop across R_P and R_I in series (R_P~120Ω) will be significantly larger than the delta changes in the forward voltage drop of the D_1 or D_2 diodes over a wide range of current. As such, we can effectively assume V_{FWD} ~ 0.75V for moderate levels of current.

Example Transient Solution

Based on the circuit of Figure 10, negative and positive ESD discharge circuit models of the SP720 and HCU04 are shown in Figure 13A and 13B. The negative ESD voltage is taken as the worse case condition because a positive ESD voltage will discharge to the V_{CC} power supply and the positive offset voltage will reduce the forward current. Using the negative model, a peak current value for I_{SP} can be determined by the transient conditions of the applied voltage, $V_S(t)$ at the input.

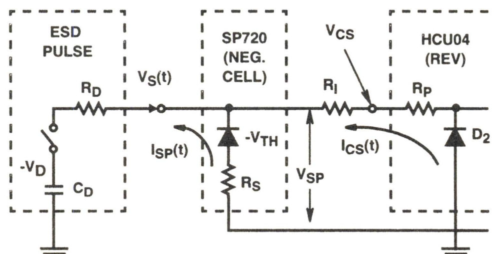


FIGURE 13A. NEGATIVE ESD DISCHARGE MODEL

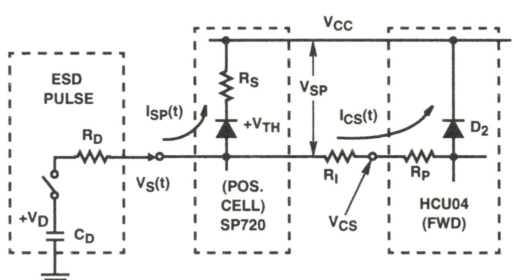


FIGURE 13B. POSITIVE ESD DISCHARGE MODEL

11

APPLICATION NOTES

Given MIL-STD ESD HBM test conditions (C_D = 100pF and R_D = 1500Ω), Equation 3 with the resistors R_D and R_S in series, we can calculate the peak current for a specified voltage, V_D on the capacitor, C_D.

$$I_{SP}(t) = [V_D(t) - V_{TH}]/(R_D + R_S) \sim V_D(t)/R_D \qquad \text{(EQ. 5)}$$

Here, V_D replaces V_S as the driving voltage; and assumes that (1) R_S is much less than R_D; (2) R_S is much less than (R_I + R_P); and (3) V_{TH} is much less than V_D. This may or may not be the general case but is true for the values indicated here. As such,

$$[I_{SP}]_{t=0} \sim V_D/1500.$$

Given an ESD discharge of -15KV, neglecting inductive effects and distributed capacitance, the peak current at time t = 0 will be ~10A. And, with the SP720 latched on as shown in Equation 3, the 10A peak current will result in an ESD pulse at the input of the SP720 of ~11V. For the HCU04 to withstand this surge of voltage, it is required that the dropping resistor, R_I attenuate the peak voltage, V_{CS} at the HCU04 input to within acceptable ratings.

The negative reverse current path is through R_I, R_P and D_2; where R_P and D_2 are part of the HCU04. For a negative ESD discharge voltage, V_D from capacitor C_D, the equation for the peak voltage, V_{CS} at the input to the HCU04 is derived as follows:

Substituting Equation 5 into Equation 3, we have

$$V_S \sim (V_D/R_D) \bullet R_S - 1.1 \qquad \text{(EQ . 6)}$$

and from Equation 2 and Equation 4A, a general solution for the V_{CS} voltage is

$$V_{CS} = [(V_S - V_{FWD2})/(R_I + R_P)] \bullet R_P + V_{FWD2} \qquad \text{(EQ. 7)}$$

For a simpler approach, one can work backwards to arrive at the correct solution. The reverse CMOS voltage vs current curve of Figure 11 indicates that a peak voltage, V_{CS} of -3V will produce a negative current of approximately -20mA which is the rated absolute maximum limit. For a -15kV ESD discharge and from Equation 6, the peak voltage, V_S is

$$V_S = (V_D/R_D) \bullet R_S - 1.1 = (-15/1500) - 1.1 = -11.1V$$

The peak current, I_{CS} from Equation 4A is

$$I_{CS} = [(V_S - V_{FWD2})/(R_I + R_P)]$$
$$= [(-11.1 - (-0.7))]/(R_I + 120\Omega)$$

Given the I_{CS} current of -20mA and solving for R_I,

$$R_I = 397.5\Omega$$

The same result can be derived from Equation 7 but is more susceptible to rounding errors and the assumed voltage drop of V_{FWD2} due to the (V_{CS} - V_{FWD2}) difference that appears in the equation.

The approximation solution given here is based on a ±20mA current rating for the HCU04 device; although, input voltage ratings are exceeded at this level of current. As such, the solution is intended to apply only to short duration pulse conditions similar to the MIL-STD-883, Method 3015.7 specifications for ESD discharge conditions. For long periods of sustained dissipation, the SP720 is limited by the rated capability of its package.

Figure 14 shows the distribution of currents for the circuit of Figure 10 given a specific value of R_I. Curves are shown for both I_S (HCU04 + SP720) and I_{SP} (SP720) versus a negative input voltage, V_S. The resistor, R_I value of 10Ω is used here primarily to sense the current flow into the HCU04. (This data was taken with the unused inputs to the HCU04 connected to ground and the unused inputs to the SP720 biased to $V_{CC}/2$ on a resistive divider.) The Figure 14 curves verify the model condition of Figure 13A with the exception that resistive heating at higher currents increases the resistance in the latched on SCR. This curve explains the ESD protection of the Harris High Speed Logic "HC" family and, in particular, demonstrates the value of the R_P internal resistor as protection for the HCU04 gate input. Added series resistance external to a signal input is always recommended for maximum ESD protection.

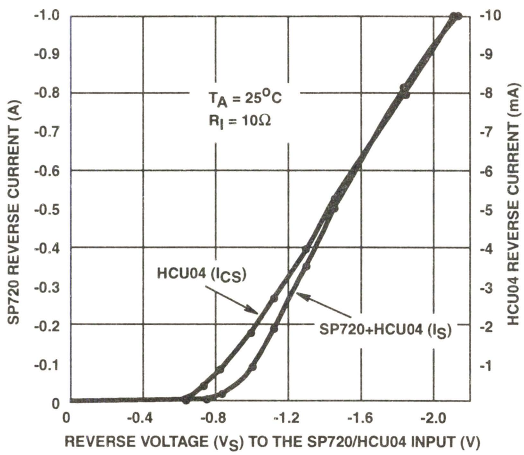


FIGURE 14. MEASURED REVERSE CURRENT vs VOLTAGE CHARACTERISTIC OF THE SP720/HCU04 FOR THE FIGURE 10 CIRCUIT PROTECTION MODE

Range of Capability

While the SP720 has substantially greater ESD self protection capability than small signal or logics circuits such as the HCU04, it should be understood that it is not intended for interface protection beyond the limits implied in the data sheet or the application note. The MIL-STD-883, Method 3015.7 condition noted here defines a human body model of 100pF and 1500Ω where the capacitor is charged to a specified level and discharged through the series resistor into the circuit being tested. The capability of the SP720 under this condition has been noted as ±15kV. And, for a machine model where no resistance is specified, a 200pF capacitor is discharged into the input under test. For the machine model the level of capability is ±1kV; again demonstrating that the series resistor used in the test or as part of the application circuit has pronounced effect for improving the level of ESD protection.

While a series resistor at the input to a signal device can greatly extend the level of ESD protection, a circuit application, for speed or other restrictions, may not be tolerant to added series resistance. However, even a few ohms of resistance can substantially improve ESD protection levels. Where an ESD sensitive signal device to be protected has no internal input series resistance and interfaces to a potentially damaging environment, added resistance between the SP720 and the device is essential for added ESD protection. Circuits often contain substrate or pocket diodes at the input to GND or V_{CC}. and will shunt very high peak currents during an ESD discharge. For example, if the HCU04 of Figure 14 is replaced with device having a protection diode to ground and no series resistor, the anticipated increase in input current is 10 times.

Shunt capacitance is sometimes added to a signal input for added ESD protection but, for practical values of capacitance, is much less effective in suppressing transients. For most applications, added series resistance can substantially improve ESD transient protection with less signal degradation.

A further concern for devices to be protected is forward or reverse conduction thresholds within the power supply range (not uncommon in analog circuits). Depending on the cost considerations, the power supply V+ and V- levels for the SP720 could be adjusted to match specific requirements. This may not be practical unless the levels are also common to an existing power supply. The solution of this problem goes beyond added series resistance for improved protection. Each case must be treated with respect to the precise V-I input characteristics of the device to be protected.

Interface and Power Supply Switching

Where separate system components with different power supplies are used for the source signal output and the receiving signal input, additional interface protection circuitry maybe needed. The SP720 would normally have the same power supply levels as the receiving (input) device it is intended to protect. When the SP720 with its receiving interface circuit is powered off, a remote source signal may be activated from a separate supply (i.e., remote bus connected systems). The user should be aware that the SP720 remains active when powered down and may conduct current from the IN input to the V+ (or V-) supply.

Within its own structure, **any** IN input of the SP720 will forward conduct to V+ when the input voltage increases to a level greater than a V_{BE} threshold above the V+ supply. Similarly, the SP720 will reverse conduct to V- when the input voltage decreases to a level less than a V_{BE} threshold below the V- supply. Either condition will exist as the V+ or V- level changes and will continue to exist as the V+ collapses to ground (or V-) when the SP720 supply is switched off. If a transient or power surge is provided from the source input to the IN terminal of the SP720, after the V+ has been switched off, forward current will be conducted to the V+/V_{CC} power supply line. Without a power supply to clamp or limit the rising voltage, a power surge on the input line may damage other signal devices common to the V_{CC} power supply. Bypassing the V_{CC} line may not be adequate to protect for large energy surges. The best choice for protection against this type of damage is to add a zener diode clamp to the V_{CC} line. The zener voltage level should be greater than V_{CC} but within the absolute maximum ratings of all devices powered from the V_{CC} supply line.

Power Supply Off Protection, Rise/Fall Speed

To illustrate the active switching of the SP720 and the speed of the SCR for both turn on and turn off, oscilloscope traces were taken for the circuit conditions of Figure 15. A pulse input signal is applied with **NO** supply voltage applied to the SP720. Figure 15 shows the positive and negative pulse conditions to V+ and V- respectively. The trace scales for Figure 15 are 10ns/division horizontal and 1V/division vertical. Input and output pulses are shown on each trace with the smaller pulse being the output. The smaller output trace is due to an offset resulting from the voltage dropped across the SCR in forward conduction. The OUT+ and OUT- pulses quickly respond to the rising edge of the input pulse, following within ~2ns delay from the start of the IN pulse and tracking the input signal. The output falls with approximately the same delay.

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2. L.R. Avery, "Using SCR's as Transient Protection Structures in Integrated Circuits," EOS/ESD Symp. Proc., 1983, Pg. 90 - 96.
3. MIL-STD-883D, 15 Nov 91, Electrostatic Discharge Sensitivity Classification, Method 3015.7, 22 Mar 89.
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6. Harris Semiconductor, SP720, File No. 2791, Electronic Protection Array for ESD and Overvoltage Protection. (16 Lead Plastic IC available in DIP and SOIC packages).
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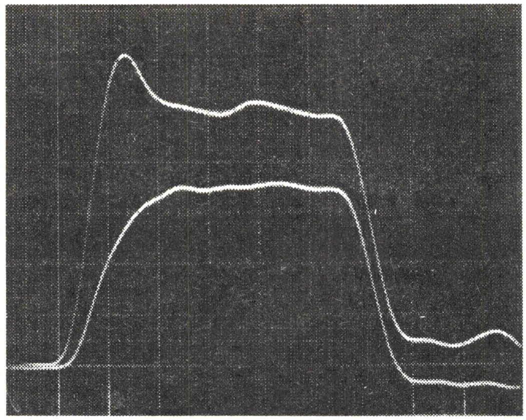
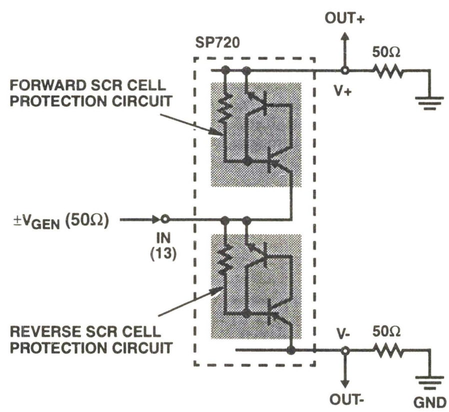
POSITIVE/FORWARD CONDUCTION
HIGH SPEED ON/OFF PULSE (OUT+)





NEGATIVE/REVERSE CONDUCTION
HIGH SPEED ON/OFF PULSE (OUT-)

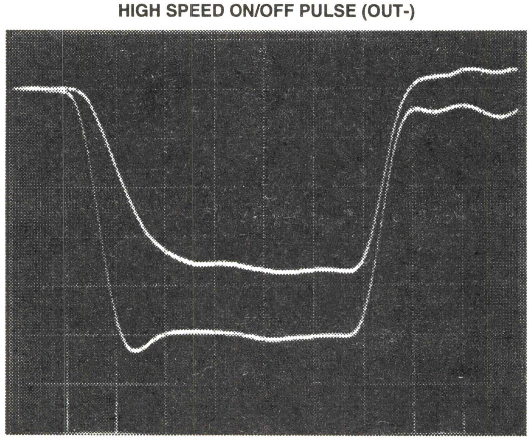


FIGURE 15. SP720 CIRCUIT WITH NO POWER SUPPLY INPUT PULSE TEST WITH 50Ω, (0V TO ±5V) INPUT. THE TRACE SCALES FOR OUT+ AND OUT- ARE 1V/DIV VERTICAL AND 10ns/DIV HORIZONTAL

No. AN9307.2 January 1998

The Connector Pin Varistor for Transient Voltage Protection in Connectors

Authors: Paul McCambridge and Martin Corbett

Introduction

Nonlinear devices have long been used for transient voltage protection and have bee available in conventional package configurations - axial, radial, and power packages (Figure 1) The connector pin varistor represents a new approach to transient suppression by forming the active material into a shape which requires no leads or package (Figure 2) The idea was developed many years ago, but only recently have breakthroughs in the manufacturing process allowed cost-effective production of such devices.

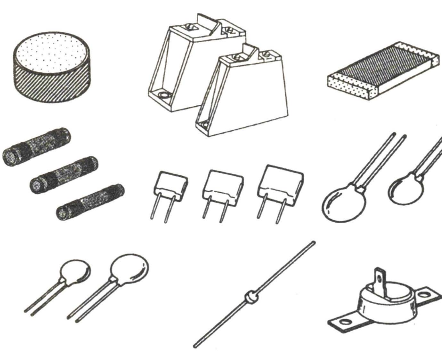


FIGURE 1. CONVENTIONAL PACKAGE CONFIGURATIONS

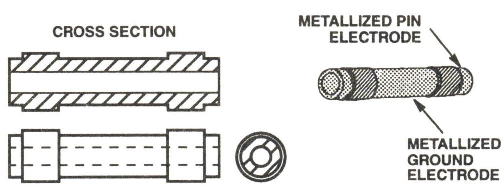


FIGURE 2. TUBULAR VARISTOR (CONNECTOR PIN VARISTOR)

Connector pin varistors are voltage dependent nonlinear semiconducting devices having electrical behavior similar to back-to-back zener diodes. The symmetrical sharp breakdown characteristic enables the varistor to provide excellent transient suppression. As the voltage of a transient rises, the impedance of the varistor changes from a very high value to an extremely low value, limiting the voltage rise across the varistor (Figure 3). The destructive energy is absorbed by circuit impedance and varistor impedance. Energy is converted into hear and, if the varistor is properly rated, no components are harmed.

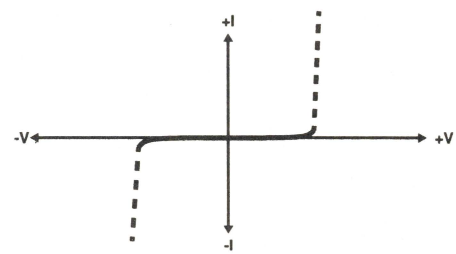
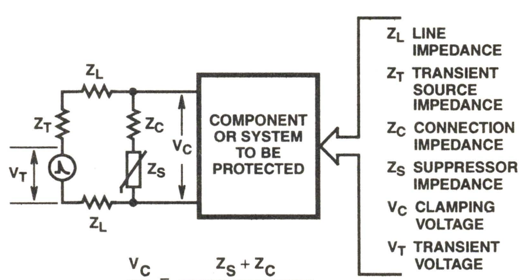


FIGURE 3. VOLTAGE IMPEDANCE CHARACTERISTICS OF A TYPICAL VARISTOR

To obtain the lowest clamping voltage, the impedance of the varistor (Z_S) and the impedance of the varistor leads (Z_C), should be as low as possible, but the impedance of the line (Z_L) and the transient source (Z_T) should be as high as possible (Figure 4). The part of Z_L which is contributed by the ground return also reduces Z_L, but at the same time lifts the ground above true ground and therefore should be small. Unfortunately, the impedance of the transient source (Z_T) cannot be controlled and is unknown in most instances.[1]



$$\frac{V_C}{V_T} = \frac{Z_S + Z_C}{Z_S + Z_C + Z_L + Z_T}$$

FIGURE 4. IMPEDANCE RELATIONSHIP IN A TRANSIENT SUPPRESSOR CIRCUIT

Varistors contain zinc oxide, bismuth, cobalt, manganese and other metal oxides. The structure of the body consists of conductive zinc oxide grains surrounded by a glassy layer (the grain boundary) which provides the 2.5V PN-junction semiconductor characteristics. Figure 5 shows a simplified cross section of the varistor material.

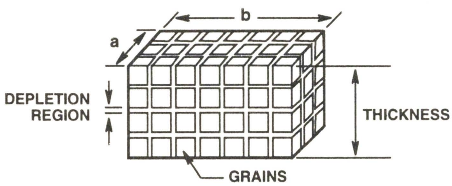


FIGURE 5. SIMPLIFIED MICROSTRUCTURE OF A VARISTOR MATERIAL

The varistor is a multi-junction device with many junctions in parallel and series. Each junction is heat sunk by zinc oxide grains resulting in low junction temperatures and large overload capabilities.

As shown in Figure 5, the more junctions that are connected in series, the higher the voltage rating and as more junctions are connected in parallel, the higher the current rating. Energy rating, on the other hand, is related to both voltage and current and is proportional to the volume of the varistor. In summary:

- Thickness is proportional to voltage
- Area is proportional to current (a x b) or [(d2 • π)/4] or (d • π • length).
- Volume is proportional to energy (area x thickness)

Electrical Characteristics

An electrical model for a varistor is represented by the equivalent circuit shown in Figure 6.

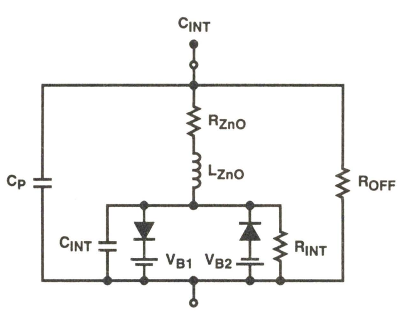


FIGURE 6. VARISTOR EQUIVALENT CIRCUIT

Pulse Response

The pulse response of a varistor is best understood by using the equivalent circuit representation consisting of a pure capacitor (C_P), two batteries, the grain resistance (R_{ZnO}) and the intergrain capacitance (C_{INT}). The off-resistance (R_{OFF}) is not applicable in this discussion.

Due to the varistor capacitance (C_P), the varistor is initially a short circuit to any applied pulse. Varistor breakdown conduction through (V_{B1}) and (V_{B2}), as illustrated in Figure 6 does not occur until this capacitor is charged to the varistor breakdown voltage (V_B). The time is calculated by:

$$t_C = C_P \bullet (V_{B1}/\bar{I}) \text{ or } (2)$$

Where $\bar{I}$ is the average pulse current (capacitor charging current) for $0 \leq t \leq t_C$. The value of the peak current is controlled by $\hat{I} = (di/dt) \bullet C_P$, the source impedance voltage of the transient, and the varistor's dimensions (area proportional to C).

For longer duration pulses $t > t_C$, V_{B1} and V_{B2} will participate on the current conduction process, as the voltage on C_P rises above the breakover voltage (V_B).

Speed of Response

The conduction mechanism is that of a II - VI polycrystalline semiconductor. Conduction occurs rapidly, with no apparent time lag even in the picosecond range.

Figure 7 shows a composite photograph of two voltage traces with and without a varistor connected to a low-inductance high speed pulse generator having a rise time of 500ps. The second trace is not synchronized with the first, but merely superimposed on the oscilloscope screen, showing the instantaneous voltage clamping effect of the varistor. There is no delay or any indication which would justify concern about response time.

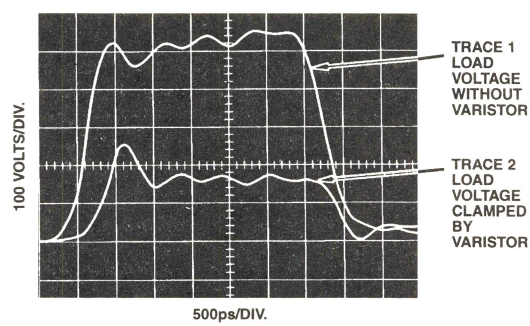


FIGURE 7. RESPONSE OF A VARISTOR TO A FAST RISING PULSE (dv/dt = 1MV/μs)

Using conventional lead-mounted varistors, the inductance of the leads completely masks the fast action of the varistor; therefore, the test results as shown in Figure 7 required the insertion of a small piece of varistor material in a coaxial line to demonstrate the intrinsic varistor response.

Tests made on lead-mounted devices, even with careful attention to minimize lead length, show that the voltage induced through lead inductance contributes substantially to the voltage appearing across the varistor terminals (Figure 8). These undesirable induced voltage are proportional to lead inductance and di/dt and can be positive or negative.

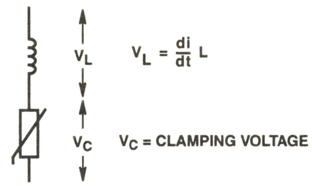


FIGURE 8. THE ELECTRICAL EQUIVALENT OF A LEAD-MOUNTED VARISTOR

Figure 9 shows the positive and negative part of the induced voltage, resulting from a pulse with a rise time of 4ns to a peak current of 2.5A. When the measurement is repeated with a leadless varistor, such as the connector pin varistor, its unique coaxial mounting allows it to become part of the transmission line. This completely eliminates inductive lead effect (Figure 10).

Calculations of the induced voltage (V_L) as a direct result of lead effect for different current rise times provides a better understanding of the di/dt value at which the lead effect become significant. Table 1 is based on an assumption of a current pulse of 10A, 1 inch of lead wire (which translates into approximately 15nH) and rise times ranging from seconds to femtoseconds.

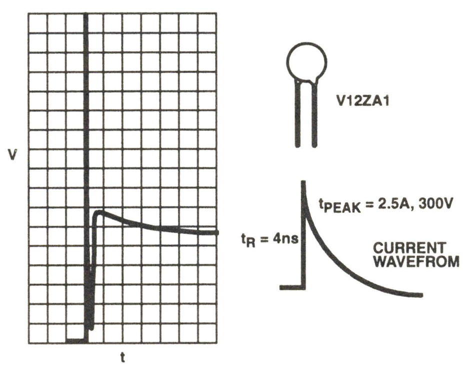


FIGURE 9. EXPONENTIAL PULSE APPLIED TO A RADIAL DEVICE (5V/DIV., 50s/DIV.)

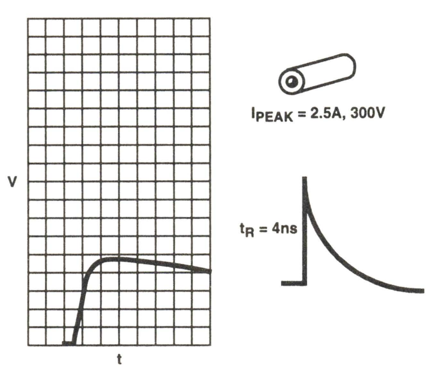


FIGURE 10. EXPONENTIAL PULSE APPLIED TO A PIN-VARISTOR (5V/DIV., 50nS/DIV.)

TABLE 1. INDUCED VOLTAGE (V_L) IN 1 IN. LEADS. PEAK CURRENT 10A, AT DIFFERENT CURRENT RISE TIMES

	TIME	I	L	V_L
1×10^{0}	1 sec.	10A	15nH	150×10^{-9}
1×10^{-3}	1ms	10A	15nH	150×10^{-5}
1×10^{-5}	1μs	10A	15nH	150×10^{-3}
1×10^{-9}	1ns	10A	15nH	150
1×10^{-12}	1ps	10A	15nH	150×10^{-3}
1×10^{-18}	1fs	10A	15nH	150×10^{-6}

Figure 11 illustrates the lead effect even more dramatically for fast rising pulses ranging in rise time from milliseconds to femtoseconds.

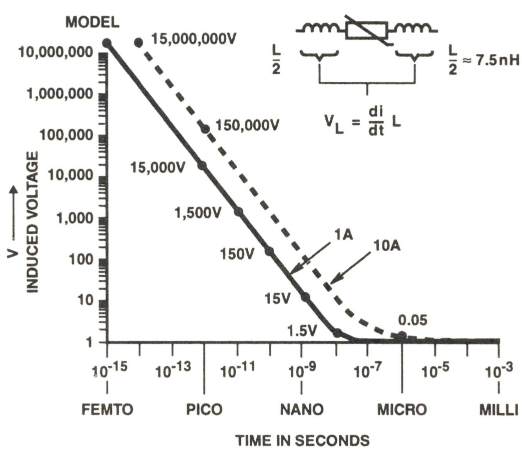


FIGURE 11. LEAD EFFECT OF 1 INCH CONNECTION (L ≈ 15nH)

Temperature Coefficient (Electrical)

The temperature coefficient is usually of little importance. It is most pronounced at low voltage and current levels and decreases to practically zero at the upper end of the V-I characteristics (Figure 12).

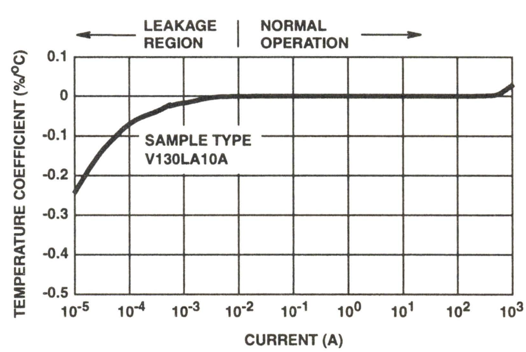


FIGURE 12. TYPICAL TEMPERATURE COEFFICIENT OF VOLTAGE vs CURRENT (-55°C to 125°C)

Connector Pins vs Circuit Board Suppressors

Circuit designers may ask, "Why use connector pin varistors when suppressors could be located on the printed circuit board of the electronic control module (ECM)?" Reasons include saving space and avoiding side effects of circuit board suppressor action.

A simplified schematic of an ECM is illustrated in Figure 13. Suppressors usually would be installed across the power analog and digital signal lines entering the ECM. These would divert surges to ground to avoid upset or damage of the ICs fed by those lines. However, side effects could occur if the suppressors are located internally. The paths of circulating current for diverting surges to ground could be of significant length and impedance. If the suppressor current paths share some impedance, then a surge current in one suppressor could cause a surge voltage on the ground line of another circuit. Also, surges can be coupled from one line to another within the ECM by radiation or by capacitive means. These problems are even more likely with surges that have fast fronts causing high V = Ldi/dt voltages, such as when tubes are activated.

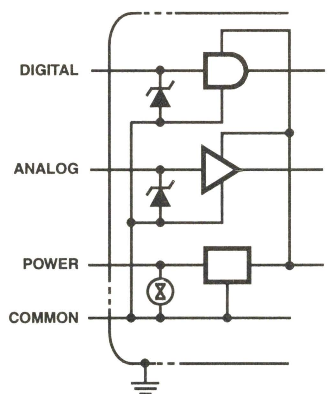


FIGURE 13. CIRCUIT BOARD SUPPRESSOR INSTALLATION

The above concerns are avoided when connector pin varistors are used as shown in Figure 14. Currents then can be diverted directly to a grounding plate within the connector which, in turn, terminates to the exterior of the ECM shielded housing. Surge currents stay outside of the "black box," and sensitive circuits are not exposed to the side effects of suppressor operation. Even if the ICs have on-chip suppressors for ESD protection, or the PC board has local suppressors, the connector pin varistors are desirable because they can divert some of the surge. This permits the local devices, in combination with line impedances and filter chokes, if present, to become secondary protectors. The local surge currents will be less, surge coupling side effects will be reduced, and lower clamping voltages can be attained.

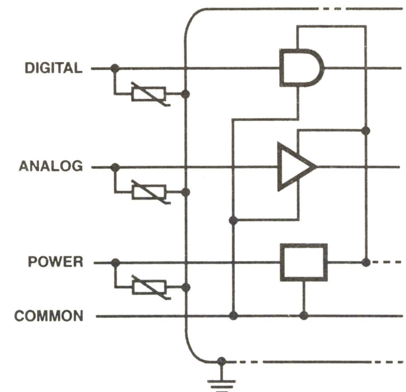


FIGURE 14. CONNECTOR PIN VARISTOR INSTALLATION

Connector Pins vs Zener Diodes

Clamping Voltage

Clamping voltage is an important feature of a transient suppressor. Zener diode type devices have lower clamping voltage than varistors (Figure 15). Because all protective devices are connected in parallel with the device or system to be protected, a lower clamping voltage will apply less stress to the device protected.

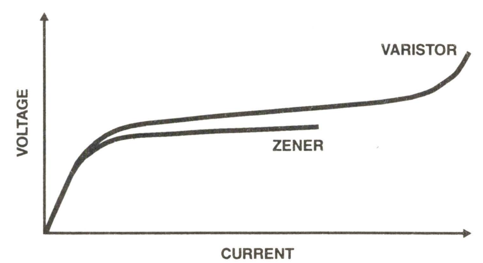


FIGURE 15. CHARACTERISTICS OF ZENER AND VARISTOR

Speeds Compared

Response times of less than 1ps are claimed for zener diodes. For varistors, measurements were made down to 500ps with a voltage rise time (dv/dt) of 1 million volts per microsecond. Another consideration is the lead effect, previously discussed. Both devices are fast enough to respond to any practical requirements, including NEMP type transients.

Leakage Currents

Leakage current and sharpness of the knee are two areas of misconception about the varistor and zener diode devices. Figure 16 shows a zener diode and a varistor, both recommended by their manufacturers for protection of integrated circuits having 5V supply voltages.

The zener diode leakage is about 100 times higher at 5V than the varistor, 200µA versus less than 2µA.

For a leakage current comparison, 25 zener diode devices were measured at 25°C. Only 1 device measured 30mA. The rest were 150mA and more. At elevated temperatures, the comparison is even more favorable to the varistor. The zener diode is specified at 1000mA at 5.5V.

The leakage current of a zener can be reduced by specifying a higher voltage device which would have a lower leakage current, but the price is a higher clamping voltage and the advantage of the zener disappears.

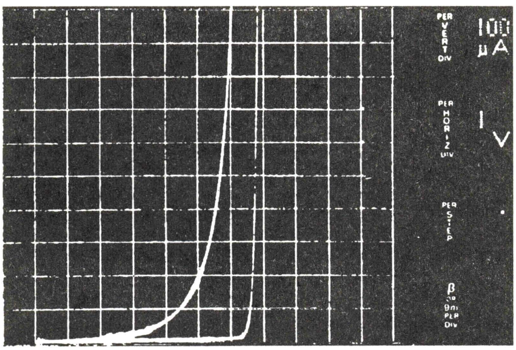


FIGURE 16. CHARACTERISTICS OF A ZENER DIODE (ON LEFT) vs A VARISTOR (ON RIGHT)

Peak Pulse Power

Transient suppressors have to be optimized to absorb large amounts of power or energy in a short time duration: nanoseconds, microseconds or, in some rare instances, milliseconds.

Electrical energy is transformed into heat and has to be distributed instantaneously throughout the device. Transient thermal impedance is much more important than steady-state thermal impedance, as it keeps peak junction temperature to a minimum. In other words, heat should be instantly and evenly distributed throughout the device.

The varistor meets these requirements: an extremely reliable device with large overload capability. Zener diodes on the other hand, transform electrical energy into heat in the depletion region, an extremely small area, resulting in high peak temperature. From there the heat will flow through the silicon and solder joint to the copper. Thermal coefficient mismatch and large temperature differentials can result in an unreliable device for transient suppression.

Figure 17 shows peak pulse power versus pulse width for the varistor and the zener diode, the same devices compared for leakage current.

At 1ms, the two devices are almost the same. At 2µs the varistor is almost 10 times better, 7kW for the zener versus 60kW for the varistor.

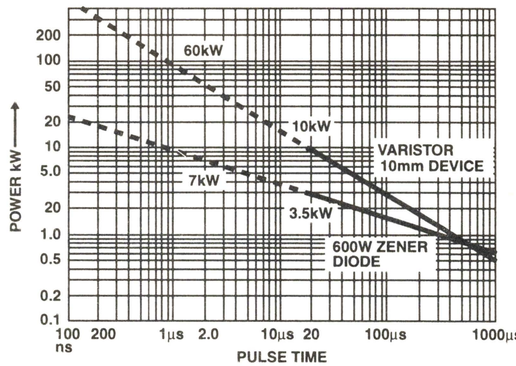


FIGURE 17. PEAK PULSE POWER vs PULSE TIME

Aging

A common misconception is that a varistor's V-I characteristics changes every time energy is absorbed. As illustrated in Figure 18, the V-I characteristic changed on some of the devices, but returned to its original value after applying a second or third pulse. Is this an inversion of the aging process? Time and temperature have very similar effects.

To be conservative, peak pulse limits have been established which, in many cases, have been exceeded manyfold without harm to the device. This does not mean that established limits should be ignored, but rather, viewed in perspective of the definition of a failed device. A failed device shows a ±10 percent change of the V-I characteristic at the 1mA point. Zener diodes, on the other hand, fail suddenly at predictable power and energy levels.

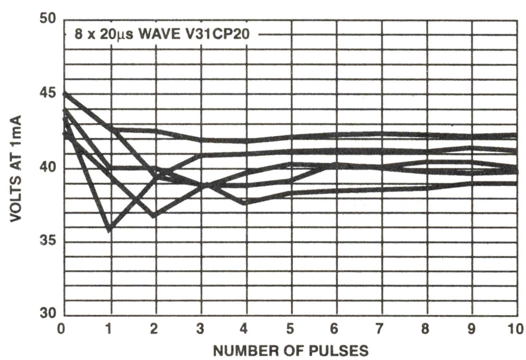


FIGURE 18. 250A PULSE-WITHSTAND CAPABILITIES

Failure Mode

Varistors fail short, but can also explode when energy is excessive, resulting in an open circuit. Because of the large peak pulse capabilities of varistors, these types of failure are quite rare for properly selected devices.

Zeners, on the other hand, can fail either short or open. If the pellet is connected by a wire, it can act as a fuse, disconnecting the device and resulting in an open circuit.

Designers must analyze which failure mode, open or short, is preferred for their circuits.

Should a suppression device fail during a transient, a short-circuit mode is usually preferred, since it will provide a current path bypass and continue to protect the sensitive components. On the other hand, if a device fails open during a transient, the remaining energy ends up in the sensitive components that were supposed to be protected. If the energy is already dissipated, the circuit will now operate without a suppressor and the next transient, or the next few transients, could damage the equipment.

Another consideration is a hybrid approach, making use of the best features, described above, of both types of transient suppressors (Figure 19).

FIGURE 19. HYBRID PROTECTION USING VARISTORS, ZENERS, R AND L

Capacitance

Depending on the application, transient suppressor capacitance can be a very desirable or undesirable feature compared to zener diodes. Varistors have a higher capacitance. In DC circuits, capacitance is desirable: the larger the better. Decoupling capacitors are used on IC supply voltage pins and can in any cases be replaced by varistors, providing both the decoupling and transient voltage clamping functions.

The same is true for filter connectors where the varistor can perform the dual functions of providing both filtering and transient suppression.

There are circuits, however, where capacitance is less desirable, such as high frequency digital or some analog circuits.

As a rule, the source impedance of the signal and the frequency as well as the capacitance of the transient suppressor should be considered (Figure 20).

The current through C_P is a function of dv/dt and the distortion is a function of the signal's source impedance. Each case must be evaluated individually to determine the maximum allowable capacitance.

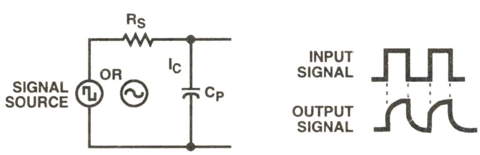


FIGURE 20. SOURCE IMPEDANCE (R_S) AND PARASITIC CAPACITANCE (C_P)

Response to Radiation

For space applications, an extremely important property of a protection device is its response to imposed radiation effects.

Electron Irradiation

Figure 21 represents MOV and zener devices exposed to electron irradiation. The V-I curves, before and after test, are shown. The MOV is virtually unaffected, even at the extremely high dose of 10^8 rads, while the zener shows a dramatic increase in leakage current.

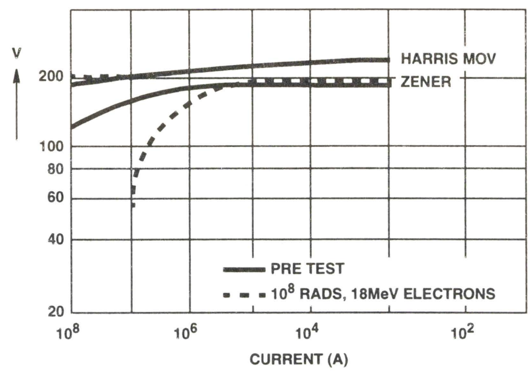


FIGURE 21. RADIATION SENSITIVITY OF MOV AND ZENER DEVICES

Neutron Effects

A second MOV-zener comparison was made with respect to neutron fluence. The selected devices were equal in area.

Figure 22 shows the clamping voltage response of the MOV and the zener to neutron irradiation as high as 10^{15}N/cm^2. In contrast to the large change in the zener, the MOV is unaltered. At higher currents where the MOV's clamping voltage is again unchanged, the zener device clamping voltage increases by as much as 36 percent.

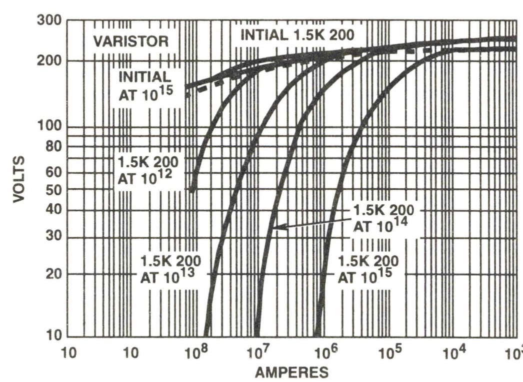


FIGURE 22. VOLTAGE CURRENTS CHARACTERISTIC RESPONSE TO NEUTRON IRRADIATION FOR MOV AND ZENER DIODE DEVICES

Counterclockwise rotation of the V-I characteristics is observed in silicon devices at high neutron irradiation levels. In other words, leakage increases at low current levels and clamping voltage increases at higher current levels.

The solid and open circles for a given fluence represent the high and low breakdown currents for the sample of devices tested. A marked decrease in current (or energy) handling capability with increased neutron fluence should be noted.

The failure threshold level of silicon semiconductor junctions is further reduced when high or rapidly increasing currents are applied. Junctions develop hot spots, which enlarge until a short occurs if current is not limited or quickly removed.

The characteristic voltage current relationship of a PN-Junction is shown in Figure 23.

At low reverse voltage, the device will conduct very little current (the saturation current). At higher reverse voltage V_{BO} (breakdown voltage), the current increases rapidly as the electrons are either pulled by the electric field (zener effect) or knocked out by other electrons (avalanching). A further increase in voltage causes the device to exhibit a negative resistance characteristic leading to a secondary breakdown. This manifests itself through the formation of hotspots, and irreversible damage decreases under neutron irradiation for zeners, but not for zinc oxide varistors.

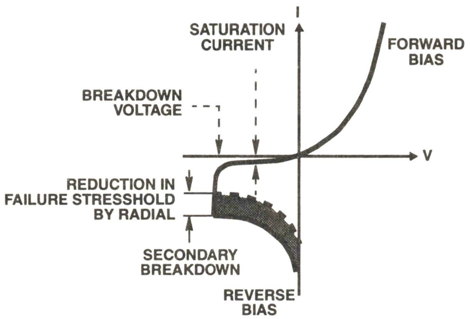


FIGURE 23. VOLTAGE CURRENTS CHARACTERISTIC OF PN-JUNCTION

Gamma Radiation[7]

Radiation damage studies were performed on specified varistors. Emission spectra and V-I characteristics were collected before and after irradiation with 10^6 rads Co^{60} gamma radiation. Both show no change, within experimental error, after irradiation.

Mechanical Strength

After sintering, the varistor becomes a strong, rugged ceramic material. As with all ceramic materials, it has high compressive strength and lower tensile or shear strength. An experiment was performed to demonstrate the strength of the varistor material when used in the tubular form. Results are shown in Table 2. P1 and P2 represent maximum pressures applied before fracture. Directions of applied stresses are shown in Figure 24.

TABLE 2. VARISTOR MATERIAL STRENGTH

PART SIZE	P1	P2
20A	100lbs	30lbs
20B	100lbs	14lbs
22B	100lbs	14lbs

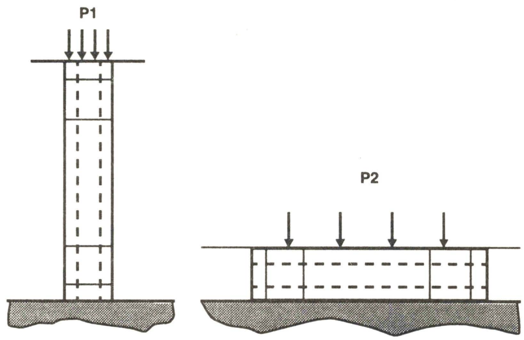


FIGURE 24. APPLIED STRESSES

Conclusions

Connector pin varistors provide a unique way to install surge protection in electronic systems without the bulkiness of some approaches. The tubular form of this varistor gives a relatively large area for conducting surge current, with an inherent mass for dissipating electrical heat energy. The rugged body physically resembles passive components; but, because it is a semiconductor device, response time is very fast. The leadless form reduces the voltage overshoot that can be caused by lead inductance. Also, the device has a high degree of inherent radiation hardness. Connector pin varistors divert surge currents to the outside surface of the "black box" housing, not to printed board runs feeding sensitive circuits, thereby helping to avoid or reduce surge coupling side effects.

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Harris Semiconductor

APP NOTE

No. AN9308.2 January 1998

Harris Suppression Products

AC Line Voltage Transients and Their Suppression

Author: Martin P. Corbett

Introduction

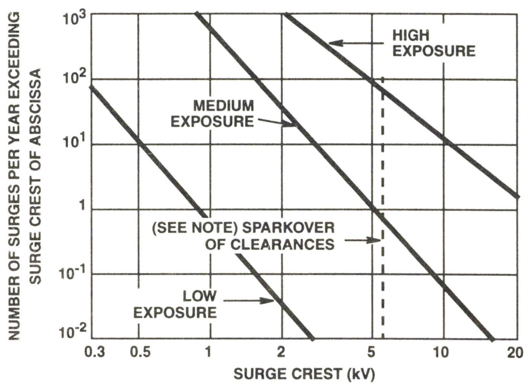
The increasing usage of sensitive solid state devices in modem electrical systems, particularly computers, communications systems and military equipment, has given rise to concerns about system reliability. These concerns stem from the fact that the solid state devices are very susceptible to stray electrical transients which may be present in the distribution system.

The initial use of semiconductor devices resulted in a number of unexplained failures. Investigation into these failures revealed that they were caused by transients, which were present In many different forms in the system. Transients in an electrical circuit result from tile sudden release of previously stored energy. The severity of, and hence the damage caused by transients depends on their frequency of occurrence, the peak transient currents and voltages present and their waveshapes.

In order to adequately protect sensitive electrical systems, thereby assuring reliable operation, transient voltage suppression must be part of the initial design process and not simply included as an afterthought. To ensure effective transient suppression, the device chosen must have the capability to dissipate the impulse energy of the transient at a sufficiently low voltage so that the capabilities of the circuit being protected are not affected. The most successful type of suppression device used is the metal oxide varistor. Other devices which are also used are the zener diode and the gas-tube arrestor.

The Transient Environment

The occurrence rate of surges varies over wide limits, depending on the particular power system. These transients are difficult to deal with, due to their random occurrences and the problems in defining their amplitude, duration and energy content. Data collected from many independent sources have led to the data shown in Figure 1. This prediction shows with certainty only a relative frequency of occurrence, while the absolute number of occurrences can be described only in terms of low, medium or high exposure. This data was taken from unprotected circuits with no surge suppression devices.



NOTE: In some locations, sparkover of clearances may limit the overvoltages.

FIGURE 1. RATE OF SURGE OCCURRENCES vs VOLTAGE LEVEL AT UNPROTECTED LOCATIONS

The low exposure portion of the graph Is derived from data collected in geographical areas known for low lightning activity, with little load switching activity. Medium exposure systems are geographical areas known for high lightning activity, with frequent and severe switching transients. High exposure areas are rare, but real systems, supplied by long overhead lines and subject to reflections at line ends, where the characteristics of the installation produce high sparkover levels of the clearances.

Investigations into the two most common exposure levels, low and medium, have shown that the majority of surges occurring here can be represented by typical waveform shapes (per ANSI/IEEE C62.41-1980). The majority of surges which occur in indoor low voltage power systems can be modeled to an oscillatory waveform (see Figure 2). A surge impinging on the system excites the natural resonant frequencies of the conductor system. As a result, not only are the surges oscillatory but surges may have different amplitudes and waveshapes at different locations in the system. These oscillatory frequencies range from 5kHz to 500kHz with 100kHz being a realistic choice.

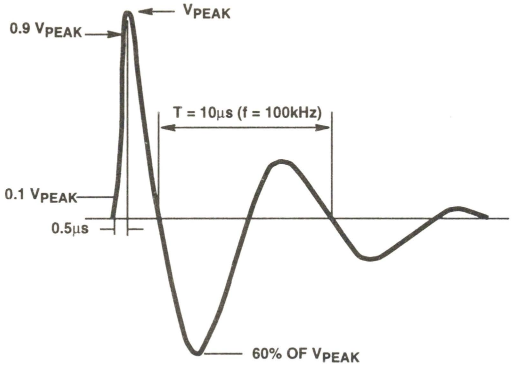


FIGURE 2. 0.5µs - 100kHz RING WAVE (OPEN CIRCUIT VOLTAGE)

In outdoor situations the surge waveforms recorded have been categorized by virtue of the energy content associated with them. These waveshapes involve greater energy than those associated with the indoor environment. These waveforms were found to be unidirectional in nature (see Figure 3).

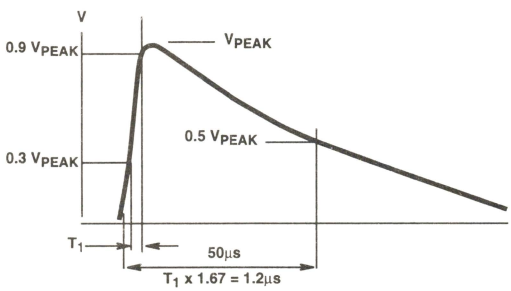


FIGURE 3A. OPEN-CIRCUIT WAVEFORM

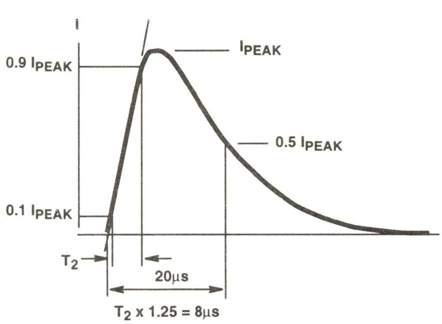


FIGURE 3B. DISCHARGE CURRENT WAVEFORM

FIGURE 3. UNIDIRECTIONAL WAVESHAPES (OUTDOOR LOCATIONS)

Transient Energy and Source Impedance

Some transients may be intentionally created in the circuit due to inductive load switching, commutation voltage spikes, etc. These transients are easy to suppress since their energy content is known. It is the transients which are generated external to the circuit and coupled into it which cause problems. These can be caused by the discharge of electromagnetic energy, e.g., lightning or electrostatic discharge. These transients are more difficult to identify, measure and suppress. Regardless of their source, transients have one thing in common - they are destructive. The destruction potential of transients is defined by their peak voltage, the follow-on current and the time duration of the current flow, that is:

$$E = \int_0^{\tau} Vc(t) \bullet I(t)\, dt$$

where:

E = Transient energy

I = Peak transient current

Vc = Resulting clamping voltage

t = Time

τ = Impulse duration of the transient

It should be noted that considering the very small possibilities of a direct lightning hit it may be deemed economically unfeasible to protect against such transients. However, to protect against transients generated by line switching, ESD, EMP and other such causes is essential, and if ignored will lead to expensive component and/or system losses.

The energy contained in a transient will be divided between the transient suppressor and the line upon which it is travelling in a way which is determined by their two impedances. It is essential to make a realistic assumption of the transient's source impedance in order to ensure that the device selected for protection has adequate surge handling capability. In a gas-tube arrestor, the low impedance of the arc after sparkover forces most of the energy to be dissipated elsewhere - for instance in a power-follow current-limiting resistor that has to be added in series with the gap. This is one of tile disadvantages of the gas-tube arrestor. A voltage clamping suppressor (e.g., a metal oxide varistor) must be capable of absorbing a large amount of transient surge energy. Its clamping action does not involve the power-follow energy resulting from the short-circuit action of the gap.

The degree to which source impedance is important depends largely on the type of suppressor used. The surge suppressor must be able to handle the current passed through them by the surge source. An assumption of too high an impedance (when testing the suppressor) may not subject it to sufficient stresses, while the assumption of too low an impedance may subject it to unrealistically large stress; there is a trade off between the size/cost of the suppressor and the amount of protection required.

In a building, the source impedance and the load impedance increases from the outside to locations well within the inside of the building, i.e., as one gets further from the service entrance, the impedance increases. Since the wire in a structure does not provide much attention, the open circuit voltages show little variation. Figure 4 illustrates the application of three categories to the wiring of a power system.

These three categories represent the majority of locations from the electrical service entrance to the most remote wall outlet. Table 1 is intended as an aid in the selection of surge suppressors devices, since it is very difficult to select a specific value of source impedance.

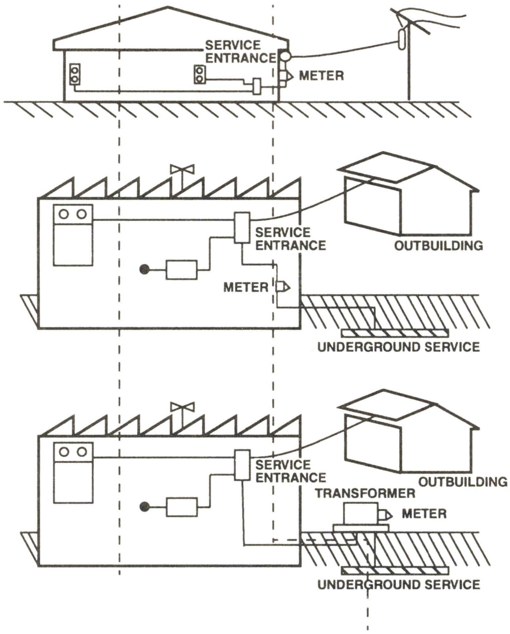
Category A covers outlets and long branch circuits over 30 feet from category B and those over 60 feet from category C. Category B is for major feeders and short branch circuits from the electrical entrance. Examples at this location are bus and feeder systems in industrial plants, distribution panel devices, and lightning systems in commercial buildings. Category C applies to outdoor locations and the electrical service entrance. It covers the service drop from pole to building entrance, the run between meter and the distribution panel, the overhead line to detached buildings and underground lines to well pumps.

TABLE 1. SURGE VOLTAGES AND CURRENTS DEEMED TO REPRESENT THE INDOOR ENVIRONMENT AND RECOMMENDED FOR USE IN DESIGNING PROTECTIVE SYSTEMS

LOCATION CATEGORY CENTER	COMPARABLE TO IEC 664 CATEGORY	IMPULSE		TYPE OF SPECIMEN OR LOAD CIRCUIT CIRCUIT	ENERGY (JOULES) DEPOSITED IN A SUPPRESSOR WITH CLAMPING VOLTAGE	
		WAVEFORM	MEDIUM EXPOSURE AMPLITUDE		500V	1000V
					(120V Sys.)	(240V Sys.)
A. Long branch circuits and outlets	II	0.5µs - 100kHz	6kV	High Impedance (Note 1)	-	-
			200A	Low Impedance (Note 2)	0.8	1.6
B. Major feeders short branch circuits, and load center	III	1.2/50µs	6kV	High Impedance (Note 1)	-	-
		8/20µs	3kA	Low Impedance (Note 2)	40	80
		0.5µs - 100kHz	6kV	High Impedance (Note 1)	-	-
			500A	Low Impedance	2	4

NOTES:

1. For high-impedance test specimens or load circuits, the voltage shown represents the surge voltage. In making simulation tests, use that value for the open-circuit voltage of the test generator.
2. For low-impedance test specimens or load circuits, the current shown represents the discharge current of the surge (not the short-circuit current of the power system). In making simulation tests, use that current for the short-circuit current of the test generator.
3. Other suppressors which have different clamping voltages would receive different energy levels.



A	B	C
Outlets and long branch circuits. All outlets at more than 10m (30ft.) from Category B. All outlets at more than 20m (60ft.) from Category C.	Feeders and short branch circuits Distribution Panel Devices Bus and feeder in industrial plants Heavy appliance outlets with "short" connections to service entrance Lighting systems in large buildings	Outside and service entrance Service drop from pole to building. Run between meter and panel. Overhead line to detached building. Underground line to well pump.

FIGURE 4. LOCATION CATEGORIES

Transient Suppression

The best type of transient suppressor to use depends on the intended application, bearing in mind that in some cases both primary and secondary protection may be required. It is the function of tile transient suppressor to, in one way or another, limit the maximum instantaneous voltage that can develop across the protected load. The choice depends on several factors, but the decision is ultimately a trade-off between the cost of the suppressor and the amount of protection needed.

The time required for a transient suppressor to begin functioning is extremely important when it is used to protect sensitive components. If the suppressor is slow acting and a fast-rise transient spike appears on the system the voltage across the protected load can rise to damaging levels before suppression begins. On AC power lines the best type of suppression to use is a metal oxide varistor. Other devices occasionally used are the zener diode and the gas-tube arrestor.

Gas-Tube Arresters

This is a suppression device which finds most of its applications in telecommunication systems. It is made of two metallic conductors usually separated by 10mils to 15mils encapsulated in a glass envelope. This glass envelope is pressurized and contains a number of different gases. Types specifically designed for AC line operation are available and offer high surge current ratings.

Zener Diodes

One type of clamp-action device used in transient suppression is the zener diode. When a voltage of sufficient amplitude is applied in the reverse direction, the zener diode is said to break down, and will conduct current in this direction. This phenomenon is called avalanche. The voltage appearing across the diode is therefore called the reverse avalanche or zener voltage.

When a transient propagates along the line with a voltage exceeding the reverse-based voltage rating of the diode, the

diode will conduct and the transient will be clamped at the zener voltage. This clamping voltage is lower than that of an equivalent varistor. Some manufacturers have claimed that the response time of a zener diode is 1ps to 2ps. In practice, the speed of response is greatly determined by the parasitic inductance of the package and the manner in which the device is connected via its leads. Although zener diodes can provide transient protection, they cannot survive significant instantaneous power surges. Larger diodes can be used to increase the power rating, but this is only at the expense of increased costs. Also, the maximum tolerable surge current for a zener diode in reverse breakdown is small when compared to tolerable surge currents for varistors. Due to the fact that there is only the p-n junction in a zener diode, it will need to have some additional heat sinking in order to facilitate the rapid build-up of heat which occurs in the junction after it has encountered a transient.

Metal Oxide Varistor

As the name suggests, metal oxide varistors (MOV) are variable resistors. Unlike a potentiometer, which is manually adjusted, the resistance of a varistor varies automatically in response to changes in voltages appearing across it. Varistors are a monolithic device consisting of many grains of zinc oxide, mixed with other materials, and compressed into a single form. The boundaries between individual grains can be equated to p-n junctions with the entire mass represented as a series-parallel diode network.

When a MOV is biased, some grains are forward biased and some are reverse biased. As the voltage is increased, a growing number of the reversed biased grains exhibit reverse avalanche and begin to conduct. Through careful control in manufacturing, most of the nonconducting p-n junctions can be made to avalanche at the same voltage. MOVs respond to changes in voltages almost instantaneously. The actual reaction time of a given MOV depends on physical characteristics of the MOV and the wave shape of the current pulse driven through it by the voltage spike. Experimental work has shown the response time to be in the 500 picosecond range.

One misconception about varistors is that they are slow to respond to rapid rise transients. This "slow" response is due to parasitic inductance in the package and leads when the varistor is not connected with minimal lead length. If due consideration is given to these effects in its installation, the MOV will be more than capable of suppressing any voltage transients found in the low voltage AC power system.

The MOV has many advantages over the zener diode, the greatest of which is its ability to handle transients of much larger energy content. Because it consists of many p-n junctions, power is dissipated throughout its entire bulk, and unlike the zener, no single hot spot will develop. Another advantage of the MOV is its ability to survive much higher instantaneous power.

Summary

When designing circuits of the complex nature seen in todays electrical environment, the initial design must incorporate some form of transient voltage surge suppression. The expense of incorporating a surge protection device in a system is very low when compared with the cost of equipment downtime, maintenance and lost productivity which may result as a consequence of not having protection. When selecting surge suppressors for retrofit to an existing design, one important point to remember is that the location of the load to be protected relative to the service entrance is as important as the transient entrance which may be present in an overvoltage situation.

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APP NOTE

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Harris Suppression Products

Surge Suppression Technologies for AC Mains Compared (MOVs, SADs, Gas Tubes, Filters and Transformers)

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Synopsis

Protection on the low voltage AC mains system from transient overvoltages is now a fundamental power quality concern. The use of correctly selected and installed surge protectors have a long and proven history of successful field performance. The expected transient environment is addressed, along with various types of surge suppression components are compared to MOVs.

Introduction

The increasing use of semiconductors and other solid state components in modern electrical systems has resulted in a growing awareness about system reliability. This is a consequence of the fact that solid state devices are very susceptible to stray electrical transients which may be present in the low voltage AC distribution system. The initial use of semiconductors resulted in a large number of unexplained failures. Investigation into these failures revealed that they were caused by a number of diverse overvoltage conditions which were present in the distribution system. Transient voltages result from the sudden release of previously stored energy from overstress conditions such as lightning, inductive load switching, electromagnetic pulses or electrostatic discharges. The severity of, and hence the damage caused, by the transient depends on their frequency of occurrence, their peak values and their waveshapes.

Electrical overvoltages on AC mains can cause either permanent deterioration, or temporary malfunctions in electronic components and systems. Protection from transients can be obtained by using specially designed components which will, either limit the magnitude of the transient using a large series impedance or by diverting the transient using a low value shunt impedance.

A prudent designer will consider the need for transient protection in the early stages of the design. Too many times it has been necessary to retrofit existing equipment with transient suppressors. This is expensive in terms of field failures, customer downtime and potential loss of business. In some systems retrofitting becomes cumbersome, as the space required was not planned for in the initial design. The device selected as the system protector must have the capability to dissipate the impulse energy of the transient at a sufficiently low voltage so that the capabilities of the system being protected are not affected.

Problem Definition (The Transient Environment) [1, 2, 3, 4]

Primarily the problem is that of the enigmatic presence of overvoltage surges, above the normal system voltage. Overvoltages are sometimes explainable or sometimes they just mysteriously appear in the electrical system; they take the form of disturbances, notches, swells, sags, brownouts, outages or combinations of the above and are generically known as transients. A common result of encountering these overvoltages is the early failure of semiconductor components and other sensitive electrical components. An equally serious effect is the loss of control in solid-state logic systems that may think surges are legitimate signals and thus endeavor to react to them.

Numerous studies have been performed which indicate that the causes of the surges in an electrical system can be attributed to one of the following causes:

- Lightning
- Opening or closing of switch contacts under load
- Propagation of surges through transformers
- Severe load changes in adjacent systems
- Power line fluctuations and pulses
- Short circuits or blown fuses

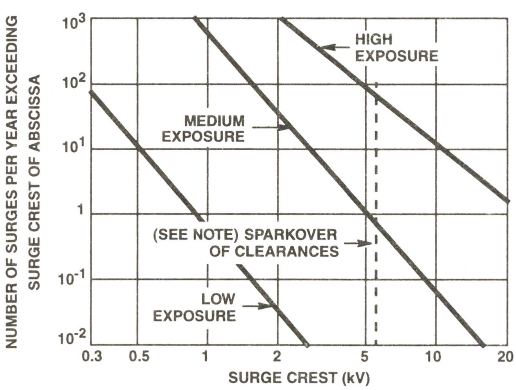
The power system is made up of a large network of cross connected transmission lines. This power system is often interfered with by transients originating from one of the aforementioned sources.

Transients caused by lightning can inject very high currents into the system. These lightning strikes, usually to the primary transmission lines, may result in coupling to the secondary line through mutual inductive or capacitive coupling. Even a lightning hit that misses the line can induce substantial voltage onto the primary conductors, triggering lightning arresters and creating transients. Man-made switching transients can be of a lesser, but more frequent threat. Switching of the power grid can cause transients which may damage down line equipment. The use of thyristors in switching circuits or power control can also create such transients.

Studies and laboratory investigation of residential and industrial low voltage AC power systems have shown that the amplitude of the transient is proportional to the rate of its occurrence, i.e. lower magnitude transients occur most often. Governing standards bodies, in particular IEEE and ANSI, have established a document which gives practical guidelines of the transient environment one may expect to encounter in a low voltage AC power system. This document is called the ANSI/IEEE standard C62.41 and was developed in 1980. Since its inception, more accurate information has become available on the transient environment and this has led to the generation of an updated standard, which should be available later this year.

Rate of Occurrence

The rate of occurrence of surges varies quite a lot and is dependent upon the particular power system. Rate is related to the level of surges and low magnitude surges are more common than high level surges. Data from many sources have shown that surges of 1kV or less are relatively common, while surges of 3kV are more rare. The data generated from the studies was used to generate the curve shown in Figure 1. This curve shows with certainty only a relative frequency of occurrence, while the absolute number of occurrences can be described in terms of "low exposure", "medium exposure" and "high exposure".



NOTE: In some locations, sparkover of clearances may limit the overvoltages.

FIGURE 1. RATE OF SURGE OCCURRENCES vs VOLTAGE LEVEL AT UNPROTECTED LOCATIONS

An area described as a "low exposure" area would have very little lightning activity and few switching loads on the AC power system. A "medium exposure" area is known for high lightning activity, with frequent and severe switching transients. When designing equipment for the global environment it is expedient that it be, at least, designed for use in an area with "medium exposure" transient occurrences. "High exposure" areas are rare but real systems supplied by long overhead transmission lines and subject to reflections at line ends, where the characteristics of the installation produce high sparkover levels of the clearances.

All indoor low-voltage AC power systems have an inherent protection system built into the wiring of the building. Wiring systems used in 120V - 240V systems have a natural spark-over level of 6000V. This 6kV level has therefore been selected as the worst case cutoff for the occurrence of transients in the indoor power system. The transient generated by spark-over creates a high energy, low impedance pulse. The further away from the source of the transient the protected equipment is located, the more the energy is absorbed in the wiring impedance and the more the equipment is protected. This, therefore, allows different size suppressors to be used at different locations in the system.

Representative Transients

Table 1 reflects the surge voltages and currents deemed to represent the indoor transient environment in a low-voltage AC power system. When deciding on the type of device to use as a transient voltage surge suppressor, it is recommended that the device selected have, as a minimum, the capability to handle the conditions called out in location Category A of Table 1. The optimum device would preferably have a minimum capability of surviving the transient occurrences called out in location Category B.

TABLE 1. SURGE VOLTAGES AND CURRENTS DEEMED TO REPRESENT THE INDOOR ENVIRONMENT

LOCATION CATEGORY		IMPULSE	
		WAVEFORM	MEDIUM EXPOSURE
A	Long Branch Circuits and Outlets	0.5µs 100kHz	6kV 200A
B	Major Feeders and Short Branch Circuits	1.2/50µs 8/20µs	6kV 3kA
		0.5µs 100kHz	6kV 500A

The investigation into the indoor low voltage system revealed that location Category A encounters transients with oscillatory waveshapes with frequency ranges from 5kHz to more than 500kHz; the 100kHz being deemed most common (Figure 2). Surges recorded at the service entrance, location Category B, are both oscillatory and unidirectional in nature. The typical "lightning surge" has been established as 1.2/50µs voltage wave and 8/20µs current wave (Figure 3).

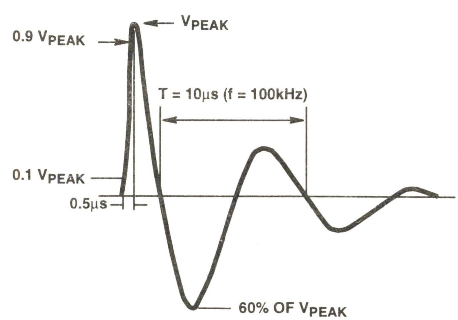


FIGURE 2. 0.5µs - 100kHz RING WAVE (OPEN CIRCUIT VOLTAGE)

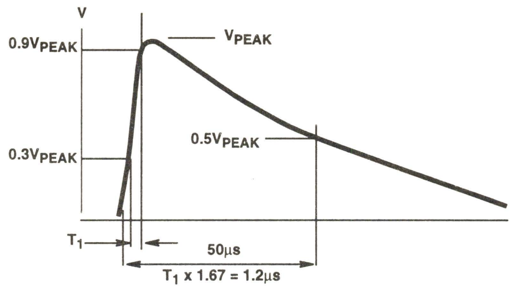


FIGURE 3A. OPEN-CIRCUIT WAVEFORM

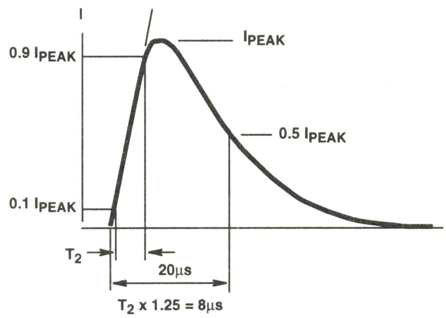


FIGURE 3B. DISCHARGE CURRENT WAVEFORM

FIGURE 3. UNIDIRECTIONAL WAVESHAPES (OUTDOOR LOCATIONS)

Transient Protection

Once it has been decided to include transient suppression in the design of equipment, the next stage in the process is to decide on what protection technology to use and on how to use it. The transient suppressor selected must be able to suppress surges to levels which are below the failure threshold of the equipment being protected, and the suppressor must survive a definite number of worst case transients. When comparing the various devices available considerations must be given to characteristics such as protection levels required, component survivability, cost, and size.

There are a number of different technologies available for use as a transient suppressor in the low voltage AC mains system. Generally speaking, these can be grouped into two major categories of suppressors: a) those that attenuate transients, thus preventing their propagation into the sensitive circuit; and b) those that divert transients away from sensitive loads and so limit the residual voltage.

Attenuating a transient - that is, keeping it from propagating away from its source or keeping it from impinging on a sensitive load - is accomplished with by placing either filters or isolating transformers in series within a circuit. The *isolator* attenuates the transient (high frequency) and allows the signal or power flow (low frequency) to continue undisturbed.

Diverting the transient can be accomplished with a crowbar type device or with a voltage clamping device. *Crowbar* device types involve a switching action, either the breakdown of a gas between electrodes or the turn on of a thyristor. After switching on, they offer a very low impedance path which diverts the transient away form the parallel-connected load. *Clamping* devices have a varying impedance which depends, either, on the current flowing through the device or on the voltage across the terminals. These devices exhibit a nonlinear impedance characteristic. The variation of the impedance is monotonic; that is, it does not contain discontinuities in contrast to the crowbar device, which exhibits a turn on action.

Filters

The installation of a filter in series with the equipment seems an obvious solution to overvoltage conditions. The impedance of a low pass filter, e.g. a capacitor, forms a voltage divider with the source impedance. As the frequency components of a transient are several orders of magnitude above the power frequency of the AC circuit, the inclusion of the filter will result in attenuation of the transient at high frequencies. Unfortunately, this simple approach may have some undesirable side affects; a) unwanted resonances with inductive components located elsewhere in the system leading to high voltage peaks, b) high inrush currents during switching and c) excessive reactive load on the power system voltage. These undesirable effects can be reduced by adding a series resistor, hence the popular use of RC snubber networks. However, the price of the added resistance is less effective clamping.

There is a fundamental limitation to the use of a filter for transient suppression. Filter components have a response which is a linear function of current. This is a big disadvantage in a situation where the source of the transient is unknown and it is necessary to assume a source impedance or an open-circuit voltage. If the assumption of the characteristics of the impinging transient are incorrect the consequences for a linear suppressor is dramatic. A slight change in the source impedance can result in a disproportionately increase in clamping voltage[6].

Isolation Transformers

Isolation transformers generally consist of a primary and secondary windings with an electrostatic shield between the windings. The isolation transformer is placed between the source and the equipment requiring protection. As its name suggests, there is no conduction path between the primary and secondary windings. A widely held belief is that "isolation transformers attenuate voltage spikes" and "that transients do not pass through the windings of the transformer". When properly applied, the isolation transformers is useful to break ground loops, i.e. block common-mode voltages.

Unfortunately, a simple isolation transformer provides no differential-mode attenuation[7]. Thus, a differential-mode transient will be transmitted through the windings of the device. Also, an isolation transformer will not provide any voltage regulation.

Spark Gaps and Gas Tubes

Spark gap suppression is a crowbar suppression technology. During an overvoltage condition, a crowbar device changes from being an insulator to an almost ideal conductor. Crowbars suppress transients by brute force, (they have the effect of dropping a metal crowbar across the system). The main type of crowbar device is the gas tube surge arrester.

The original offering in the spark gap surge suppression family was a carbon blocks. The carbon block suppressor used the principle of a voltage arcing across an air gap. The air gap breaks down at approximately 150V per thousands of an inch. The minimum size gap was used to provide the lowest level of protection without disturbing regular system operation. When a transient overvoltage occurred in the system, the air gap in the carbon block would ionize and break down. The breakdown of the gap forms a very low impedance path to ground thus diverting the surge away from the equipment. As soon as the overvoltage condition was removed, the air gap is restored and system operation is continued.

The disadvantage of carbon block spark gap technology was that short duration pulses “pitted” the surface of the carbon blocks, thus removing small pieces of the face material. This material builds up after a number of surges, eventually causing a permanently shortened gap resulting in the need for protector replacement. This had a very adverse effect on the maintenance and replacement costs of the protection circuit. Another disadvantage of this technology was the difficulty in exactly controlling the breakdown characteristics over a wide variety of operating conditions.

In an effort to overcome the disadvantages of the carbon block, a sealed spark gap was developed which uses an inert gas in a sealed ceramic envelope. This technology is known as a gas tube surge arrester. In a non conducting mode the impedance of the gas is in the gigiohms region. The gas is set to ionize at a predetermined voltage and offers an extremely low impedance path to ground. Once the overvoltage condition is removed the gas deionizes and the circuit restores itself to its normal operating condition.

The gas tube arrester is an inherently bidirectional device and is comprised of either two or three electrodes lying opposite each other in the sealed chamber. When the voltage across the arrester terminals exceeds a certain limit, known as the firing or breakdown voltage, it triggers an electric arc. This arc limits the voltages applied to the connected equipment. Gas tubes have typical DC firing voltages between 150V and 1000V. They have the smallest shunt resistance of all nonlinear transient suppressors, typically in the milliohm range. Their capacitance is low, between 1pF and 5pF, and they are commonly found in high frequency transmission applications, such as telephone systems. Another advantage of this technology is its ability to handle large currents (up to 20kA).

In applications where there is a normal operating voltage, as in the AC mains, there is a possibility that the gas tube will not reset itself once it has fired and suppressed the transient. This condition is known as follow on current and is defined by ANSI “as the current that passes through a device from the connected power source following the passage of discharge current”. Follow on current will maintain conduction of the ionized gas after the transient has disappeared and the concern is that the follow on current may not clear itself at a natural current zero. A gas tube specifically designed for AC line operation should be used in this type of application.

Silicon Avalanche Diodes

Although rarely used on AC mains application, due to their very low transient surge capability, silicon avalanche diodes are an excellent surge suppressor in low voltage DC applications. Avalanche diodes are designed with a wider junction than a standard zener diode. This wide junction gives them a greater ability than a zener to dissipate energy. Avalanche diodes offer the tightest clamping voltage of available devices. When a voltage greater than the device breakdown is applied, the diode will conduct in the reverse direction.

A peak pulse power rating is usually given on diode datasheets. Common values are 600W and 1500W. This peak pulse power is the product of the maximum peak pulse current, I_{PP}, and the maximum clamping voltage, V_C, at a current of I_{PP} during a 10/1000μs transient duration. Use of peak power ratings may be confusing when transients of other than 10/1000μs are to be considered. A maximum energy rating for non-repetitive, short duration transients, similar to that supplied with MOVs, may be of more benefit to design engineers.

The V-I characteristics are the best features of the avalanche diode. Low voltage devices look extremely good. The avalanche diodes has an excellent clamping voltage capability, but only over a small range of current (1 decade). The biggest disadvantage to using the avalanche diode as a transient suppressor on an AC mains line is its low peak current handling capability. Due to their being, at most, only two P-N junctions in a device their is very little material available for the dissipation of the peak power generated during high energy pulses.

Metal Oxide Varistor (MOV) [6]

A metal oxide varistor (MOV) is a nonlinear device which has the property of maintaining a relatively small voltage change across its terminals while a disproportionately large surge current flows through it. This nonlinear action allows the MOV to divert the current of a surge when connected in parallel across a line and hold the voltage to a value that protects the equipment connected to that line. Since the voltage across the MOV is held at some level higher than the normal line voltage while surge current flows, there is energy deposited in the varistor during its surge diversion function.

The basic conduction mechanism of a MOV results from semiconductor junctions (P-N junctions) at the boundaries of the zinc oxide grains. A MOV is a multi junction device with millions of grains acting as a series-parallel combination between the electrical terminals. The voltage drop across a single grain in nearly constant and is independent of grain size.

The material of a metal oxide varistor is primarily zinc oxide with small additions of bismuth, cobalt, manganese and other metal oxides. The structure of the body consists of a matrix of conductive zinc oxide grains separated by grain boundaries, which provide the P-N junction semiconductor characteristics. When the MOV is exposed to surges, the zinc oxide exhibits a "bulk action" characteristic permitting it to conduct large amounts of current without damage. The bulk action is easily explained by imagining this material to be made up of an array of semiconducting P-N junctions arranged electrically in series and parallel so that the surge is shared among all of the grains. Because of the finite resistance of the grains, they act as current limiting resistors and, consequently current flow is distributed throughout the bulk of the material in a manner which reduces the current concentration at each junction.

The MOV has many advantages which make it ideal for use as a suppressor on the low voltage AC power line. The bulk nature of its construction gives it the required energy handling capability to handle the secondary level transients resulting from indirect lightning hits.

MOVs are both cost and size effective, are widely available and do not have a significant amount of overshoot. The flexibility available in the manufacturing of these devices means that different size varistors are available for transient suppression in all categories of the ANSI/IEEE C62.41 standard. They have no follow on current and their response time is more than sufficient for the types of transients encountered in the AC mains environment.

A common misconception is that the device is irreversibly damaged every time it has to suppress a transient. Under high energy transient conditions in excess of the device ratings, the V-I characteristics of the varistor are seen to change. This change is reflected in a decrease in the nominal varistor voltage. After applying a second or third pulse the nominal varistor voltage can be seen to return to its original value (Figure 4). To be conservative, peak pulse limits have been established which, in many cases, have been exceeded many fold without causing harm to the device. Field studies and laboratory tests have shown that the degradation which may result, after a number of pulses outside the ratings of the device, is safe for the equipment being protected. This does not mean that the established limits should be ignored but rather viewed in the perspective of the definition of a failed device. A "failed" device is defined by a ±10% change in the nominal varistor voltage at the 1mA point. This does not imply a non-protecting device, but rather a device whose clamping voltage has been slightly altered.

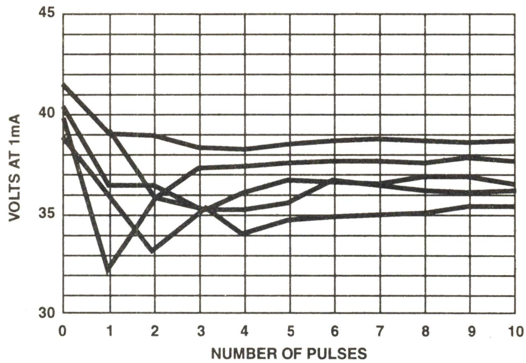


FIGURE 4. REPETITIVE PULSE WITHSTAND CAPABILITIES

Device Comparisons

A range of standard varistors, avalanche diodes, gas tube arresters and filter capacitors were evaluated under a 6kV, 0.5μs x 100kHz ring wave. This transient replicates that called out in location Category A of the ANSI/IEEE C62.41 and is the most benign condition expected in this location. All of the selected devices are rated for use on a $120V_{AC}$ line. The results obtained from this evaluation are per Table 2.

TABLE 2. COMPARATIVE PERFORMANCE DATA[8]

PROTECTION TECHNOLOGY	DEVICE PART NUMBER	AVERAGE PROTECTION LEVEL (kV)	FAILS/ SAMPLE SIZE
Metal Oxide Varistor	V130LA1	0.51	0/10
	V130LA5	0.50	0/10
	V130LA10A	0.49	0/10
Silicon Avalanche Diode	1.5KE200C	0.48	2/10
Gas Tube Surge Arrester	CG2-230	0.67	0/10
Filter Capacitor	C280A-EA4K7	1.30	0/10

Device Selection

To select the correct varistor for a specific application, determine the following information:

1. The maximum system RMS voltage.
2. How is the MOV to be connected?
3. The MOV with a voltage 10% - 25% above system voltage.
4. The worst-case transient energy that will need to be absorbed by the MOV. (Use the guidelines called out in ANSI/IEEE C62.41 -1980).
5. The clamping voltage required for system protection (As device size increases, for a given voltage family, the clamping voltage gets better).

References

For Harris documents available on the web, see http://www.semi.harris.com/
Harris AnswerFAX (407) 724-7800.

[1] "ANSI/IEEE C62.41 -1980 Guide On Surge Voltages In Low-Voltage AC Power Circuits".

[2] "AC Line Voltage Transients and Their Suppression", Corbett, M., Application Note AN9308, Harris Semiconductor, AnswerFAX Doc. No. 99308.

[3] "Understanding AC Line Transient Immunity", Dash, G. and Straus, I.

[4] "Suppression Of Voltage Transients Is An Art Trying To Be A Science", GE # 660.33.

[5] "Surge Protection of Electronics", Haskell, Jr., N.H., P.E.

[6] "Transient Voltage Suppression Devices", Harris Semiconductor DB450.

[7] "The Propagation and Attenuation of Surge Voltages and Currents in Low Voltage AC Circuits", Martzloff, F.D., - 1984.

[8] "Protective Level Comparison of Voltage Transient Suppressors", Hopkins, D.C.

[9] "Comparison of Transient Suppressors!", Korn, S.

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The ABCs of MOVs

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The ABCs of MOVs

The material in this guide has been arranged in 3 parts for easy reference; Section A, Section B and Section C.

"A" is for Applications

This section provides general guidelines on what types of MOV products are best suited for particular environments.

"B" is for Basics

This section explains what Metal Oxide Varistors are, and the basic function they perform.

"C" is for Common Questions

This section helps clarify important information about MOVs for the design engineer, and answers questions that are asked most often.

Want to know more? For a copy of the latest Harris MOV data book, please contact your local Harris sales representative. Also available is the companion document "The ABC's of Multilayer Suppressors", AN9671. For technical assistance, call 1-800-4-HARRIS (US) or visit us on the World Wide Web at http://www.harris.com/

Applications

To properly match the right MOV with a particular application, it is desirable to know:

1. The maximum system RMS or DC voltage.
2. The MOV continuous voltage at 10 - 25% above maximum system voltage.
3. The worst-case transient energy that will need to be absorbed by the MOV.

When the above information is available, these charts offer basic application guidelines:

VOLTAGE (V)	ENERGY (J)	PACKAGING AND OTHER CONSIDERATIONS	PREFERRED SERIES
AC APPLICATIONS			
130-1000	11-360	Through-Hole Mounting Low/Medium AC Power Lines	LA "C" III UltraMOV
130-660	70-250	Shock/Vibration Environment Quick Connect Terminal	PA
130-275	11-23	Surface Mount Leadless Chip	CH
130-750	270-1050	High-Energy Applications Shock/Vibration Environment	DA HA NA DB
130-880	450-3200	Rigid Terminals Primary Power Line Heavy Industrial	BA
1100-2800	3800-10000	Rigid Terminals Heavy Industrial	BB
DC APPLICATIONS			
4-460	0.1-35	Through-Hole Mounting Automotive and Low Voltage Applications	ZA
10-115	0.8-23	Surface Mount Leadless Chip	CH
9-431	0.06 - 1.70	Axial Leaded	MA
3.5-68	0.1-1.2	Surface Mount Multilayer Leadless Chip	ML, MLE
18	3-25.0	Automotive Surface Mount Leadless Chip	AUML

APPLICATION EXAMPLE	TYPICAL SERIES SELECTED†
TV/VCR/White Goods Office Equipment	ZA, LA, UltraMOV, "C" III, CH, MA and ML Series
Motor Control	ZA, LA, UltraMOV, "C" III, PA, HA, NA, BA, BB, DA and DB Series
Transformer (Primary Protection)	ZA, LA, UltraMOV, "C" III, PA, BA, BB, DA, DB, HA and NA Series
Instrumentation	MA, ZA, ML and CH Series
Automotive (Primary/ Secondary Protection)	ZA, CH and AUML Series
Noise Suppression	MA, ML, MLE, CH, ZA, LA, UltraMOV and "C" III Series
Power Supply	PA, LA, UltraMOV, "C" III, ZA, HA, NA, BA, BB, DA and DB Series
Transient Voltage Suppressor AC Power Strip	LA, UltraMOV and "C" III Series
AC Distribution Panels	LA, UltraMOV, "C" III, HA and NA Series
ESD Protection	MLE, ML Series

†See AN9671 for more information on ML, MLE and AUML Series.

Basics

What is a Harris MOV?

A Harris MOV is a Metal Oxide Varistor. Varistors are voltage dependent, nonlinear devices which have an electrical behavior similar to back-to-back Zener diodes. The varistor's symmetrical, sharp breakdown characteristics enable it to provide excellent transient suppression performance. When exposed to high voltage transients, the varistor impedance changes many orders of magnitude – from a near open circuit to a highly conductive level – and clamps the transient voltage to a safe level. The potentially destructive energy of the incoming transient pulse is absorbed by the varistor, thereby protecting vulnerable circuit components and preventing potentially costly system damage.

What is a Harris MOV Made Of?

The Harris varistor is composed primarily of zinc oxide with small additions of bismuth, cobalt, manganese and other metal oxides. The structure of the body consists of a matrix of conductive zinc oxide grains separated by grain boundaries which provide P-N junction semiconductor characteristics.

What is the Scope of the Harris MOV Product Line?

Standard Harris varistors are available with AC operating voltages from 2.5V to 3200V. Higher voltages are limited only by packaging ability. Peak current handling exceeds 70,000 amps, and energy capability extends beyond 10,000 joules for the larger units. Package styles include the tiny tubular device used in connectors, and progress in size up to the rugged industrial blocks.

Common Questions

Agency Listings

Q. Are MOVs listed to Safety Agency standards?

A. This depends upon the MOV's intended usage. For example, all Harris MOVs rated at $130V_{RMS}$ or higher are UL-listed under file number E75961 and/or E56529. (These include all BA/BB, DA/DB, LA and PA series devices as well as ZA devices.) The epoxy encapsulant complies with UL flammability code UL94-VO. Under UL Standard 497B, all ZA and LA series devices are UL approved to file number E135010. Many Harris MOVs are CSA listed, including LA and PA series types. Check the latest copy of the Harris MOV data book for complete, up-to-date listings. Radial devices have also received CECC certification

High Temperature Environments

Q. How can a radial MOV meet the requirements for temperature cycle and 125^oC operating temperatures?

A. On request. Harris radial MOVs can be encapsulated with a special phenolic material that withstands these harsh conditions. Special part number designations will be assigned. ML, AUML, MLE, CH and RA series parts are designed to operate from -55^oC to 125^oC without derating.

Connecting MOVs for Added Protection

Q. Can MOVs be connected in parallel?

A. Yes. The paralleling of MOVs provides increased peak current and energy-handling capabilities for a given application. The determination of which MOVs to use is a critical one in order to ensure that uniform current sharing occurs at high transient levels. It is recommended that Harris performs this screening and selection process.

Q. Can MOVs be connected in series for special voltage applications?

A. Yes. MOVs can be connected in series to provide voltage ratings higher than those normally available, or to provide ratings between the standard offerings.

Q. How are MOVs connected for single-phase and three-phase protection?

A. FOR SINGLE-PHASE AC: The optimum protection is to connect evenly rated MOVs from hot-neutral, hot-ground and neutral-ground. If this configuration is not possible, connection between hot-neutral and hot-ground is best. FOR THREE-PHASE AC: This depends upon the 3-phase configuration. Please refer to the Harris MOV data book.

Current Steering or Directing

Q. Does an MOV simply steer current?

A. No. It is incorrect to believe that an MOV device merely re-directs energy. In fact, the MOV dissipates heat energy within the device by actually absorbing this energy. The degree or level to which this absorption can take place is dependent on the energy rating of the device.

Date Codes

Q. Can you explain the date codes when branded on a Harris MOV?

A. The date codes tell you when the device was manufactured. Presently there are two methods used. A "character-digit" (month-year) system or a "four digit" (year-year-week-week) system where the first two digits

represent the year (97 = 1997) and the second two digits represent the sequential week of the year. Eventually, all product will utilize the "four digit" method. In addition to the date code, the parts will carry the Harris logo and UL, CSA monograms where appropriate.

Failure of Device and Fuse Selection

Q. How does an MOV fail?

A. When subjected to stresses above its ratings, an MOV can fail as a short circuit. If applied conditions significantly exceed the energy rating of the device, and current is not limited, the MOV may be completely destroyed. For this reason, the use of current-limiting fuses is suggested.

Q. How do you select a fuse to prevent failure of an MOV?

A. Fuses should be chosen to limit current below the level where damage to the MOV package could occur. Specific guidance is provided in the Harris MOV data book. Generally, the fuse should be placed in series with either the varistor or the source ahead of the varistor.

Heavy Metals/CFCs

Q. Are heavy metals such as cadmium or mercury or CFCs used in the manufacture of Harris MOVs?

A. No. There are no heavy metals or CFCs used in the manufacture of Harris MOVs.

Lead Inductance/Lead Forms/Lead Coating

Q. Does lead inductance/capacitance affect MOV performance?

A. Yes. Transient wave forms with steep fronts ($\leq 1\mu s$) and in excess of several amps produce an increase in voltage across the varistor. This is a characteristic of all leaded devices including Zeners, known as overshoot. Unlike Zeners, MOVs such as our CH, CPV/CS and ML/AUML series are leadless and do not exhibit overshoot.

Q. What standard lead forms are available on Harris radial MOVs?

A. Radial lead types include outcrimp, undercrimp and inline configurations and meet several criteria for circuit board components (e.g., mechanical stability, lead length and solderability). Harris radial MOVs are also available in tape-and-reel packaging to accommodate auto-insertion equipment.

Q. Are MOV leads coated or tinned?

A. Yes. All leads are electroplated to provide a uniform surface. This process ensures that a subsequent solder coat may be evenly applied.

Part Numbering

Q. What information does an MOV part number provide?

A. MOV part numbers were created to impart product data. Each designation follows the pattern: LETTER/NUMBER/LETTER/NUMBER/LETTER.

Letter.... The prefix "V" stands for Varistor.

Number.. Depending on the product family, this number indicates either a) the maximum $AC_{(RMS)}$ continuous voltage the device can handle or b) the nominal DC voltage (measured with a 1mA test current through the varistor).

Letter .... These two letters (LA, DB, PA, etc.) correspond to a specific product series and package configuration.

Number... This number represents the relative energy rating.

Letter .... This final letter indicates the voltage selection of the device.

Q. Why isn't the entire part number branded on the device?

A. The small size of some components cannot accommodate the relatively lengthy part number. Consequently, abbreviated brands are used. The Harris MOV data book lists these abbreviated brands (along with their corresponding factory part numbers) in the device ratings and characteristics tables of each series.

Sensitivity

Q. Are MOVs sensitive to polarity?

A. No. Since MOVs provide bidirectional clamping, they are not a polarized device.

Q. Are MOVs sensitive to electrostatic discharge?

A. No. In fact, MOVs are specifically designed to protect sensitive integrated circuits from ESD transients, such as with the ML or MLE Series of multilayer suppressors.

Q. Generally speaking, are MOVs sensitive to chemical/pressure when potted?

A. No.

Speed of Response, Compared to Zeners

Q. Are Zeners significantly faster than MOVs?

A. No, not to the extent of the claims made. The intrinsic response time of MOV material is 500 picoseconds. As the vast majority of transients have a slower rise time than this, it is of little or no significance to compare speeds of response. The response time of a leaded MOV or Zener is affected by circuit configuration and lead inductance.

Voltage Regulation, Voltage Limits

Q. Can an MOV be used as a voltage regulator?

A. No. MOVs function as nonlinear impedance devices. They are exceptional at dissipating transient voltage spikes, but they cannot dissipate continuous low level power.

Q. Is it possible to get MOVs with voltages other than those listed in the data book?

A. Yes. The Harris MOV data book discusses standard voltages only. Application-specific MOVs, with voltages tailored to customer requirements, can be manufactured upon request. Contact your Harris sales representative to discuss your individual needs.

Harris Semiconductor

APPNOTE

No. AN9312.3 January 1998 Harris Suppression Products

Suppression of Transients in an Automotive Environment

Author: Martin Corbett

The initial stage of solid state electronics into the automobile began with discrete power devices and IC components. These were to be found in the alternator rectifier, the electronic ignition system and the voltage regulator. This was followed by digital ICs and microprocessors, which are common in engine controls and trip computers. The usage of intelligent power devices and memories is common, benefiting improved electronic controls and shared visual displays. With the extensive use of electronic modules in today's vehicles, protection from transient overvoltages is essential to ensure reliable operation.

Transient Environment

As the control circuitry in the automobile continues to develop, there is a greater need to consider the capability of new technology in terms of survivability to the commonly encountered transients in the automotive environment. The circuit designer must ensure reliable circuit operation in this severe transient environment. The transients on the automobile power supply range form the severe, high energy, transients generated by the alternator/regulator system to the low-level "noise" generated by the ignition system and various accessories. A standard automotive electrical system has all of these elements necessary to generate undesirable transients (Figure 1).

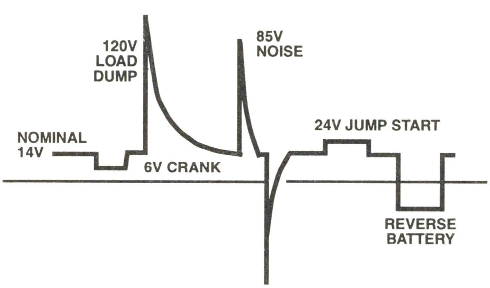

FIGURE 1. TYPICAL AUTOMOTIVE TRANSIENTS

Unlike other transient environments where external influences have the greatest impact, the transient environment of the automobile is one of the best understood. The severest transients result from either a load dump condition or a jump start overvoltage condition. Other transients may also result from relays and solenoids switching on and off, and from fuses opening.

Load Dump

The load dump overvoltage is the most formidable transient encountered in the automotive environment. It is an exponentially decaying positive voltage which occurs in the event of a battery disconnect while the alternator is still generating charging current with other loads remaining on the alternator circuit at the time of battery disconnect. The load dump amplitude depends on the alternator speed and the level of the alternator field excitation at the moment of battery disconnection. A load dump may result from a battery disconnect resulting from cable corrosion, poor connection or an intentional battery disconnect while the car is still running.

Independent studies by the Society of Automotive Engineers (SAE) have shown that voltage spikes from 25V to 125V can easily be generated[1], and they may last anywhere from 40ms to 400ms. The internal resistance of an alternator is mainly a function of the alternator rotational speed and excitation current. This resistance is typically between 0.5Ω and 4Ω (Figure 2).

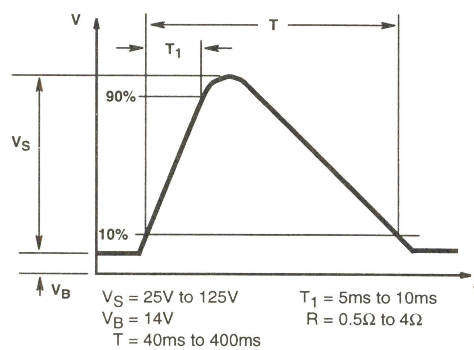

FIGURE 2. LOAD DUMP TRANSIENT

Jump Start

The jump start transient results from the temporary application of an overvoltage in excess of the rated battery voltage. The circuit power supply may be subjected to a temporary overvoltage condition due to the voltage regulator failing or it may be deliberately generated when it becomes necessary to boost start the car. Unfortunately, under such an application, the majority of repair vehicles use 24V "battery"

jump to start the car. Automotive specifications call out an extreme condition of jump start overvoltage application of up to 5 minutes.

The Society of Automotive Engineers(SAE) has defined the automotive power supply transients which are present in the system.

Table 1 shows some sources, amplitudes, polarity, and energy levels of the generated transients found in the automotive electrical system[2].

TABLE 1. TYPICAL AUTOMOTIVE TRANSIENTS

LENGTH OF TRANSIENT	CAUSE	ENERGY CAPABILITY	VOLTAGE AMPLITUDE	FREQUENCY OF OCCURRENCE
Steady State	Failed voltage regulator	•	+18V	Infrequent
5 minutes	Jump starts with 24V battery	•	±24V	Infrequent
200ms to 400ms	Load dump; disconnection of battery while at high charging	>10J	<125V	Infrequent
< 320μs	Inductive-load switching transient	<1J	300V to +80V	Often
200ms	Alternator field decay	<1J	-100V to -40V	Each Turn-Off
90ms	Ignition pulse, battery discon-nected	<0.5J	<75V	< 500Hz Several Times in Vehicle Life
1ms	Mutual coupling in harness	<1J	<200V	Often
15μs	Ignition pulse, normal	<0.001J	3V	< 500Hz Continuous
Burst	Accessory noise	<1.5V		50Hz to 10kHz
Burst	Transceiver feedback	≈20mV		R.F.
<50ns	ESD	<10mJ	15kV	Infrequent

The achievement of maximum transient protection involves many factors. First, consequences of a failure should be determined. Current limiting impedances and noise immunities need to be considered. The state of the circuit under transient conditions (on, off, unknown) and the availability of low cost components capable of withstanding the transients are other factors. Furthermore, the interaction of other parts of the automotive electrical system with the circuit under transient conditions may require definition.

Protection by a Central Suppressor

A central suppressor was the principal transient suppression device in a motor vehicle. As such, it is connected directly across the main power supply line without any intervening load resistance. It must absorb the entire available load dump energy, and withstand the full jump-start voltage. To be cost effective, it usually is best located in the most critical electronic module. In newer applications additional suppressors may be placed at other sites for further suppression and to control locally-generated transients.

The load dump energy available to the central suppressor in the worst case depends on variables such as the alternator size, the response of the sampled-data regulator system, and the loads that share the surge current and energy. Each application therefore tends to be somewhat different. However, by combining several applications, it is possible to construct a representative example. The key fact is the alternator surge power available to be dissipated in the suppressor. Figure 3A is suggested as a starting point for analysis. Since a peak surge power of 1600W is available, a suppressor with a clamping voltage of 40V would draw a peak current of 40A. The surge energy rating needed for the suppressor can be found by taking the integral of the surge power over time, resulting in approximately 85J. A jump-start rating of 24V is also needed.

Evaluating central suppressor devices can be simplified with the aid of a load dump simulator as shown in Figure 3B. The inductor L, which simulates the alternator inductance, slows the surge rise time but does not materially affect the analysis. In the absence of a suppressor or load, the output waveform will be similar to that of Figure 1B. If a suppressor is inserted, the operating characteristics can be estimated as follows:

Assume $V_C = 40V$, then $I_P = (80 - 40V)/R_1 = 40A$

The energy W dissipated in the varistor may be estimated by: $W = 1.4V_C I_P \tau$ (see AN9771 on Energy). The impulse duration τ, of the surge current (see AN9767, Figure 21) can be estimated from the delay time as:

$$\tau = 0.7RC_1$$

where R is the series-parallel combination of the effective resistance of the varistor and simulator components R_1 and R_2. To facilitate this calculation, assume that the effective resistance is given by $V_C/0.7\,I_P = 1.4\Omega$. The delay time constant with the suppressor in the circuit then becomes:

$$RC_1 = \left(\frac{2.4 \times 7}{2.4 + 7}\right)(0.03) = 0.054s$$

and the surge impulse duration:

$$\tau = 0.7\,RC_1 = 0.038s$$

The deposited energy now can be estimated by:

$W = 1.4\ V_C I_P \tau = (1.4)(40)(40)(.038) = 85J$

Hence, the simulator produces unprotected and protected circuit conditions similar to those expected in the vehicle itself.

A suppressor with the needed high energy capability has been developed and already is in use. This improved Harris Varistor model V24ZA50 has a load dump rating of 100J. A narrow-tolerance selection can satisfy the clamping requirement of 40V maximum at 40A, with a jumpstart rating of 24V. The protective performance of this suppressor can be measured conveniently using the simulator circuit shown in Figure 3B.

Suppressor Applications [3]

The sensitive electronics of the automobile need to be protected from both repetitive and random transients. In an environment of random transients, the dominating constraints are energy and clamping voltage vs standby power dissipation. For repetitive transients, transient power dissipation places an additional constraint on the choice of suppression device.

It must also be noted that the worst case transient scenarios, load dump and jump start, place conflicting constraints on the automotive suppressor. The high energy content of the load dump transient must be clamped to a worst case voltage of 40V, while the leakage current/power dissipation drawn under a jump start condition must also be kept to a minimum.

A centrally located suppressor is the principal transient suppression device used in most automobiles. It is connected directly across the main power supply line without any intervening load resistance. It must be capable of absorbing the entire available load dump energy, and must also withstand the full jump start voltage. To be cost effective, it is usually located in the most critical electronic module. Additional secondary suppression is also employed at other locations in the system for further suppression and to control locally generated transients.

As previously mentioned, the maximum load dump energy available to the central suppressor depends on a combination of the alternator size and the loads that share the surge current and energy which are thus generated. It must be remembered that there are many different automotive electronic configurations which result in a variety of diverse load dumps.

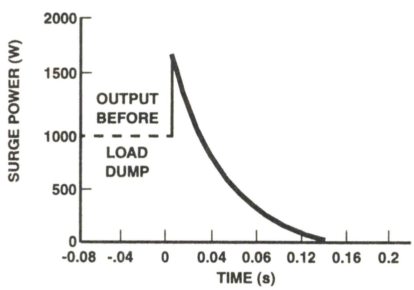

FIGURE 3A. ALTERNATOR POWER OUTPUT INTO A CENTRAL SUPPRESSOR

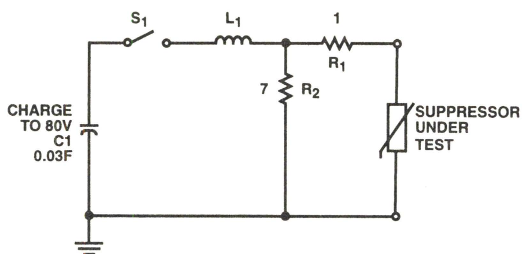

FIGURE 3B. LOAD DUMP SIMULATOR CIRCUIT

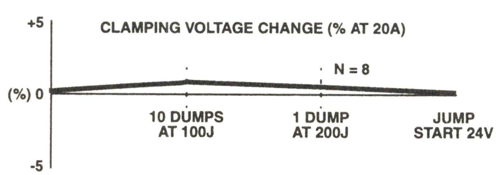

FIGURE 3C. STABILITY OF CLAMPING VOLTAGE

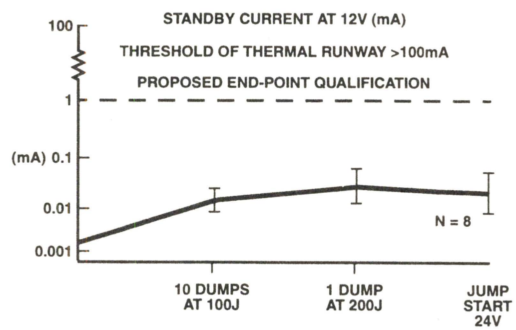

FIGURE 3D. STABILITY OF STANDBY CURRENT

MultiLayer Transient Voltage Surge Suppressor (AUML)[4, 5]

The new automotive multilayer (AUML) transient voltage suppressor is a voltage dependent, nonlinear device. It has an electrical behavior similar to that of a back-to-back zener diodes and it is inherently bidirectional. It offers protection from transients in both the forward and reverse directions. When exposed to high voltage transients, the AUML undergoes a nonlinear impedance change which is many orders of magnitude, from approximately 10^9 to 10Ω.

The crystalline structure of the AUML transient voltage suppressor consists of a matrix of fine, conductive grains separated by uniform grain boundaries, forming P-N junctions (Figure 4). These boundaries are responsible for blocking conduction at low voltages, and are the source of the nonlinear electrical conduction at higher voltages. Conduction of the transient energy takes place between the millions of P-N junctions present in the device. The uniform crystalline grains act as heat sinks for the energy absorbed by the device under a transient condition, and ensures an even distribution of the transient energy (heat) throughout the device. This even distribution results in enhanced transient energy capability and long term reliability.

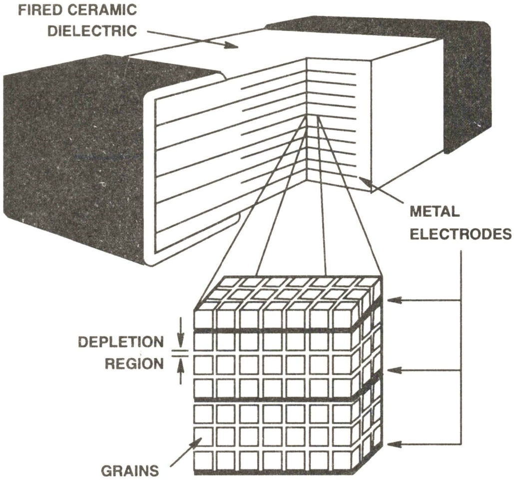

FIGURE 4. AUML TRANSIENT VOLTAGE SUPPRESSOR

The AUML is constructed by forming a combination of alternating electrode layers and semiconducting ceramic layers into a rectangular block. Each alternate layer of electrode material, separated by ceramic semiconducting material, is connected to opposite end terminations of the device.

The paralleled arrangement of the inner electrode layers represents significantly more active surface area than the small outline of the package may suggest (Figure 5). This increased active surface area, combined with an interdigitated block formation, results in proportionally higher peak energy capability.

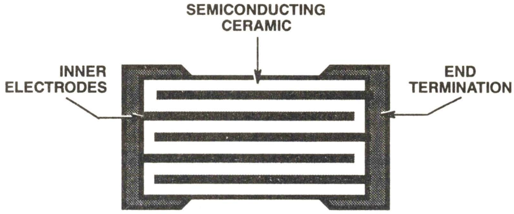

FIGURE 5. AUML INNER CONSTRUCTION

The AUML surge suppressor is a surface mountable device that is much smaller in size than the components it is designed to protect. The present size offerings for suppression in the automotive environment are “1210” (0.120 x 0.100 inches), “1812” (0.180 x 0.120 inches) and “2220” (0.220 x 0.200 inches). The correct device to use depends on the location of the suppressor in the overall electronics system.

Device Ratings and Characteristics

Package Outline

The present size offerings of the AUML series are the industry 2220, 1812 and 1210 standard form factors. Since the AUML device is inherently bidirectional, symmetrical orientation for placement on a printed circuit board is not a concern. Its robust construction makes it ideally suitable to endure the thermal stresses involved in the soldering, assembling and manufacturing steps involved in surface mount technology. The AUML device is inherently passivated by means of the fired ceramic material. They will not support combustion and are thus immune to the risk of flammability which may be present in the plastic or epoxy molded diode devices.

Load Dump Energy Capability

The most damaging classification of transients an automobile must survive is a load dump discharge occurrence. A load dump transient occurs when the alternator load in the automobile is abruptly reduced and the battery clamping effect is thus removed. The worst case scenario of the load dump occurs when the battery is disconnected while operating at full rated load. The resultant load dump energy handling capability serves as an excellent figure of merit for the AUML suppressor.

Standard load dump specifications require a device capability of 10 pulses at rated energy, across a temperature range of -40°C to 125°C. This capability requirement is well within the ratings of all of the AUML series.

Due to the assortment of electronic applications in an automotive circuit, there is a need for a wide range of surge suppressors. The transient environment can generally be divided into three distinct sections and there will be a need for a different type of suppressor within each section. The 2220 size was designed for operation in the primary transient area, i.e. directly across the alternator. The 1812 size for secondary protection and the 1210 size for tertiary protection. A typically load dump transient results in an energy discharge of approximately 100J (depending on the

size of the alternator). The deciding factor in the selection of the correct size suppressor is the amount of energy which is dissipated in the series and parallel loads in the circuit. The higher the impedance between the battery and the system requiring suppression, the smaller is the suppressor required.

Random samples of the 1210, 1812 and 2220 devices were subjected to repetitive load dump pulses at their rated energy level. This testing was performed across a temperature spectrum from -40°C to 125°C. This temperature range simulates both passenger compartment and under the hood operation. There was virtually no change in the device characteristics of any of the units tested (Figure 6).

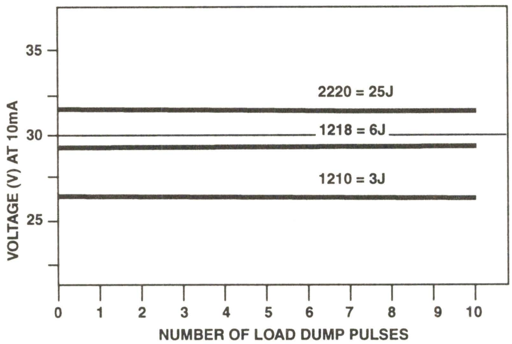

FIGURE 6. LOAD DUMP PULSING OVER A TEMPERATURE RANGE OF - 55°C TO 125°C

Further testing on the AUML series has resulted in the extension the number of load dump pulses, at rated energy, which are applied to the devices. The reliability information thus generated gives an indication of the inherent capability of the series of devices. The V18AUMLA1210 sample has been subjected to over 2000 pulses at its rated energy of 3J; the V18AUMLA1812 sample over 1000 times at 6J. The V18AUMLA2220 sample has been pulsed at 25J over 300 times (Figure 7). In all cases there has been little or no change in the device characteristics.

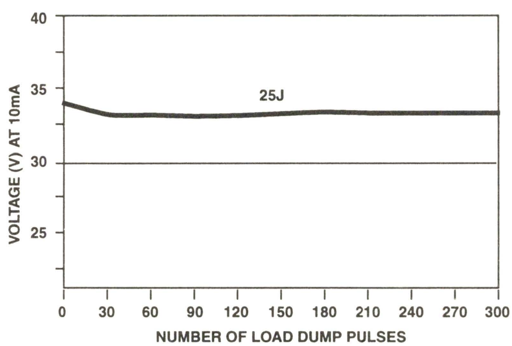

FIGURE 7. REPETITIVE LOAD DUMP PULSING AT RATED LOAD DUMP ENERGY

As previously discussed, the very high energy absorption capability of the AUML suppressor series is achieved by means of a new, highly controlled manufacturing process. This new multilayer technology ensures that a large volume of suppressor material, with an interdigitated layer construction, is available in an extremely small package. Unlike equivalent rated silicon TVS diodes, all of the AUML device package is available to act as an effective, uniform heat sink. Hence, the peak temperatures generated by the load dump transient are evenly dissipated throughout the complete device. This even energy dissipation ensures that there are lower peak temperatures generated at the P-N grain boundaries of the AUML suppressor.

Experience has shown that while the effects of a load dump transient are of real concern, its frequency of occurrence is much less than that of localized low energy inductive spikes. Such low energy spikes may be generated as a result of motors turning on and off, from ESD occurrences, or from any number of other sources. It is essential that the suppression technology selected also has the capability to suppress such transients. Testing on the V18AUMLA2220 has shown that after being subjected to a repetitive energy pulse of 2J, over 6000 times, no characteristic changes have occurred (Figure 8).

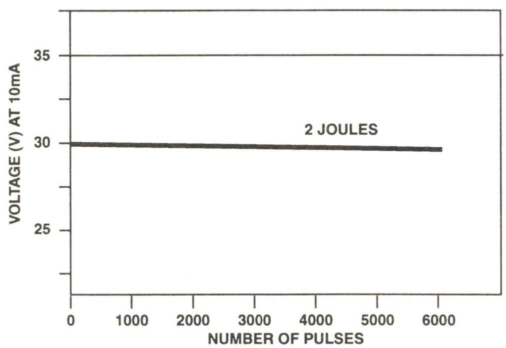

FIGURE 8. REPETITIVE ENERGY TESTING OF THE V18AUMLA2220 AT LOW ENERGY LEVELS

Clamping Voltage

The clamping voltage of a suppressor is the peak voltage appearing across the device when measured under conditions of a specified current pulse waveform. The industry recommended waveform for clamping voltage is the 8/20μs pulse which has been endorsed by UL, IEEE and ANSI. The maximum clamping voltage of the AUML should be below the system or component failure level. Shunt type suppressors like the AUML are used in parallel to the systems they protect. Their effectiveness can be increased by understanding the important influence that source and line impedance play in the overall system (Figure 9).

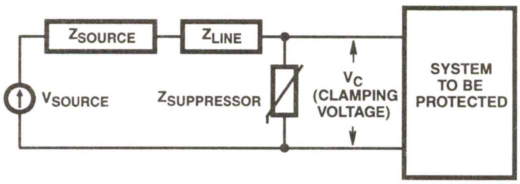

FIGURE 9. VOLTAGE DIVISIONS BETWEEN SOURCE, LINE AND SUPPRESSOR IMPEDANCE

To obtain the lowest clamping voltage (V_C) possible, it is desirable to use the lowest suppressor impedance ($Z_{SUPPRESSOR}$) and the highest line impedance (Z_{LINE}). The suppressor impedance is an inherent feature used to select the device, but the line impedance can become an important factor in selecting the location of the suppressor by adding resistances or inductances in series.

$$V_C = \frac{V_{SUPPRESSOR} \times V_{SOURCE}}{Z_{SUPPRESSOR} + Z_{LINE} + Z_{SOURCE}}$$

Speed of Response

The clamping action of the AUML suppressor depends on a conduction mechanism similar to that of other semiconductor devices (i.e. the P-N Junction). The apparent slow response time often associated with transient suppressors is due to parasitic inductance in the package and leads of the device, and is independent of the conducting material. The most critical element affecting the response time of a suppressor is the inductance of the lead material and hence the lead length.

The AUML suppressor is a surface mount device with no leads or external packaging, and thus, virtually zero inductance. The response time of a AUML surge suppressor is in the 1ns to 5ns range, which is more than sufficient for the transients which are encountered in the automotive environment.

Temperature Effects

In the off-state (leakage) region of the multilayer suppressor, the device characteristics approach a linear (ohmic) relationship and shows a temperature dependent affect. In this region the suppressor is in a very high resistance mode (approaching $10^9\Omega$) and appears as a near open circuit. Leakage currents at maximum rated voltage are in the low microamp range. When suppressing transients at higher currents (at and above the ten milliamp range), the AUML suppressor approaches a near short-circuit. In this region the characteristics of the AUML are virtually temperature independent. The clamping voltage of a multilayer transient voltage suppressor are the same at -55°C and 125°C (Figure 10).

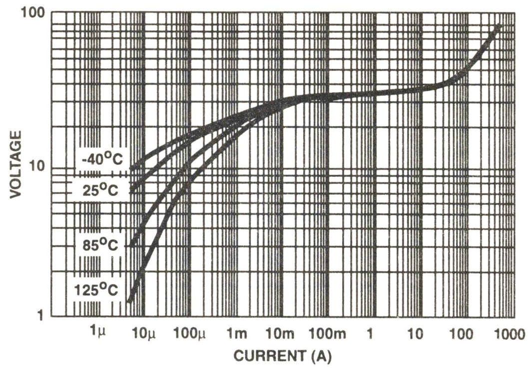

FIGURE 10. TYPICAL V - I CHARACTERISTICS OF THE V18AUMLA2220 AT -40°C, 25°C, 85°C AND 125°C

Soldering Recommendations for Multilayer Surge Suppressors[6]

When soldering all surface mount components onto printed circuit boards there are certain materials, parameters and processes which must be considered. These include:

1. Printed Circuit Board Material
2. Flux used
3. Land Pad Size
4. Soldering Methods
   4.1 Infrared Reflow Solder
   4.2 Vapor Phase Solder
   4.3 Wave Solder
5. Cleaning Methods and Fluids Employed

Substrates

There are a wide choice of substrate materials available for use as printed circuit boards in a surface mount application. The main factors which determine the choice of material to use are:

1. Electrical performance
2. Size and weight limitations
3. Thermal characteristics
4. Mechanical characteristics
5. Cost

When choosing a substrate material, the coefficient of thermal expansion for the ML surface mountable suppressor of 6ppm/°C is an important consideration. Non-organic materials (ceramic based substrates), like aluminum or beryllia, which have coefficients of thermal expansion of 5ppm - 7ppm/°C, are a good match. Table 2 below outlines some of the other materials used, and also there more important properties pertinent to surface mounting.

While the choice of substrate material should take note of the coefficient of expansion of the devices, this may not be the determining factor in whether a device can be used or not. Obviously the environment of the finished circuit board will determine what level of temperature cycling will occur. It is this which will dictate the criticality of the match between device and printed circuit board. Currently for most applications the ML series use FR4 boards without issue.

TABLE 2. SUBSTRATE MATERIAL PROPERTIES

SUBSTRATE STRUCTURE	MATERIAL PROPERTIES		
	GLASS TRANSITION TEMPERATURE (^{o}C)	XY COEFFICIENT OF THERMAL EXPANSION (PPM/^{o}C)	THERMAL CONDUCTIVITY (W/M^{o}C)
Epoxy Fiberglass FR4	125	14 - 18	0.16
Polyamide Fiberglass	250	12 - 16	0.35
Epoxy Aramid Fiber	125	6 - 8	0.12
Fiber/Teflon Laminates	75	20	0.26
Aluminum-Beryllia (Ceramic)	Not Available	5 - 7	21.0

Fluxes

Fluxes are used for the chemical cleaning of a substrate surface. They will remove any surface oxides, and will also prevent reoxidation. They can contain active ingredients such as solvents for removing soils and greases. Nonactivated fluxes ("R" type) are relatively effective in reducing oxides of copper, nickel or palladium/silver metallizations and are recommended for use with the Harris surface mount suppressor range.

Mildly activated fluxes ("RMA" type) have natural and synthetic resins, which reduce oxides to metal or soluble salts. These "RMA" fluxes are generally not conductive nor corrosive at room temperature and are the most commonly used in the mounting of electronic components.

The "RA" type (fully activated) fluxes are corrosive, difficult to remove, and can lead to circuit failures and other problems. Other nonresin fluxes depend on organic acids to reduce oxides. They are also corrosive after soldering and also can damage sensitive components. Water soluble types in particular must be thoroughly cleaned from the assembly.

Environmental concerns, and associated legislation, has led to a growing interest in fluxes with residues that can be removed with water or water and detergents (semiaqueous cleaning). Many RMA fluxes can be converted to water soluble forms by adding saponifers. There are detergents and semiaqueous cleaning apparatus available that effectively remove most RMA type fluxes. Semiaqueous cleaning also tends to be less expensive than solvent cleaning in operations where large amounts of cleaning are needed.

For the Harris Semiconductor range of surface mount varistors, nonactivated "R" type fluxes such as Alpha 100 or equivalent are recommended.

Land Pad Patterns

Land pad size and patterns are one of the most important aspects of surface mounting. They influence thermal, humidity, power and vibration cycling test results. Minimal changes (even as small as 0.005 inches) in the land pad pattern have proven to make substantial differences in reliability.

This design /reliability relationship has been shown to exist for all types of designs such as in J-lead, quadpacks, chip resistors, capacitors and small outline integrated circuit (SOIC) packages. Optimum and tested land pad dimensions are provided for some surface mounted devices along with formulas which can be applied to different size varistors. Figure 11 gives optimum land patterns for the direct mount multilayer devices, while Table 3 outlines the optimum size of the land pad for each device size.

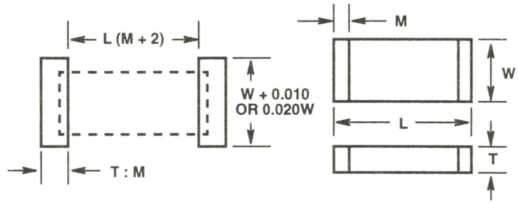

FIGURE 11. LAND PAD PATTERNS FOR MULTILAYER SUPPRESSORS

TABLE 3. RECOMMENDED MOUNTING PAD OUTLINE

SUPPRESSOR SIZE	DIMENSION		
	T + M	L - 2M	W+0.01 OR 0.02*W
1206	1.65	1.85	2.62
1210	1.85	1.85	3.73
1812	1.85	3.20	4.36
2220	1.84	4.29	6.19

Solder Materials and Soldering Temperatures

No varistor should be held longer than necessary at an elevated temperature. Exceeding the temperature and time limits can result in excessive leakage and alterations of the I-V characteristics.

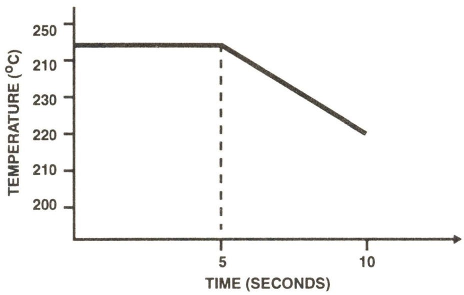

FIGURE 12. RECOMMENDED TIME AND SOLDER TEMPERATURE

To ensure that there is no leeching of the silver electrode on the varistor, solders with at least 2% silver content are recommended (62 Sn / 36 Pb / 2 Ag). Examples of silver bearing solders and their associated melting temperatures are per Table 4.

TABLE 4. SILVER BEARING SOLDERS (ALPHA METALS)

ALLOY	MELTING TEMPERATURE	
	°F	°C
62Sn/36Pb/2Ag	355	179
96.5Sn/3.5Ag	430	221
95Sn/5Ag	430 - 473	221 - 245
20Sn/88Pb/2Ag	514 - 576	268 - 302

Soldering Methods

There are a number of different soldering techniques used in the surface mount process. The most common soldering processes are infra red reflow, vapor phase reflow and wave soldering.

For the Harris surface mount suppressor range, the solder paste recommended is a 62/36/2 silver solder. While this configuration is best, other silver solder pastes can also be used. In all soldering applications, the time at peak temperature should be kept to a minimum. Any temperature steps employed in the solder process must, in broad terms, not exceed 70°C to 80°C. In the preheat stage of the reflow process, care should be taken to ensure that the chip is never subjected to a thermal gradient of greater than 4°C per second; the ideal gradient being 2°C per second. For optimum soldering, preheating to within 100°C of the peak soldering temperature is recommended; with a short dwell at the preheat temperature to help minimize the possibility of thermal shock. The dwell time at this preheat temperature should be for a time greater than $10T^2$ seconds, where T is the chip thickness in millimeters. Once the soldering process has been completed, it is still necessary to protect against further effects of thermal shocks. One possible cause of thermal shock at the post solder stage is when the hot printed circuit boards are removed from the solder bath and immediately subjected to cleaning solvents at room temperature. To avoid this thermal shock affect, the boards must first be allowed to cool to less than 50°C prior to cleaning.

Two different resistance to solder heat tests are routinely performed by Harris Semiconductor to simulate any possible effects that the high temperatures of the solder processes may have on the surface mount chip. These tests consist of the complete immersion of the chip in to a solder bath at 260°C for 5 seconds and also in to a solder bath at 220°C for 10 seconds. These soldering conditions were chosen to replicate the peak temperatures expected in a typical wave soldering operation and a typical reflow operation.

Reflow Soldering

There are two major reflow soldering techniques used in SMT today:

1. InfraRed (IR) Reflow
2. Vapor Phase Reflow

The only difference between these two methods is the process of applying heat to melt the solder. In each of these methods precise amounts of solder paste are applied to the circuit board at points where the component terminals will be located. Screen or stencil printing, allowing simultaneous application of paste on all required points, is the most commonly used method for applying solder for a reflow process. Components are then placed in the solder paste. The solder pastes are a viscous mixture of spherical solder powder, thixotropic vehicle, flux and in some cases, flux activators.

During the reflow process, the completed assembly is heated to cause the flux to activate, then heated further, causing the solder to melt and bond the components to the board. As reflow occurs, components whose terminations displace more weight, in solder, than the components weight will float in the molten solder. Surface tension forces work toward establishing the smallest possible surface area for the molten solder. Solder surface area is minimized when the component termination is in the center of the land pad and the solder forms an even fillet up the end termination. Provided the boards pads are properly designed and good wetting occurs, solder surface tension works to center component terminations on the boards connection pads. This centering action is directly proportional to the solder surface tension. Therefore, it is often advantageous to engineer reflow processes to achieve the highest possible solder surface tension, in direct contrast to the desire of minimizing surface tension in wave soldering.

In designing a reflow temperature profile, it is important that the temperature be raised at least 20°C above the melting or liquidus temperature to ensure complete solder melting, flux activation, joint formation and the avoidance of cold melts. The time the parts are held above the melting point must be long enough to alloy the alloy to wet, to become homogenous and to level, but not enough to cause leaching of solder, metallization or flux charring.

A fast heating rate may not always be advantageous. The parts or components may act as heat sinks, decreasing the rate of rise. If the coefficients of expansion of the substrate

and components are too diverse or if the application of heat is uneven, fast breaking or cooling rates may result in poor solder joints or board strengths and loss of electrical conductivity. As stated previously, thermal shock can also damage components. Very rapid heating may evaporate low boiling point organic solvents in the flux so quickly that it causes solder spattering or displacement of devices. If this occurs, removal of these solvents before reflow may be required. A slower heating rate can have similar beneficial effects.

InfraRed (IR) Reflow

InfraRed (IR) reflow is the method used for the reflowing of solder paste by the medium of a focused or unfocused infra red light. Its primary advantage is its ability to heat very localized areas.

The IR process consists of a conveyor belt passing through a tunnel, with the substrate to be soldered sitting on the belt. The tunnel consists of three main zones; a non-focused preheat, a focused reflow area and a cooling area. The unfocused infrared areas generally use two or more emitter zones, thereby providing a wide range of heating profiles for solder reflow. As the assembly passes through the oven on the belt, the time/temperature profile is controlled by the speed of the belt, the energy levels of the infrared sources, the distance of the substrate from the emitters and the absorptive qualities of the components on the assembly.

The peak temperature of the infrared soldering operation should not exceed 220^{o}C. The rate of temperature rise from the ambient condition to the peak temperature must be carefully controlled. It is recommended that no individual temperature step is greater than 80^{o}C. A preheat dwell at approximately 150^{o}C for 60 seconds will help to alleviate potential stresses resulting from sudden temperature changes. The temperature ramp up rate from the ambient condition to the peak temperature should not exceed 4^{o}C per second; the ideal gradient being 2^{o}C per second. The dwell time that the chip encounters at the peak temperature should not exceed 10 seconds. Any longer exposure to the peak temperature may result in deterioration of the device protection properties. Cooling of the substrate assembly after solder reflow is complete should be by natural cooling and not by forced air.

The advantages of IR Reflow are its ease of setup and that double sided substrates can easily be assembled. Its biggest disadvantage is that temperature control is indirect and is dependent on the IR absorption characteristics of the component and substrate materials.

On emergence from the solder chamber, cooling to ambient should be allowed to occur naturally. Natural cooling allows a gradual relaxation of thermal mismatch stresses in the solder joints. Forced air cooling should be avoided as it can induce thermal breakage.

The recommended temperature profile for the IR reflow soldering process is as Figure 13 and Table 5.

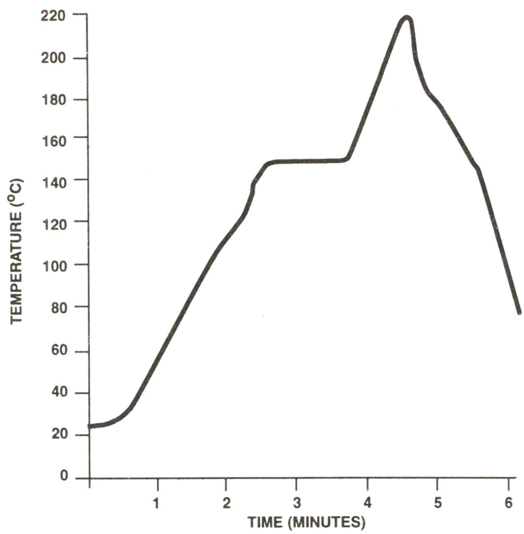

FIGURE 13. TYPICAL TEMPERATURE PROFILE FOR IR REFLOW SOLDER PROCESS

TABLE 5. RECOMMENDED TEMPERATURE PROFILE

INFRARED (IR) REFLOW	
TEMPERATURE (^{o}C)	TIME (SECONDS)
25-60	60
60-120	60
120-155	30
155-155	60
155-220	60
220-220	10
220-50	60

Vapor Phase Reflow

Vapor phase reflow soldering involves exposing the assembly and joints to be soldered to a vapor atmosphere of an inert heated solvent. The solvent is vaporized by heating coils or a molten alloy, in the sump or bath. Heat is released and transferred to the assembly where the vapor comes in contact with the colder parts of the substrate and then condenses. In this process all cold areas are heated evenly and no areas can be heated higher than the boiling point of the solvent, thus preventing charring of the flux. This method gives a very rapid and even heating affect. Further advantages of vapor phase soldering is the excellent control of temperature and that the soldering operation is performed in an inert atmosphere.

The liquids used in this process are relatively expensive and so, to overcome this a secondary less expensive solvent is often used. This solvent has a boiling temperature below 50°C. Assemblies are passed through the secondary vapor and into the primary vapor. The rate of flow through the vapors is determined by the mass of the substrate. As in the case of all soldering operations, the time the components sit at the peak temperature should be kept to a minimum. In the case of Harris surface mount suppressors a dwell of no more than 10 seconds at 222°C is recommended.

On emergence from the solder system, cooling to ambient should be allowed to occur naturally. Natural cooling allows a gradual relaxation of thermal mismatch stresses in the solder joints. Forced air cooling should be avoided as it can induce thermal breakage.

The recommended temperature profile for the vapor phase soldering process is as Figure 14 and Table 6.

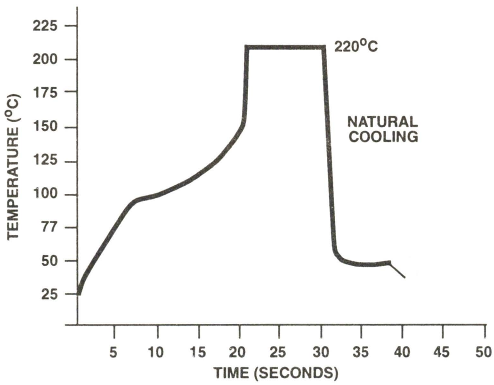

FIGURE 14. TYPICAL TEMPERATURE PROFILE FOR VAPOR PHASE REFLOW SOLDERING

TABLE 6. RECOMMENDED TEMPERATURE PROFILE

INFRARED (IR) REFLOW	
TEMPERATURE (°C)	TIME (SECONDS)
25-90	8
90-150	13
150-222	3
222-222	10
222-80	7
80-25	10

Wave Solder

This technique, while primarily used for soldering thru hole or leaded devices inserted into printed circuit boards, has also been successfully adapted to accommodate a hybrid technology where leaded, inserted components and adhesive bonded surface mount components populate the same circuit board.

The components to be soldered are first bonded to the substrate by means of a temporary adhesive. The board is then fluxed, preheated and dipped or dragged through two waves of solder. The preheating stage serves many functions. It evaporates most of the flux solvent, increases the activity of the flux and accelerates the solder wetting. It also reduces the magnitude of the temperature change experienced by the substrate and components.

The first wave in the solder process is a high velocity turbulent wave that deposits large quantities of solder on all wettable surfaces it contacts. This turbulent wave is aimed at solving one of the two problems inherent in wave soldering surface mount components, a defect called voiding (i.e. skipped areas). One disadvantage of the high velocity turbulent wave is that it gives rise to a second defect known as bridging, where the excess solder thrown at the board by the turbulent wave spans between adjacent pads or circuit elements thus creating unwanted interconnects and shorts.

The second, smooth wave accomplishes a clean up operation, melting and removing any bridges created by the turbulent wave. The smooth wave also subjects all previous soldered and wetted surfaces to a sufficiently high temperature to ensure good solder bonding to the circuit and component metallizations. In wave soldering, it is important that the solder have low surface tension to improve its surface wetting characteristics. Therefore, the molten solder bath is maintained at temperatures above its liquid point.

On emergence from the solder wave, cooling to ambient should be allowed to occur naturally. Natural cooling allows a gradual relaxation of thermal mismatch stresses in the solder joints. Forced air cooling should be avoided as it can induce thermal breakage.

The recommended temperature profile for the wave soldering process is as Table 7.

TABLE 7. RECOMMENDED TEMPERATURE PROFILE

WAVE SOLDER	
TEMPERATURE (°C)	TIME (SECONDS)
25-125	60
125-180	60
180-260	60
260-260	5
260-180	60
180-80	60
80-25	60

Cleaning Methods and Cleaning Fluids

The objective of the cleaning process is to remove any contamination, from the board, which may affect the chemical, physical or electrical performance of the circuit in its working environment.

There are a wide variety of cleaning processes which can be used, including aqueous based, solvent based or a mixture of both, tailored to meet specific applications. After the soldering of surface mount components there is less residue to remove than in conventional through hole soldering. The cleaning process selected must be capable of removing any contaminants from beneath the surface mount assemblies. Optimum cleaning is achieved by avoiding undue delays between the cleaning and soldering operations; by a minimum substrate to component clearance of 0.15mm and by avoiding the high temperatures at which oxidation occurs.

Harris recommends 1,1,1 trichloroethane solvent in an ultrasonic bath, with a cleaning time of between two and five minutes. Other solvents which may be better suited to a particular application and can also be used may include those outlined in Table 8.

TABLE 8. CLEANING FLUIDS

Water	Acetone
Isopropyl Alcohol	Fluorocarbon 113
Fluorocarbon 113 Alcohol	N-Butyl
1,1,1, Trichloroethane	Trichloroethane
Toluene	Methane

Comparison to Other Device Technologies

There are many design considerations involved when selecting the correct transient suppressor for an automotive application. One obvious consideration is cost. Other factors such as load dump energy capability, clamping voltage, temperature dependance, and size must also be weighed. Each of these factors will now be discussed.

Energy Capability

The large active electrode area available to the AUML suppressor ensures that load dump energy handling capability is one of it's best features. By virtue of its interdigitated construction, the AUML suppressor is capable of dissipating significant amounts of energy over a very small volume of material. The interdigitated construction also ensures that the very high temperatures resulting from a load dump transient will be evenly dissipated through millions of P-N junctions.

Silicon surge suppressors may also be used for the suppression of transients in an automotive environment. In the case of a silicon suppressor, only one P-N junction is available to handle the energy of the load transient. It should be noted that many different materials, with varying thermal coefficients of expansion, are employed in the construction of a silicon suppressor. This may result in extreme thermal stresses being created in the body of the suppressor during a load dump condition.

Comparing the typical peak current, energy and power derating curves of the Harris multilayer to an equivalent silicon suppressor at 125°C, the AUML has 100% of rated value while the zener diode has only 35% (Figure 15).

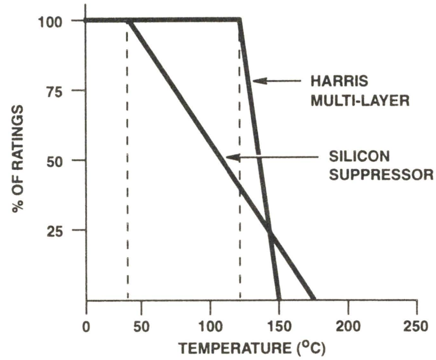

FIGURE 15. AUML AND SILICON SUPPRESSORS CURRENT, ENERGY AND POWER DERATING CURVE

Clamping Voltage

In the majority of automotive applications, the maximum clamping voltage requirement for the primary surge suppressor is 40V at 40A (8/20μs current waveform). Both the AUML and silicon suppressors easily meet this requirement.

The V-I characteristic for a silicon diode is defined over a small current range (1 decade). The AUML current range is extended over a few more decades, which illustrates it's large peak current and energy handling capability.

Temperature Effects

Both the AUML and the silicon diode have a temperature dependance with respect to off state leakage current - leakage current increases as temperature increases. However, beyond the breakdown point, the clamping voltage of the AUML will remain constant between 25°C and 125°C, while the clamping voltage for the zener diode at 125°C is higher than that specified at 25°C.

Size

Common surface mount surge suppressors available are leaded gull-wing and j-bend silicon diodes or a relatively large surface mount metal oxide varistor. In these cases a large area of the PC board is needed for mounting. As previously mentioned, electrically equivalent AUML suppressors are much smaller than their silicon counterparts, resulting in significant surface mount PC board area savings (Figure 16).

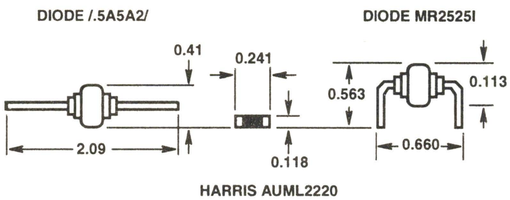

FIGURE 16. SIZE COMPARISONS OF AUTOMOTIVE SURGE SUPPRESSORS

The compact size of the AUML suppressor is obtained by the paralleled stacking manufacturing process. This results in a high density energy absorber where the device volume is not taken up by lead frames, headers, external leads, and epoxy. Additional board area savings are also realized with the smaller solder mounting area required by the AUML.

Description of AUML Ratings and Characteristics

Maximum Continuous DC Working Voltage ($V_{M(DC)}$): This is the maximum continuous dc voltage which may be applied, up to the maximum operating temperature (125°C), to the AUML suppressor. This voltage is used as the reference test point for leakage current and is always less than the breakdown voltage of the device.

Load Dump Energy Rating (W_{ld}): A load dump occurs when the alternator load is suddenly reduced. The worst case load dump is caused by disconnecting a discharged battery when the alternator is running at full load. The load dump energy discharge occurs with the rated battery voltage also applied and must not cause device failure. This pulse can be applied to the AUML suppressor in either polarity.

Maximum Clamping Voltage (V_C): This is the peak voltage appearing across the AUML suppressor when measured with an 8/20μs pulse current (Figure 17).

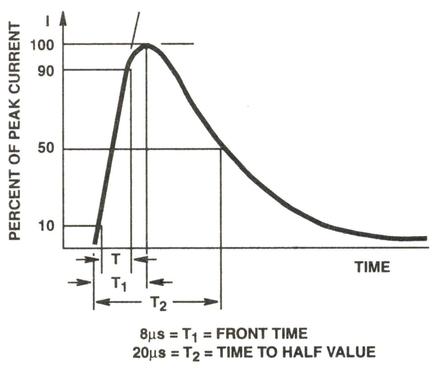

FIGURE 17.

Leakage Current (I_L): This is the amount of current drawn by the AUML suppressor in its non-operational mode, i.e. when the voltage applied across the AUML does not exceed the rated $V_{M(DC)}$ voltage of the device.

Nominal Voltage ($V_{N(DC)}$): This is the voltage at which the AUML enters its conduction state and begins to suppress transients. In the automotive environment this voltage is defined at the 10mA point and has a minimum and maximum voltage specified.

References

For Harris documents available on the web, see http://www.semi.harris.com/
Harris AnswerFAX (407) 724-7800.

[1] Electromagnetic Susceptibility Measurement Procedures for Vehicle Components - SAE J1113, August, 1987.

[2] “Transient Voltage Suppression in Automotive Vehicles”, Application Note AN9002, Harris Semiconductor, AnswerFAX Doc. No. 99002.

[3] Transient Voltage Suppression Devices, Harris Semiconductor DB450.

[4] “Transient Suppression in the Automotive Environment”, Corbett, M. and McCambridge, P., Automotive Electronic Design, October, 1991.

[5] “Harris “ML” Multilayer Surface Mount Surge Suppressors”, Application Note AN9108, Harris Semiconductor, AnswerFAX Doc. No. 99108.

[6] CANE SMT 2588, Syfer Technology Limited, UK.

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APPLICATION NOTES

IEC 1000-4-2 ESD Immunity and Transient Current Capability for the Harris SP720, SP721 and SP723 Electronic Protection Array Circuits

Author: Wayne Austin

The SP720, SP721 and SP723 are protection ICs with an array of SCR/Diode bipolar structures for ESD and over-voltage protection of sensitive input circuits. They have 2 protection SCR/Diode device structures per input. The SP720 is supplied in 16 lead DIP and SOIC packages and has a total of 14 available inputs that can be used to protect up to 14 external signal or bus lines. The SP721 and SP723 are 8 pin devices with the same protection structures and have the same package options. The SP723 has dual cell structures for each input to achieve substantially improved ESD and Transient Current capability.

The SCR structures are designed for fast triggering at a threshold of one $+V_{BE}$ diode threshold above V+ (positive supply terminal) or a $-V_{BE}$ diode threshold below V- (negative or ground). A clamp to V+ is activated at each protection input if a transient pulse causes the input to be increased to a voltage level greater than one V_{BE} above V+. A similar clamp to V- is activated if a negative pulse, one V_{BE} less than V-, is applied to an input.

Various standards for testing the ESD capability of semiconductor products have been developed in recent years. Each standard was generated with regard to a specific need related to the electromagnetic compatibility of the system environment. They include the Human Body Model (HBM), Machine Model (MM) and the Charged Device Model (CDM). Each such standard relates to the nature of electrostatic discharge generated within a system application and the potential for damage to the IC. For these better known standards, the actual results for ESD tests on the SP720 and SP721 are as follows:

1. Human Body Model using a modified version of the MIL-STD-883, Method 3015.7; with V+ and V- grounded and ESD discharge applied to each individual IN pin - Passed all test levels from ±9kV to ±16kV (1kV steps).
2. Human Body Model using the MIL-STD-883, Method 3015.7 (with V- only grounded) and ESD discharge applied to each individual IN pin - Passed all test levels to ±6kV, failed ±7kV (1kV steps).
3. Machine Model using EIAJ IC121 ($R_D = 0\Omega$); discharge applied to IN pins with all others grounded - Passed all test levels to ±1kV, failed ±1.2kV; (200V steps).
4. Human Body Model using the IEC 1000-4-2 standard with V+ and V- grounded and ESD discharge applied to each individual IN pin - Passed test Level 2.

The SP723 capability surpasses those of the SP720 and SP721 and meets the Level 4 requirements of the IEC 1000-4-2 HBM standard.

IEC 1000-4-2 ESD Standard

One of the more recent standards to be developed is the IEC (International Electrotechnical Commission) 1000-4-2. The IEC document relates to the HBM but encompasses a range of normal environmental conditions. Testing for ESD immunity is more broadly defined to include a device, equipment or system. Both direct contact and air discharge methods of testing are used with four discrete steps in the severity level ranging up to 8kV and 15kV respectively. In its simplest form, the Figure 1 test circuit provides for a means of charging the 150pF capacitor, R_C through the charge switch and discharging ESD pulses through the 330Ω resistor, R_D and discharge switch to the Equipment or Device Under Test (EUT, DUT) under test.

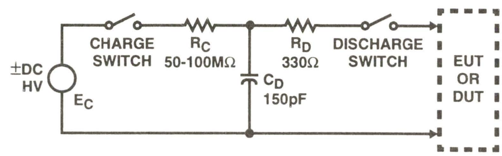


FIGURE 1. SIMPLIFIED IEC 1000-4-2 ESD TEST ENERGY SOURCE

The test equipment for the IEC 1000-4-2 standard is constructed to provide the equivalent of an actual human body ESD discharge and has the waveform shown in Figure 2.

The IEC 1000-4-2 severity level of testing is defined by stepping the DC High Voltage rather than changing the R_C discharge components. The severity levels are separately defined for plus and minus polarity of direct contact discharge (preferred) and air discharge as shown in Table 1. Other voltage levels may be specified for the IEC 1000-4-2 test equipment and conditions.

As a subsystem component, the SP720, SP721 and SP723 may be used at the PC board or module interface for protection. In a typical application, the ESD Protection Arrays would be used to protect more sensitive circuits at the line interface or input terminals to a board or module.

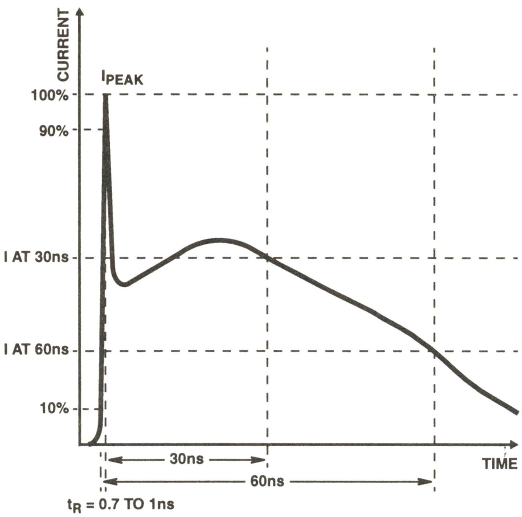


FIGURE 2. TYPICAL WAVEFORM OF THE OUTPUT CURRENT OF THE HBM ESD GENERATOR AS SPECIFIED IN THE IEC 1000-4-2 STANDARD

TABLE 1. IEC 1000-4-2 SEVERITY LEVELS

LEVEL	TEST VOLTAGE, kV CONTACT DISCHARGE	TEST VOLTAGE, kV AIR DISCHARGE
1	2	2
2	4	4
3	6	8
4	8	15

Normally, the circuit configuration of Figure 3 is the recommended way to protect ESD sensitive inputs which relates to the IEC 1000-4-2 definitions for equipment, systems, subsystems and peripherals. To determine the capability of ESD Protection Arrays to protect an active circuit, the ESD Protection Arrays were tested as single devices. Following the conditions of the IEC 1000-4-2 specification, both direct contact and air discharge ESD tests were performed.

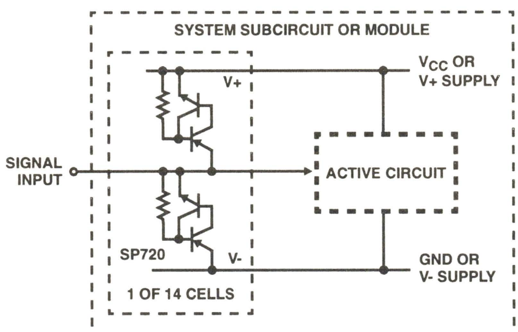


FIGURE 3. ONE PROTECTION CELL OF THE SP720 SHOWN AS PROTECTION INTERFACE ON A CIRCUIT MODULE

IEC 1000-4-2 ESD Test Evaluation

ESD Direct Contact and Air Discharge Capability

For V- = Ground, V+ = V_{CC} (varied) and T_A = 25°C, single pulse ESD testing was done at each pin of the SP720 and SP721. The results are shown in Tables 2A and 2B. In general, the SP720 and SP721 have the capability to withstand Level 2 direct contact ESD discharge for the test conditions defined in the IEC 1000-4-2 standard.

In Table 2C, all pins on six SP720 and four SP721 devices were tested for ESD Air Discharge Capability and passed without failures up to 16.5kV. This is better than the IEC 1000-4-2 standard to Level 4 severity requirements. The SP723 was tested using the same conditions given for the SP720 and SP721.

TABLE 2A. SP720 TESTS TO IEC 1000-4-2 STRESS LEVELS USING DIRECT CONTACT

STRESS LEVELS	(+) DIRECT CONTACT DISCHARGE VOLTAGE LEVELS TO EACH PIN	(-) DIRECT CONTACT DISCHARGE VOLTAGE LEVELS TO EACH PIN
V_{CC} = 0V, 5 Devices Tested		
1, 2, 3	All Pass	All Pass
4	All Pass	2 Fail
V_{CC} = 5.5V, 20 Devices Tested		
1, 2	All Pass	All Pass
3	All Pass	8 Fail
4	All Pass	Remaining 12 Fail
V_{CC} = 15V, 6 Devices Tested		
1, 2	All Pass	All Pass
3	All Pass	3 Fail
4	All Pass	Remaining 3 Fail

TABLE 2B. SP721 TESTS TO IEC 1000-4-2 STRESS LEVELS USING DIRECT CONTACT

STRESS LEVELS	(+) DIRECT CONTACT DISCHARGE VOLTAGE LEVELS TO EACH PIN	(-) DIRECT CONTACT DISCHARGE VOLTAGE LEVELS TO EACH PIN
V_{CC} = 5.5V, 20 Devices Tested		
1, 2	All Pass	All Pass
3	All Pass	8 Fail
4	All Pass	Remaining 12 Fail

TABLE 2C. SP720 AND SP721 TESTS TO IEC 1000-4-2 STRESS LEVELS USING AIR DISCHARGE

STRESS LEVELS	(+) AIR DISCHARGE VOLTAGE LEVELS TO EACH PIN	(-) AIR DISCHARGE VOLTAGE LEVELS TO EACH PIN
V_{CC} = 15V, 6 SP720, 4 SP721 Devices Tested		
1	All Pass	All Pass
2	All Pass	All Pass
3	All Pass	All Pass
4	All Pass	All Pass

The SP723 was tested using the same conditions given for the SP720 and SP721.

Table 2D shows the results for direct contact discharge and Table 2E show the SP723 capability for air discharge. Where each SP723 input has a dual input structure equal to the SP720 and SP721 which pass Level 4 air discharge conditions, the capability of the SP723 will exceed that by a wide margin but testing was not done due to test equipment limitations.

TABLE 2D. SP723 TESTS TO IEC 1000-4-2 STRESS LEVELS USING DIRECT DISCHARGE

STRESS LEVELS	(+) DIRECT DISCHARGE VOLTAGE LEVELS TO EACH PIN	(-) DIRECT DISCHARGE VOLTAGE LEVELS TO EACH PIN
V_{CC} = 15V, 8 Devices Tested		
1, 2, 3, 4	All Pass	All Pass

TABLE 2E. SP723 IEC 1000-4-2 STRESS LEVEL CAPABILITY USING AIR DISCHARGE

STRESS LEVELS	(+) AIR DISCHARGE VOLTAGE LEVELS TO EACH PIN	(-) AIR DISCHARGE VOLTAGE LEVELS TO EACH PIN
Results based on SP720, SP721 Data		
1, 2, 3, 4	All Pass	All Pass

Measured Peak Current in Direct Discharge ESD Testing

Verification for peak current calibration during testing for the ESD direct contact discharge was done for ESD Tests in Table 2. The measured peak currents occurs in 1ns and the 50% discharge occurs in 30ns as shown in Figure 2. The verified results as shown below in Table 3. These test levels conform to the IEC 1000-4-2 standard requirement for peak current to be within 10%.

TABLE 3. SP720 TESTS TO IEC 1000-4-2 VOLTAGE LEVELS

LEVEL	VOLTAGE	PEAK CURRENT 0.7ns TO 1ns RISE TIME, MEASURED	PEAK CURRENT 0.7ns TO 1ns RISE TIME, STANDARD
Level 1	+2kV -2kV	+7.5A -8A	7.5A
Level 2	+4kV -4kV	+15A -16A	15A
Level 3	+6kV -6kV	+22A -22A	22.5A
Level 4	+8kV -8kV	-	30A at 8kV
Level 4 plus 1kV	+9kV -9kV	+34A -34A	

The 9kV level was measured (instead of 8kV) to verify the extended range level of performance, which is the limit of the test equipment. A linear increase beyond the specified standard of 30A at 8kV would be equivalent to 33.75A at 9kV.

Multiple Pin Input ESD Test Evaluation

While the SP723 would be a preferred choice to extend the range of ESD protection, by using 2 or more IN input pins of the SP720 or SP721 also increases the range of ESD immunity. For example, by connecting adjacent SP720 pins in parallel using the dual pin combinations 1+2, 3+4, 5+6, 7+9, 10+11, 12+13 and 14+15, the IEC 1000-4-2 voltage capability is increased to better than ±9kV. (The ±9kV level is an equipment limited maximum voltage.)

Peak Current Capability

While the primary purpose of the SP720, SP721 and SP723 are for ESD protection, there is an implied need for surge current immunity in some circuit applications. As noted by the high peak currents recorded during ESD testing (Table 3), it can be expected that peak transient current capability rises sharply as the width of the current pulse narrows.

Destructive testing was done to fully evaluate device ability to withstand a wide range of peak current pulses vs time. The circuit used to generate current pulses is shown in Figure 4. The test circuit of Figure 4 is shown with a positive pulse input as it would apply to the SP720. For a negative pulse input, the (-) current pulse input goes to an SP720 'IN' input pin and the (+) current pulse input goes to the SP720 V- pin. The V+ to V- supply of the SP720 must be allowed to float. (i.e. It is not tied to the ground reference of the current pulse generator.)

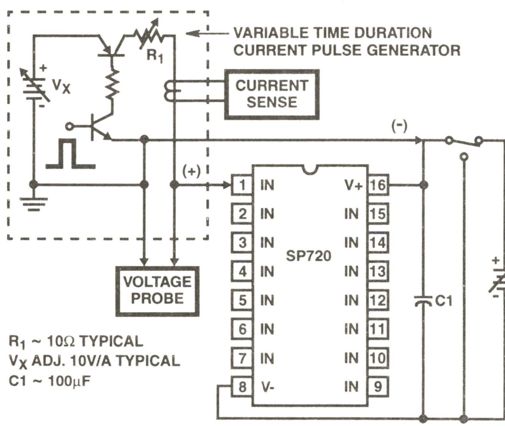


FIGURE 4. TYPICAL SP720 PEAK CURRENT TEST CIRCUIT WITH A VARIABLE PULSE WIDTH INPUT

Figure 5 shows a connected curve for each point of overstress as defined by increased leakage in the SP720 to well over the published limits of the data sheet. Using the similar connection test circuit configuration, the SP723 capability is shown on the same curve. The SP723 curve for a 15V supply shows a capability of 10A peak current for the 10µs pulse and 4A peak current for the 1ms pulse. The complete curve for a single pulse time up to 1 second is shown.

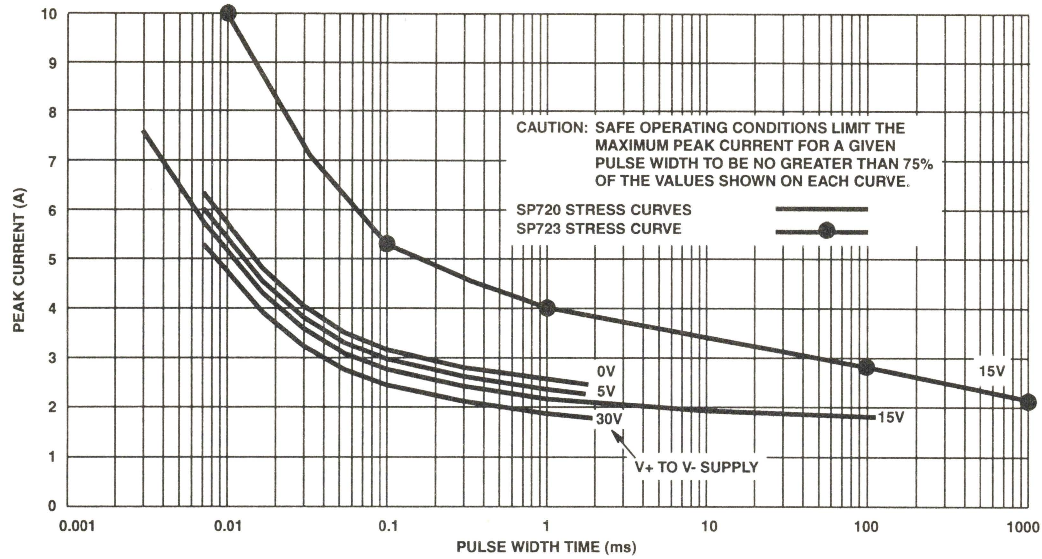


FIGURE 5. SP720 AND SP723 TYPICAL SINGLE PULSE PEAK CURRENT CURVES SHOWING THE MEASURED POINT OF OVER-STRESS IN AMPERES vs PULSE WIDTH TIME IN MILLISECONDS, ($T_A = 25^oC$)

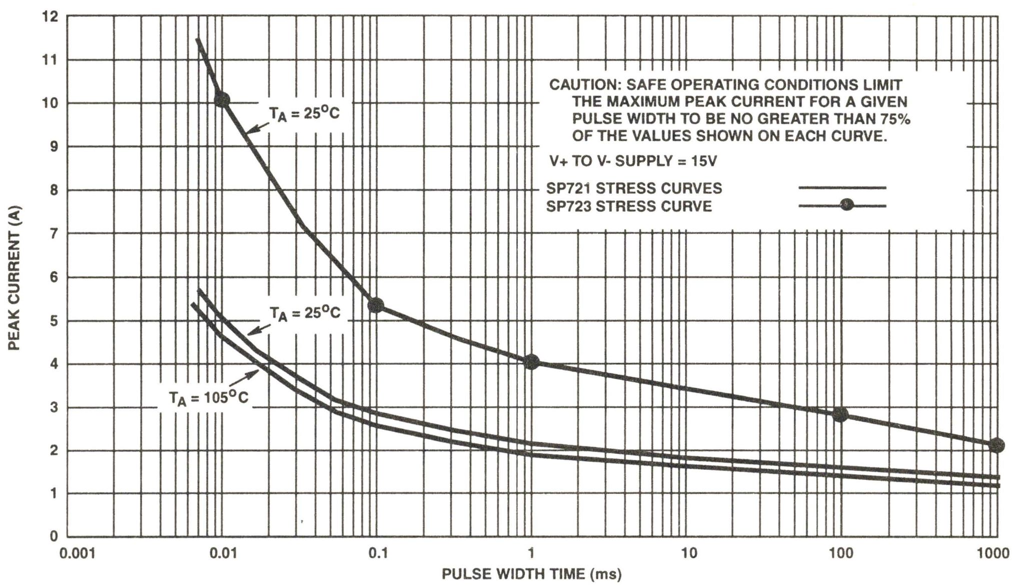


FIGURE 6. SP721 AND SP723 TYPICAL SINGLE PULSE PEAK CURRENT CURVES SHOWING THE MEASURED POINT OF OVER-STRESS IN AMPERES vs PULSE WIDTH TIME IN MILLISECONDS

Figure 6 shows the single pulse peak current capability of the SP721 for 105°C ambient temperature conditions. The SP721 is an 8 pin package version of the SP720 but is otherwise has the same short pulse width peak current capability. The SP721 curve for 25°C is shown for comparison. The reduction in maximum peak current attributed to an increase of ambient temperature from 25°C to 105°C is typically 10%. The overall effect of increased chip temperature, whether by ambient temperature increase or current induced dissipation, is to reduce the peak current ratings. The maximum rated operating ambient temperature for both the SP720 and SP721 is 105°C.

Multiple Pin Input Peak Current Test Evaluation

Uniformity of design and processing in the SP720 provides the capability to use multiple pins for added input protection. The very short pulse test capability for the dual pins is approximately twice the peak current for a single pin. However, for the 100ms to 1000ms pulses, the dual pin peak current stress capability decreases, approaching that of the single pin level. The longer pulse condition is limited by the heat capacity of the chip and eventually forces a more rapid increase in the chip temperature.

Other Transient Conditions

Conducted Susceptibility to Transients

Conducted Susceptibility to Transients is a test defined by the automotive SAE J1113 standard. The waveform used to test devices simulates the transient caused by a parallel or series inductive load when the supply current is switched off. Figure 7 illustrates the pulse waveforms generated by a Schaffner 5000 Transient Pulse Test Generator used to test the SP720. For the purposes of this test, Test Pulse 1 and 2 were applied while the V+ and V- voltage to the SP720 was at ground. Destructive level testing at room temperature was conducted with a single 200µs pulse while applying the transient signal to each IN input pin. It should be noted that the width for the 200µs pulse is defined for the 10% turn-on levels. The sourced voltage from the generator, V_S, was varied while the peak current was monitored.

Test Results for Single Pin Testing

Up to 10 consecutive pulses were applied at a 5 second rate to verify the transient capability of each input. It was determined that levels of +5.5A and -8A were sufficient to damage the inputs. Peak current levels of +5A (+6.5V) and -7A (-6V) were found to be a marginal safe level for single pulses applied to the IN inputs.

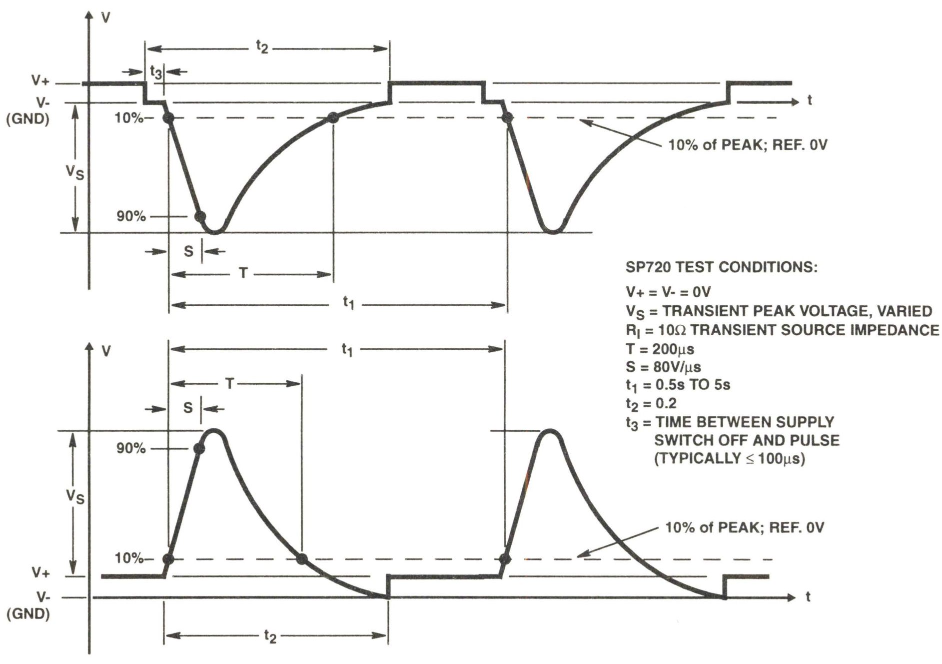


FIGURE 7. TRANSIENT INDUCTIVE DISCHARGE VOLTAGE vs TIME WAVEFORMS APPLIED TO THE SP720 INPUT 'IN' PINS. THE TOP WAVEFORM IS APPLIED FOR THE A DUT IN PARALLEL WITH AN INDUCTIVE LOAD AND THE BOTTOM WAVEFORM IS APPLIED FOR SERIES CONNECTED POWER TURN-OFF (REF. SAE J1113 STANDARD)

Test Results for Double Pin Testing

It was determined that paralleling input pins will permit twice the single pin current capability. Sustained testing at a 2Hz rate was done after paralleling pins 1+2, 3+5 and 6+7. The results for a +10A, 200µs positive transient current pulse were:

PINS IN PARALLEL	1+2	3+5	6+7	
Device 2 Failed at	-	3500	5600	Pulses
Device 3 Failed at	1150	230	340	Pulses

Sustained safe peak current levels should be no more than 70% of the point of overstress. At higher ambient temperature up to the maximum rated conditions of 105°C, the allowed maximum peak current should be further reduced by at least 10%.

SP720 and SP723 Surge Immunity Test Capability per the 8/20µs Short Circuit Conditions of IEC 1000-4-5

While the IEC 1000-4-5 is a standard that generally implies higher levels of power than recommended for the SP720 and SP723, testing was done to determine the comparable level of capability. The test circuit conditions for an 8/20µs short circuit current pulse are shown in Figures 8A and 8B. It should be noted that the 8/20µs pulse is defined as 20µs wide from a delayed turn-on to a 50% turn-off.

SP720 Test Results: The short circuit current marginal point of overstress at room temperature was determined to be:

For +IN Positive Surge Polarity (upper unit):

V_{CC} = 6V	Typically greater than 5A
V_{CC} = 15V	Typically greater than 4.8A
V_{CC} = 35V	Typically greater than 4.2A

For -IN Negative Surge Polarity (lower unit):

V_{CC} = 15V	Typically greater than 5.8A
V_{CC} = 35V	Typically greater than 5.8A

As previously noted, paralleling pins on the SP720 will increase the current capability to approximately twice that of a single IN pin.

SP723 Test Results: The short circuit current marginal point of overstress at room temperature was determined to be: .

For +IN Positive Surge Polarity (upper unit):

V_{CC} = 6V	Typically greater than 9.8A
V_{CC} = 15V	Typically greater than 9.5A
V_{CC} = 35V	Typically greater than 9A

For -IN Negative Surge Polarity (lower unit):

V_{CC} = 6V	Typically greater than 11.7A
V_{CC} = 15V	Typically greater than 11.1A
V_{CC} = 35V	Typically greater than 10.6A

As previously noted, sustained safe peak current levels should be no more than 70% of the point of overstress. At higher ambient temperature up to the maximum rated conditions of 105°C, the allowed maximum peak current should be further reduced by at least 10%.

R_C CHARGING RESISTOR
C_C ENERGY STORAGE CAPACITOR
R_{S1}, R_{S2} PULSE SHAPING RESISTORS
L_R RISETIME SHAPING INDUCTOR

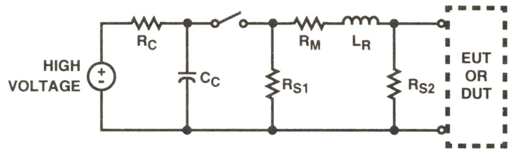


FIGURE 8A. CIRCUIT DIAGRAM OF GENERATOR FOR 8/20µs PULSE WAVEFORM

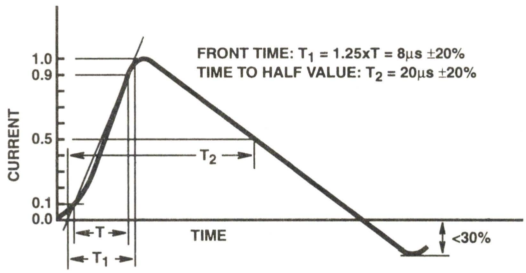


FIGURE 8B. WAVE SHAPE FOR 8/20µs SHORT CIRCUIT CURRENT PULSE PER IEC 60-1

Harris Semiconductor

APPNOTE

No. AN9671.1 January 1998

Harris Suppression Products

The ABCs of Harris Multilayer Suppressors

Author: Don Tidey

Introduction

This guide is similar to "The ABCs of MOVs", offering specific information on Multilayer suppressor device technology and is intended to be a supplement to the Harris Multilayer data sheets.

"A" is for Applications, giving general examples of where these products are used.

"B" is for Basics, describing the fundamental fabrication, operation and functions.

"C" is for Common Questions, addressing frequently asked questions from Production Engineers, and Designers.

There are a number of sources from which literature may be received. To learn more about Multilayer Suppressors:

- Call the Harris Central Applications group at 1-800-4-HARRIS in the U.S. (407-727-9207 outside the U.S.) or, EMAIL centapp@harris.com
- Call the Harris AnswerFAX system (1-407-724-7800)
- Visit the Internet at www.semi.harris.com

Applications

As with MOVs, Harris Multilayer Suppressors protect a broad range of applications and circuit components. They are offered in different designs to accommodate different suppression requirements. For an initial determination of which type is suitable, it is desirable to know:

1. The working voltage or maximum system voltage.
2. The type of transient that is to be suppressed and its energy level.
3. What circuit or component requires protection and, therefore, to what level must the transient be suppressed.

Multilayer Suppressors are most often applied to low voltage (<50VDC) systems on power supply, signal, or control lines in order to suppress ESD, EFT, Surge, or other transients at the circuit board level for component protection. Additionally, these devices may be applied to products subjected to immunity testing such as the EN61000 (IEC) standards in order to achieve specific electromagnetic compatibility (EMC) ratings.

The products and circuits to which these Multilayer Suppressors are applicable are diverse and include:

- Computers and their associated peripheral devices including I/O interfaces
- Office equipment such as keypad/controllers for copiers, facsimile and printers
- Automotive electronic modules
- Medical equipment such as electronic diagnostic instruments, monitors and recorders
- Communication devices including MODEMs, wireless LANs, Cellular phones/Cordless phones, Pagers
- Power supplies
- Microprocessor-based controls for machinery and robotics
- Opto isolator
- Sensors
- Portable/hand-held industrial instruments
- LASER diode devices
- Consumer electronics

Basics

Q. What is a Multilayer Suppressor?

A. A Harris Multilayer Suppressor is one of a family of transient voltage suppression devices. They bear similarity to Metal Oxide Varistors in that they are voltage dependent, non-linear devices that exhibit a bidirectional clamping characteristic and are based on a Zinc Oxide material technology. They are designed to suppress transients at the circuit board level in order to protect components and circuit functions by clamping the transient and dissipating its energy within the suppressor. These devices are ceramic and manufactured in leadless, surface mount form.

Q. What are the Device Families?

A. Since voltage transients have numerous sources and characteristics, Harris Multilayer Suppressors are offered in three separate Series.

The **"ML"** Series (data sheet #2461) supports the broadest range of applications with operating voltages from 3.5 to 120VDC and sizes of "0603", "0805", "1206", and "1210". This Series offers high peak current (8x20) ratings and is designed for board-level Surge, EFT, ESD and other specific transient events.

The **"AUML"** Series (data sheet #3387) is specifically characterized for Automotive-related parameters and transients. This Series has the single, 18VDC working voltage in sizes of "1210", "1812", and "2220", and affords module protection from secondary Load Dump and other transients found in the auto environment.

The **"MLE"** Series (data sheet #4263) is designed for lower energy transients and is rated for ESD suppression in order to protect sensitive components and, like the "ML", helps products meet Electromagnetic Compatibility test immunity standards. This Series is also specifically characterized for capacitance and impedance for combined suppressor/high frequency attenuation applications. MLE devices may be applied to circuits with a working voltage up to 18VDC and are offered in "0603", "0805", and "1206" sizes.

Q. How Are These Devices Fabricated?

A. Each of the three Series is fabricated by interleaving layers of a specific semiconducting dielectric material and metal electrodes which are alternately screened onto a substrate. The number of layers built and the dielectric material and thickness varies with the device type. This substrate is then divided into the individual devices which are sintered or "fired", forming a homogenous ceramic device. Metal end terminations are then applied and also fired, completing the basic operation.

Common Questions

Q. Is There Any Difference Between the ML, AUML, and MLE Series?

A. Yes. Generically they are the same, but they can differ from each other in terms of dielectric material formulation, layer count, sizes offered, electrical characterization/parameters, and ratings.

Q. Can Custom Voltage Parts Be Made for My Particular Application?

A. Yes. Harris can tailor the voltage rating of Multilayers by changing the dielectric material and/or thickness during fabrication. Also, by changing layer count, parameters such as Capacitance and Energy ratings can also be modified.

Q. How is the High Peak Surge Current Rating Achieved?

A. The internal, interleaved dielectric/electrode layers form essentially parallel devices so the effective surface area is much larger than the Multilayer size would suggest.

Q. Is There Any Plastic Used to Form the Package?

A. The ceramic construction forms the device itself. There is no encapsulation, plastic or otherwise, used in these devices.

Q. What Standard End Termination Materials are Used?

A. The standard termination is a fired-on Silver/Platinum alloy. Optional Silver/Palladium or Nickel/Tin versions are also available. To designate either, a character in the model number is added or deleted as shown in the associated data sheet under ordering information.

Q. Why are Different End Terminations Offered?

A. In order to best match specific soldering operations/requirements. Generally, the standard Silver/Platinum finish is used for reflow methods. The optional Silver/Palladium finish is recommended for wave solder methods in order to improve leach resistance. The Nickel/Tin finish may be used in either reflow or wave soldering operations.

Q. What are the Advantages of the Nickel/Tin End Termination?

A. The resistance to leaching during soldering is greatly enhanced with the Nickel/Tin finish. This permits flexibility in the design and control of the solder process. Secondly, the match to Tin/Lead solders improves wetting and fillet height. Also, the Nickel/Tin finish permits usage in those applications that restrict silver terminals.

Q. Does Harris Have a Recommended Solder Procedure?

A. Harris Multilayer devices are compatible with typical industry standard reflow and solder wave methods. Specific solder profile recommendations can be found in the Harris ML or MLE data sheets.

Q. What is the Capacitance of Multilayers?

A. Generally speaking, the range of capacitance for Multilayers is from less than 100 Picofarads to a few thousand Picofarads and inversely proportional to the working voltage. Dielectric type and thickness, number of layers, and device size all contribute in determining the capacitance. Capacitance, therefore, can be tailored by changing these variables.

Q. How Do the Multilayer Series Differ From the Harris CH Series?

A. The CH Series is fabricated from a single layer of MOV material. It is supplied in a single, larger chip size of 5mm x 8mm (3220) and has a higher voltage range up to 369VDC.

Q. Can the Harris ML Series Replace a Zener?

A. Harris Multilayers are often used to replace TVSS Zener diodes. Because the technologies and form factors differ, a direct cross reference is not practical. Contact Harris to help compare parameters and determine if a Multilayer can be used in the application.

Q. Do Multilayers Provide Bidirectional Clamping Like MOVs?

A. Yes. Multilayers provide suppression of transients of either polarity.

Q. Are Multilayer Suppressors 100% Tested?

A. Yes. All Multilayer Suppressors receive a final 100% electrical test for Nominal Voltage and Leakage at the Tape and Reel packaging operation.

Q. What Information is Contained in the ML or MLE Model Number Sequence?

A. Using the V18MLA0805L as an example:

V	The Multilayer maintains the Harris MOV "V" (Varistor) designation for Transient Suppressors.
18	The maximum DC working voltage
ML	The Multilayer Series
A	Performance or application designator
0805	The EIA size for length and width. (80mils x 50mils in this case)
L	Low Capacitance version (reduced layer count version in this case)

Q. Will This Part Number Vary When Placing An Order?

A. Yes. A suffix is added to identify the desired packaging (bulk or reeled) or end termination options. See the Harris data sheet for instructions. Additionally, a custom part will have an X suffix followed by a unique 4 digit designation.

Q. What is the Procedure in Selecting a Multilayer?

A. The basic procedure is to:

1. Determine the working voltage of the circuit in which the ML is to be placed and select an ML with equal or greater $V_{(DC)}$ MAX.
2. Determine what transient needs to be suppressed in terms of its type, peak surge current and energy in order to select the appropriate Series and device size.
3. Determine the maximum acceptable clamping voltage (or sensitivity level) of the components to be protected and review the V-I characteristics curves of the particular ML.
4. Other things to consider are the bidirectional clamping and typical capacitance of the ML.

Q. Are The Multilayers Subject To Listing By Safety Organizations?

A. Since the intended usage is in low voltage applications and not AC line or high voltage circuits, no listings are required. Likewise, since these devices are ceramic and not plastic, flammability ratings are not applicable.

Q. What ESD Level is the MLE Rated For?

A. The MLE is rated to the highest ESD voltage level categories of the IEC-1000-4-2 (human body model) specification. These are the 15kV (air discharge) and the 8kV (direct contact) methods. The IEC specification is a test method used to determine a given level of ESD immunity for EMC (Electromagnetic Compatibility) ratings of end products or systems. The MLE Series is used to suppress this ESD transient, thereby allowing products to meet EMC criteria.

Q. Why is the MLE Characterized for Impedance?

A. While operating in their normal standby mode, the inherent capacitance of all MLs help attenuate unwanted noise signals or harmonic frequencies. The MLE is additionally characterized for impedance since the low voltage circuits to which this Series is intended for use may be particularly sensitive to noise or require filtering of power supply lines, for example.

Q. Is Clamping Performance Derated Over Temperature for Multilayers?

A. No. Clamping voltage, peak current and energy are not derated over the entire temperature range, -55°C to 125°C ambient.

Q. Are These Devices Marked or Branded?

A. No. At the present time part designation is identified on packaging/shipping labels, including bar coding, where applicable.

Q. Where can Multilayers Typically be Placed in Circuits?

A. As a Clamping-Type Suppressor, the Multilayer is usually placed between the circuit point subject to transients and the reference electrical "Ground" or "Common", as close as practical to the transient source. Board level connections include:

- Across Switching Transistors
- Across Inductive Loads such as Relays or Solenoids
- On Local DC Power Supply Lines, Replacing Zener or Zener/Capacitor Combinations
- The Data Lines or Control Lines of ICs to Ground
- Across Remote Sensors
- On High Side or Low Side Drivers
- Bus Transceiver I/O Lines to Ground
- Across Laser Diodes
- Transistor Base or Gate Terminals to Ground
- Op Amp Input or Output Terminals to Ground
- On Interface Terminals or Connectors Subject to Human Contact or Conducted Transients

Harris Semiconductor

APPNOTE

No. AN9708 March 1997

Harris Intelligent Power

SP720, SP721 and SP723 Turn-On and Turn-Off Characteristics

Author: Wayne Austin

Introduction

The purpose of this Application Note is to focus on customer concerns related to the fast switching characteristics of the SP720, SP721 and SP723 family of protection ICs during an ESD discharge. The SCR cell structures of this family were first introduced for ESD protection of sensitive ICs that were subject to substantially more severe conditions than normal Human Body Model stress. The primary ESD protection requirement of the SCR structure is to absorb and divert energy away from the signal interface of sensitive circuits. Shown in Figure 1, each active input has a pair of SCRs to provide dual polarity protection directly in the signal interface.

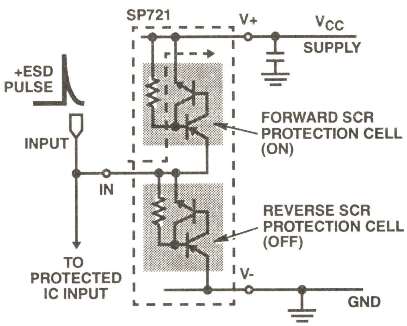


FIGURE 1. AN ILLUSTRATION OF SP721 ESD PROTECTION FOR A POSITIVE ESD PULSE, THE FORWARD SCR CELL CONDUCTS CURRENT TO THE V_{CC} SUPPLY

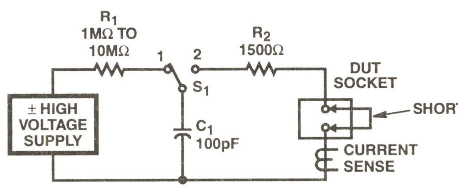
To meet the needs of a high performance application, a protection device must have a wide dynamic operating range with minimal loading. The SP720, SP721 and SP723 have a wide dynamic operating range of 35V with low input capacitance and low leakage while still providing the rugged level of protection necessary for most signal interface requirements. Low capacitance loading is essential for a fast ESD protection response time. The input capacitance of the SP720 and SP721 is typically 3pF and for the SP723 is 5pF. Each IN input has typically 5nA of leakage and the quiescent power supply current has 50nA of current.

The SCR cell structure was chosen for both a fast turn-on response and a low series resistance path to the high current of an ESD discharge. The SCR has a characteristic of decreasing resistance with increasing current, typically decreasing to 1Ω at 2A peak current. Positive and negative SCR cells are paired to work as active switches. The energy of an ESD discharge is both absorbed and shunted by the SCR to the supply line (positive pulse) or ground (negative pulse). When the energy is dissipated, the SCR quickly returns to its off state because there is no current to sustain the latched holding condition of the SCR.

Turn-On Time of the SP721AP

Figure 1 shows the paired SCR cell configuration of the SP721 with an illustration of how it responds to a positive ESD pulse applied to the input. The top or forward SCR cell responds to a positive ESD pulse and turns on when the voltage at the IN input is one V_{BE} greater than the voltage of the V+ terminal. ESD pulse current is conducted from the IN input to V+. The V+ of the SP721 is common to the V_{CC} power supply line of the IC being protected. The SCR begins to conduct in ~0.7ns and has a typical turn-on delay time of 2ns.

To illustrate the turn-on characteristic and speed of the SCR, Figure 2 shows the Human Body Model ESD pulse simulator per MIL-STD-883D, Method 3015.7. This circuit discharges a 100pF capacitor through 1500Ω to a device under test (DUT). The waveform Turn-ON characteristic for current vs. time of an SP721 when activated by a +2kV ESD pulse is shown in Figure 3. The SP720, SP721 and SP723 have the same cell design and turn-on characteristic.



SWITCH S_1 IN POSITION 1 CHARGES CAPACITOR C_1. WHEN S_1 IS SWITCHED TO POSITION 2, CAPACITOR C_1 DISCHARGES INTO R_1 AND THE DEVICE UNDER TEST (DUT). THE DUT SOCKET IS SHORTED PIN-TO-PIN FOR SIMULATOR WAVEFORM VERIFICATION. AN OSCILLOSCOPE CURRENT PROBE IS USED TO SENSE THE DISCHARGE CURRENT WAVEFORM.

FIGURE 2. MIL-STD-883D, METHOD 3015.7 ESD TEST CIRCUIT SHOWING THE CURRENT WAVEFORM VERIFICATION SETUP FOR THE HBM TEST FIXTURE

11

APPLICATION NOTES

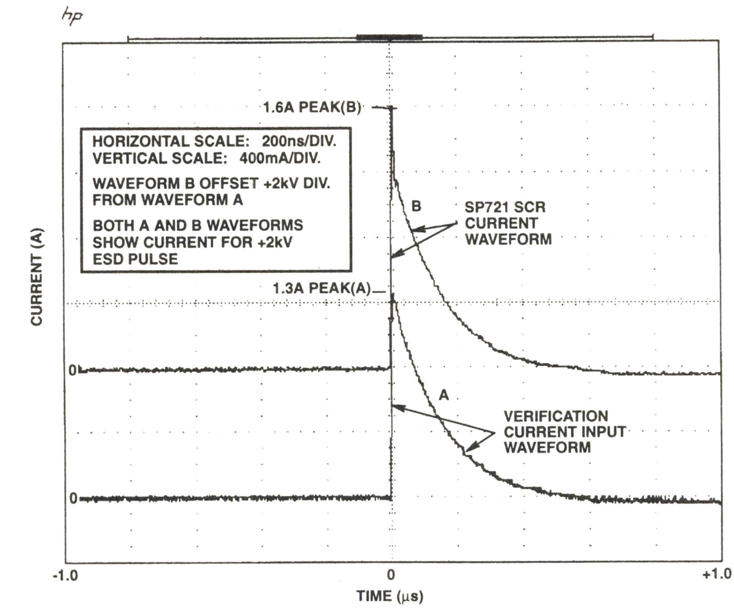


FIGURE 3A.

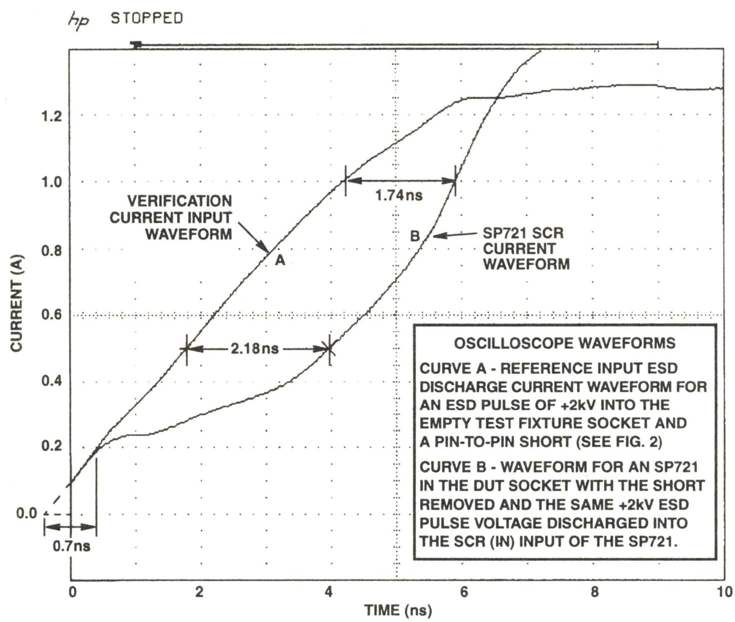


FIGURE 3B.

FIGURE 3. OSCILLOSCOPE WAVEFORMS SHOWING CURRENT vs TIME FOR THE MIL-STD-883D, METHOD 3015.7 TEST CIRCUIT OF FIGURE 2. FIGURE 3A IS A FULL SCALE OF ESD DISCHARGE TIME AS SHOWN ON A HP54540A DIGITAL OSCILLOSCOPE. FIGURE 3B SHOWS AN EXPANDED VIEW WITH AN OVERLAY OF THE REFERENCE OR SHORTED FIXTURE WAVEFORM "A" FOR VERIFICATION (CALIBRATION) AND WAVEFORM "B" AS THE SCR TURN-ON AND DELAY TIME RESPONSE. THE SCR TURN-ON DELAY TIME IS TYPICALLY 2ns

Figure 3 shows waveforms of switching time vs current for the SP721. The top display is a full scale view of an SP721 ESD discharge waveform vs a reference short circuit (calibration) discharge waveform for the test fixture of Figure 2. The bottom display is an expanded view for both curves with the same zero reference for the SP721 turn-on waveform "B" vs the input reference waveform "A". (The zero baselines of both waveforms are initially offset 0.35ns by the threshold of the scope trigger level.) The turn-on delay of the SP721 SCR increases to just over 2ns from the reference input waveform "A" and then drops back to less than 2ns.

The 1500Ω of the standard test circuit should allow an initial peak current of 1.33A when the capacitor C_1 charge is 2kV. Current through the SP721 peaks at 1.6A and is then quickly damped. Lead inductance and stray capacitance at the input causes some transient ringing and overshoot. After a few nanoseconds of ringing, the fall time of the SP721 current waveform "B" (shown in the top display) is identical to the reference waveform "A".

Speed vs ESD Rated Capability

For any application, the maximum rated ESD capability is most desirable. However, this is a trade-off with performance related parameters such frequency (Mb or MHz), static or dynamic impedance and stability. The SP720, SP721 and SP723 offer an optimal trade-off, having high HBM ESD voltage capability to both MIL-STD-883 and IEC 1000-4-2 standards with very low capacitance and are designed to work in the signal interface to protect sensitive ICs. Many competitive ESD protection products have high capacitance and can only be used for power supply or power line protection.

SCR Structure vs a Zener Device

What is the advantage of the SCR over a Zener diode? While it is relative simple to suggest that Zener diode may offer more capability, increasing area for improved ESD ratings increases the capacitance of the Zener junction. When a Zener becomes active, dissipation at the junction is the Zener voltage times the current. When the SCR structure becomes active, it latches on with low resistance and low internal dissipation.

SCR Unlatch Speed

The SCR quickly unlatches when the current drops to zero. Figure 3A shows the full waveform for turn-on and turn-off time. The SP721 waveform "B" closely follows the reference input waveform "A". Delay in the SCR turn-off is not significantly longer than the disruptive period of the simulated ESD pulse.

Latch

It should be noted that "latch" as referenced in the turn-on of the SCR has no relation to latching input problems that were common in older CMOS devices and may occasionally occur as an irregularity in other processes. The SCR cells are designed to latch on with a disruptive signal that is greater than the supply voltage (V+) or less than ground (V-). The SCR falls out of latch when input voltage returns to a normal mode of operation.

How Best to Protect a CMOS IC Input

Figure 4 illustrates an SP720, SP721 or SP723 interface with a typical CMOS IC input circuit. This example shows a typical input for high speed CMOS which includes an internal series resistor R_P to stacked protection diodes, followed by a resistor and diode. R_P is typically an integral polysilicon resistor with a resistance of 120Ω and can be subjected to ESD damage for voltage levels higher than 2kV. Use of an SP720, SP721 or SP723 will substantially improve the signal line input against an ESD discharge.

While the conducting SCR will clamp an ESD pulse, the discharge current will cause some ride-up of the voltage on the signal input line. For example, an HBM ESD discharge of

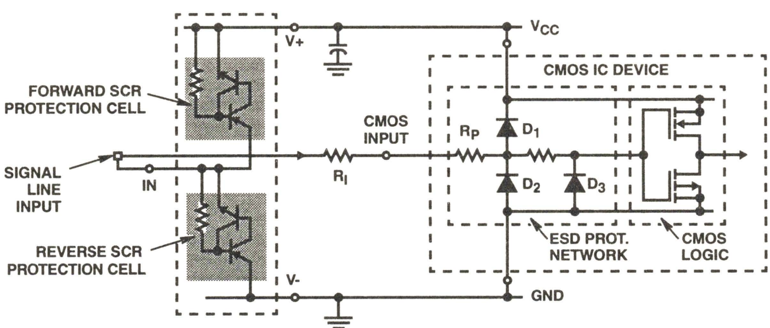


FIGURE 4. SP720, SP721 OR SP723 SCR INTERFACE TO A CMOS INPUT WITH R_I ADDED TO ILLUSTRATE MORE EFFECTIVE ESD PROTECTION FOR CMOS DEVICES

+3kV (see Figure 2) will cause approximately 2A of current. With this positive input current, the input voltage will exceed the V_{CC} level and turn-on the forward SCR. The data sheet I-V curve indicates that the forward voltage drop of the SCR for 2A will be typically 3V. As such, it is recommended that a series resistor be used at the CMOS input (shown here as R_1). This will add resistance to limit current into the CMOS IC by forming a current divider with the latched-on SCR. Without R_1, diode D_1 would see a 3V forward turn-on or (3V - 0.7V)/(120) = 19.2mA. A typically HC CMOS should tolerate twice this level. However, an external resistor of 120Ω would further reduce the current by one-half. An IC with a 2kV rated input can be protected to 10kV or higher, depending on the CMOS internal network and resistor, R_1.

It is recommended to use the largest value of R_1 that is permitted, consistent with the trade-off in circuit performance. In layout, it is also recommended to keep the signal line input layout as short as possible to minimize ringing and transients caused by stray inductance and capacitance.

No. AN9730 January 1998

Harris Suppression Products

Basic Construction and Theory of Gas Discharge Tubes

Construction

Gas Discharge Tube (GDT) surge arresters commonly employ hermetically-sealed enclosures utilizing either ceramic-to-metal or glass-to-metal seals. The many advantages of ceramic-to-metal units have made them the norm for gas discharge tube surge arresters such as Harris GDTs. Along with being low cost, they offer high product uniformity capable of handling extreme levels of shock, vibration, and temperature.

The ceramic for GDTs is alumina ranging from 94-98% Al_2O_3. The ceramic-to-metal seals are prepared by moly-manganese or tungsten metallizing processes with nickel plating and the final seal is made in a gas-filled vacuum furnace using braze preforms made of copper-silver eutectic. The electrodes used for GDTs are either copper or a nickel-iron alloy, often with a coating to lower the work function and/or add gettering capability. Stripes or bands of semiconductive material are applied to the inner surfaces of the ceramic to improve stability and high-speed response.

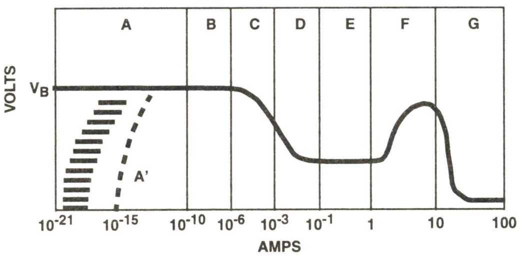


FIGURE 1. HARRIS PLASMA ARRESTER TYPICAL OPERATING CHARACTERISTICS

Theory

The basic operation of gas tube surge arrestors is best understood by referring to the schematic form of the voltage-current (V-I) relationship of a generic gas discharge device such as the one depicted in Figure 1.

Description of Regions of a Generic V-I Characteristic of a Plasma Device

A For voltages below the breakdown voltage, the gas provides a good insulator. Very low leakage currents (10-12A) occasionally encountered result from ionization by cosmic rays, high energy photons, etc; and is, therefore, subject to statistical fluctuations.

A' The current is higher due to supplementary electron sources such as photoemission.

B The discharge is self-sustaining due to gas ionization -- if external agents such as those mentioned for regions A and A' are removed, the current will not change (Townsend discharge). This occurs at the breakdown voltage of the device.

C The transition region. As the electric field increases, more secondary electrons are generated, decreasing the voltage drop until the glow voltage (region D) is reached. Stable operation can only be maintained with active current regulation because of the negative slope of the V-I characteristic.

D The glow region (or normal glow region). In this region, the glow voltage is roughly constant with respect to small changes in current.

E The abnormal glow region. In contrast to the normal glow region, the glow voltage begins to increase as the current is increased.

F The glow-to-arc transition region.

G The arc region. In this region, the arc voltage will quickly drop and the arc current will quickly increase within the limitations of the drive energy and impedance.

If the current through the gas discharge device is adjusted over the range of values of 10-18 to 102 amps, the voltage across the device will also vary. When a gas discharge device is operated as a transient voltage protector, the modes of operation of greatest significance are in regions A, F, and G. The applied voltage is normally less than the breakdown voltage of the device, V_{BD}, at which time the current through the device is in the A region. The charged carriers of electric current in this mode originate from the cathode by photon emission and within the fill gas by collisions of gas particles with cosmic rays (or radioactive decay particles if an isotope is used in the device).

As soon as the applied voltage across the device exceeds the breakdown voltage, the current through the device increases rapidly to values of several amps or greater. The rate of current rise and the level reached is limited by the source capacity and the series impedance of the circuit. The voltage across the device at this time is very low with typical values of 20V or less.

APPNOTE

No. AN9731 October 1997

Harris Suppression Products

Surge Protection of Main Distribution Frame Using GDTs

Introduction

Transient voltages induced in the telecommunication cable network can cause considerable damage to main distribution frame and telecommunication equipment. Effective surge protection can avoid expensive repair work and improve product reliability.

This note describes the possible transient sources which can occur on the telecommunication network and how to take preventive protective measures on the main distribution frame, based on tests and practical experience.

Modern telephone systems are fast, efficient, and complex. Many developments have been made in control office equipment which involve solid state circuitry.

Unfortunately, solid state devices are much more susceptible to malfunction or failure due to transient voltages. In addition, the increased usage of telephone lines for data transmission has produced a further intolerance for transient voltages.

Telephone networks, having a wide cable distribution, are highly exposed to voltage transients and therefore require protection components with maximum power capability, long life and high reliability.

For these reasons gas discharge tube (GDT) surge arrestors find an increasing use as the primary protector in telephone systems, replacing older types of protectors (air gaps, carbon blocs) and being designed into nearly all new and future equipment systems.

Causes and Effects of Transients on Telephone Equipment

Direct Lightning Strike

The earth's surface continuously experiences electrical disturbance activities. The extent of this activity is significant as it is estimated that 100 lightning flashes strike the earth every second. It is therefore not surprising that lightning is the most common source of overvoltage surges in communication systems.

The effects of a direct lightning strike are devastating. It has been estimated that the energy dissipation per unit length of channel in a single lightning stroke is 100KJ/m. The average length of a lightning stroke is 3km. The average duration of a stroke is 30µs with 4 strokes per lightning. Therefore, the peak power per stroke is 1×10^{13}W.

The destructive power of lightning arises from high pressure generated in the lightning channel. In open air, energy deposited by a single stroke is equivalent to approximately 22g of TNT per meter, or 1/10 ton of TNT for the average channel. Most of this energy, however, is converted along the lightning channel leaving only a fraction of it at the end of the channel.

Four lightning parameters have to be considered when studying the effects of direct lightning strikes:

- Current amplitude (I): responsible for ohmic voltage drop in earth ground resistance.
- Steepness of the lightning current rise (di/dt): determines inductive voltage drops.
- Electric charge ($\int i dt$): is a measure of the energy transmitted by the lightning arc to metallic surfaces, causing melting effects.
- Current square impulse ($\int i^2 dt$): is at the base of every mechanical effect and electrical impulse heating of ohmic resistors.

TABLE 1. LIGHTNING PARAMETERS

Percent of Strokes	90%	50%	10%
Crest Current (i)	2kA to 8kA	10kA to 25kA	40kA to 300kA
Rate of Current Rinse (di/dt)	2kA/µs	8kA/µs	20-300kA/µs
Duration of Single Pulse	100µs to 600µs	0.5ms to 3ms	20ms to 400ms
Total Stroke Duration	10ms to 100ms	100ms to 300ms	0.5s to 1.5s
Number of Pulses per Stroke	1-2	2-4	5-34

Indirect lightning

The most noticeable and frequent interference in telephone systems is due to the inductive effect of lightning strikes. Although the induced effect of lightning is more common on overhead lines, buried lines are still susceptible through resistive coupling.

Overvoltages, mostly induced by cloud-to-cloud discharges, can be as high as several kilovolts with kiloamperes short circuit current. The surge voltage that appears at the end of the cable depends on the distance to the source, the type of cable, the shield material, and its thickness and insulation, along with the amplitude and waveshape of the lightning current in the shield.

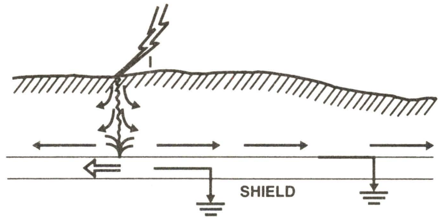


FIGURE 1. INDIRECT LIGHTNING IN BURIED CABLES

Power System Induced Transients

Overhead telephone lines often share a utility pole and ground wire with the commercial AC power system. Buried telephone and power cables often share the same trench. Because of this, three types of overvoltage transients induced into the telephone lines can occur in conjunction with power system faults.

- Power contact or power cross: power lines make direct contact with telephone cables.
- Power induction: electromagnetic coupling of a heavy fault in the power system (this can be solved with proper shielding).
- Ground potential rise: heavy ground currents of power system faults flow in the common ground connections and cause substantial differences in potential.

Engineers have defined the power cross situation as the most severe condition. Therefore, the many requirements call for the suppression device to withstand $10A_{RMS}$ for a duration ranging from 10 to 60 cycles of the power system frequency.

Protection of Main Distribution Frame

The telephone system is made up of a central switching network which interconnects the different subscribers through repeaters, multiplexers, and concentrators. The cable network which links the subscribers makes the system vulnerable to damaging transients. The cables consist of conductors in shielded cables, which are suspended on poles or buried in earth.

Along with the cable network, antennas on wireless equipment connected to the telephone system are also a potential source of transients to the network. Additionally, the power used by a telecom system is usually obtained from commercial power lines which are subjected to the same possible overvoltage surges as the telephone signal lines.

As one can see, the complexity and exposure of the telephone system makes it highly susceptible to all types of overvoltage transients. From a practical standpoint, however, the cost of installing and maintaining a 100% protection system would not be cost effective. Therefore, network planners usually develop a location's network protection level plan based upon the implementation cost, stroke factor, ground resistance, type of facilities, desired reliability of service, and the exposure to lightning.

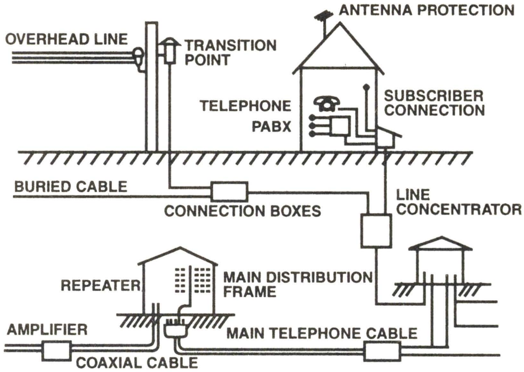


FIGURE 2. TELECOMMUNICATION NETWORK

The main distribution frame (MDF) (Figure 3) is the link between the cables coming from anywhere in a local telephone network and the cable coming from the exchange switching equipment. The MDF rack consists of tubular and angular rails for the various MDF devices to be attached. On the line side (mostly accommodated on vertically rails), local cables are terminated. On the exchange side, horizontal arranged terminal blocs are connected to the exchange switches. An overvoltage protection magazine installed on the line side protects the exchange switching equipment against harmful overvoltage transients when connected to the external cable network.

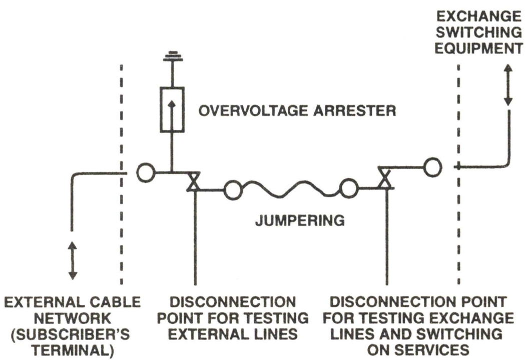


FIGURE 3. MAIN DISTRIBUTION FRAME

Protecting the MDF with GDTs

Of the devices available for transient protection, the gas discharge tube (GDT) reliably offers the highest surge current dissipation that is required to protect against lightning. GDT devices are unique in their ability to handle transient currents many times beyond the capability of solid state devices.

In the presence of a fast rising voltage surge, the GDT crowbars (switches) from its normally high impedance state to short circuit the transient safely to ground. Once in their fired state, GDT surge arrestors act like low voltage clamping devices (10V-20V) whose clamping voltage is essentially independent

of the transient's current magnitude. In the non-operating mode, the GDT surge arrestors are essentially transparent to the network's performance since they offer extremely high isolation resistance and very low line capacitance.

For these reasons the GDT arrester can be considered the best solution to provide the telephone network the primary protection against direct or induced high voltage transients.

Typical performance ratings of the GDT are:

- Environmental
  - Temperature . . . . -40 to 90°C
  - Relative Humidity . . . . up to 95%
- Electrical
  - DC Breakdown . . . . 250V nominal
  - Impulse Breakdown at 100V/µs . . . . 900V (Max)
  - Insulation Resistance . . . . >1000MΩ
  - Capacitance . . . . ≤5pF
  - Life Tests
    - Impulse 8/20, 10 events, 10kA peak
    - Impulse 10/1000, 300 events, 100A peak
    - AC, 15Hz-62Hz for 1s, 5 events, $10A_{RMS}$

In many situations, a fail safe system is specified on GDT devices so the line is permanently grounded after excessive heating of the surge arrester by a long duration power cross. If this situation occurs, the GDT device and fail safe mechanism must be replaced.

Two Electrode Configuration

GDTs are used in many telecommunication networks around the world for main distribution frame protection. Harris Semiconductor's GDTs are constructed of two metal electrodes hermetically sealed in a gas filled, rugged ceramic cylinder. Through ongoing research and engineering improvements, surge arrester families offer impressive characteristics for MDF protection.

The two electrode HG2 series can best be used where microsecond transient rise times are expected. They provide fast response time, high holdover voltage and high follow-on current capacity.

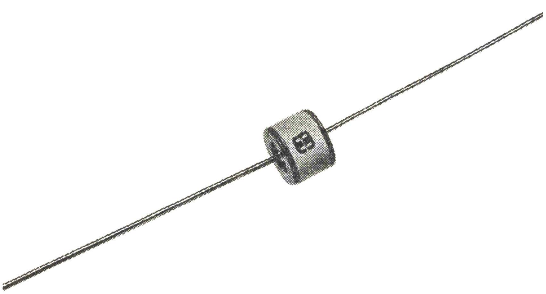


FIGURE 4. HARRIS' BIPOLAR GDTs

HG2-230L Performance

- Nominal DC Breakdown Voltage . . . . $230V_{DC}$
- Impulse Breakdown at 100V/ms . . . . 600V (Max)
- Insulation Resistance . . . . 1000MΩ (Min)
- Maximum Capacitance . . . . 1pF (Max)
- Surge Life
  - Impulse 8/20, 10kA, 10 events
  - Impulse 10/1000, 500A, 1000 events
  - AC, 15Hz-62Hz for 1s, 10 events, 20A $_{RMS}$.

Three Electrode Configuration

In a telephone cable, signals are conducted through pairs of copper wires. Therefore, transient voltages induced into the conductors will be common to both signal wires (typically called "tip" and "ring"). This is shown in Figure 5.

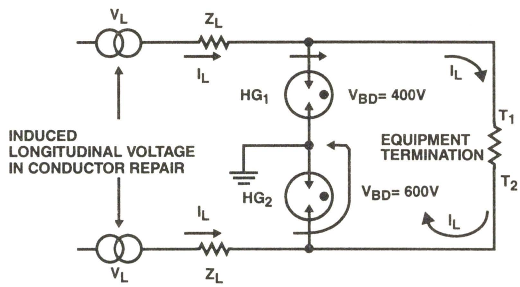


FIGURE 5. UNBALANCED LINE PROTECTION

If protector HG_1 should breakdown at 400V while HG_2 requires 600V to breakdown, the difference would cause a transient current to flow through the load. To eliminate the problem of unbalanced line breakdown, dual gap or three electrode tubes like the HPMT3 have been developed. See Figure 6.

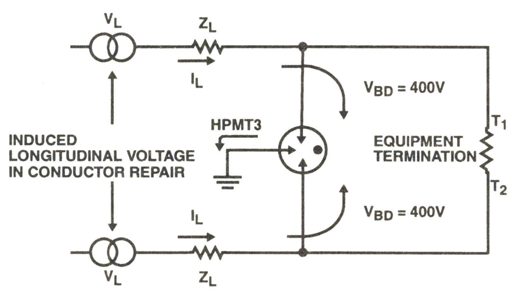


FIGURE 6. BALANCED LINE PROTECTION

The HPMT3 series from Harris are three electrode, medium duty surge arrestors designed to protect electronic equipment from damage due to excessive voltages and current. The HPMT3 products have extremely fast response times characterized by the impulse breakdown voltage, which

describes their dynamic behavior. For ease of mounting on PC boards, the devices are available in many different lead configurations.

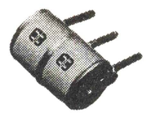


FIGURE 7. HARRIS' TRIPOLAR GDTs

HPMT3-23004 Performance

- Nominal DC Breakdown Voltage . . . . $230V_{DC}$
- Impulse Breakdown at 100V/ms 600V
- Insulation Resistance. . . . . 1000MΩ (Min)
- Maximum Capacitance . . . . .1pF (Max)
- Surge Life:
  - Impulse 8/20, 10kA per side, 20kA total
  - Impulse 10/1000, 500A, 400 events
  - AC, 15Hz-62Hz for 11 cycles, 65A

The voltage rating of the surge arrester is determined by the voltage applied between the tip and ring signal wires. Most telecommunication systems have $48V_{DC}$ with a super imposed ring voltage of $100V_{RMS}$ (154V peak) maximum which results in a minimum breakdown voltage of 202V. Therefore, the HPMT3-230 would be appropriate three electrode selections for this application.

Protection Verification

In actual field operation, surge arrester devices are subjected to transients which, by their nature, are unpredictable in magnitude and duration. In order to best simulate transients such as lightning, international committees have developed standard lightning wave shape tests which can be conducted to evaluate protection components. Figure 8 illustrates the standard characteristics of these wave slopes. Harris utilizes these recommendations and standards when specifying, qualifying, and testing our GDT devices.

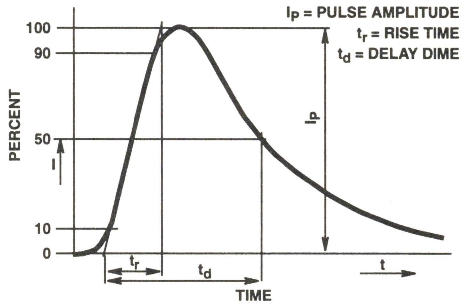


FIGURE 8. DESCRIPTION OF SURGE CURRENT

Maintenance of Protection Devices

Most components utilized in lightning protection systems degenerate gradually due to the effects of repetitive surge damage and weather exposure. Component deterioration can cause a loss of protection resulting in unexpected system damage as well as performance degradation in the power and signal circuits. Periodic maintenance will help insure that the protection system remains at its original design and installation performance capability. Unlike semiconductor devices, the deterioration of GDT protectors can easily be measured. A GDT's performance can gradually degenerate due to erosion of its metallic electrodes. The degeneration, which is a function of lightning stroke frequency and magnitude, may easily be detected by measuring a decreased insulation resistance value across the electrodes of the device.

Harris Semiconductor

APP NOTE

No. AN9732 October 1997

Harris Suppression Products

Combining GDTs and MOVs for Surge Protection of AC Power Lines

AC power line disturbances are the cause of many equipment failures. The damage can be as elusive as occasional data crashes or as dramatic as the destruction of a power supply, computer terminal, or television set. Power line disturbances go by many names -- transients, surges, spikes, glitches, etc. -- but regardless of the name, an understanding of their characteristics and the operation of the various protection devices available is necessary to design an effective protection circuit. This Application Note will illustrate how to design high-performance, cost-effective surge protection for equipment connected to AC power lines. The role of gas discharge tube (GDT) surge arresters specifically designed for AC power line protection will also be discussed.

The first step in providing an effective defense against power line transients is to accurately characterize the transients. One good reference is IEEE C62.41-1991 entitled "IEEE Recommended Practice on Surge Voltages in Low-Voltage AC Power Circuits" (formerly IEEE Standard 587). This standard defines the open circuit voltage and short circuit current waveforms which can be expected to occur on AC power lines of 1000 Volts (RMS) or less. The standard defines three levels of increasing transient activity, labeled Location Categories A through C, dependent on the distance of the equipment from the service entrance. Line cord-connected equipment will usually be covered by Location Category A or, occasionally, Location Category B. There are two standard waveforms which define the types of transients expected in these Location Categories:

- 0.5μs-100kHz Ring Wave (Figure 1A) — an oscillatory waveform having a peak open circuit voltage of up to 6kV (Note 1), a risetime of 0.5ms, a ring frequency of 100kHz, and a "Q" of three. Though a short-circuit current is not specified, peak currents of up to 0.5kA can be expected (Note 1).
- 1.2/50μs-8/20μs Combination Wave (Figure 1B) — a unidirectional impulse waveform having a peak open-circuit voltage of up to 6kV (Note 1) with a rise time of 1.2μs and a duration of 50μs (Note 2) AND a peak short-circuit current of up to 3kA (Note 1) with a rise time of 8μs and a duration of 20μs (Note 3).

Test waveforms for evaluation of a surge protection system should conform to these standard waveforms as closely as possible to ensure valid results. The use of test waveforms having slower rise times or lower peak currents/voltages may result in a false sense of security concerning the level of protection actually provided under field conditions.

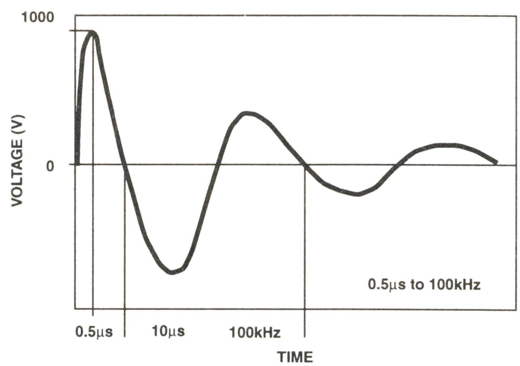


FIGURE 1A. IEEE-587 RING WAVE

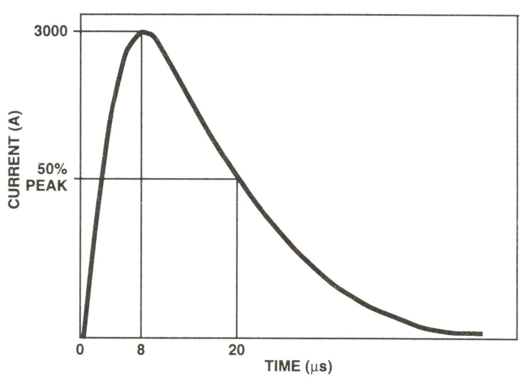


FIGURE 1B. IEEE-587 COMBINATION

The second step in designing an effective surge protection circuit is to choose which type(s) of surge protector to use. Surge protection devices can be divided into two basic types: Crowbar-type devices such as gas tube surge arresters, spark gaps, and SCRs; and Clamp-type devices such as avalanche diodes, transient absorption zener diodes, and metal oxide varistors.

The clamp-type devices have faster response times but are limited in their current handling ability because most of the energy of the transient must be dissipated by the clamping device. Also, the voltage drop across a clamp-type surge protector increases with the conducted current as shown in Figure 2A.

Crowbar-type devices such as gas tube surge arresters have slightly slower response times but can handle much higher current because they act as a low impedance switch which diverts the transient energy away from the protected equipment to be dissipated externally. While the peak voltage experienced by the protected circuit during the leading edge of some transients may be higher than with a clamp-type device; the duration, and thus the total energy delivered to the protected circuit, is much lower when using a crowbar-type device as shown in Figure 2B.

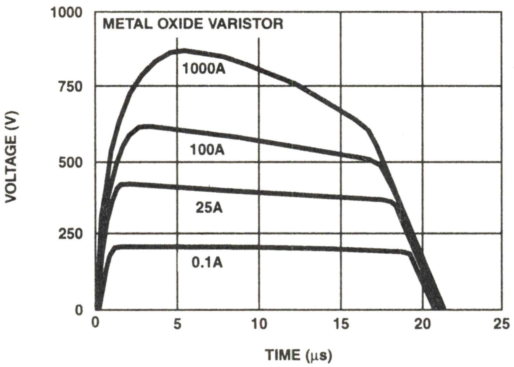


FIGURE 2A. MOV CLAMPING VOLTAGE AT VARIOUS CURRENT LEVELS

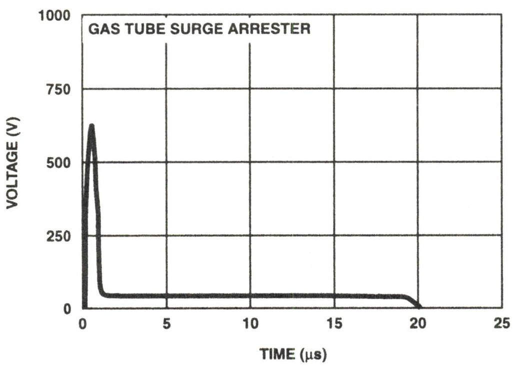


FIGURE 2B. TRANSIENT RESPONSE OF PLASMA SURGE ARRESTER

This peak voltage is a function of the rise time of the leading edge of the transient. Faster rise times will result in higher peak voltages due to the response time of the protector. Although Zener-gated SCRs and thyristors are available which offer faster response times, their use is limited to telecom and signal line applications due to their relatively low peak current ratings. A major benefit of the gas tube surge arrester is that the voltage drop across the device remains essentially constant (<20V) regardless of the conducted current.

The ideal surge protector would overcome the current handling and energy diverting characteristics of the crowbar type device with the speed of the clamp type device. This approach has been difficult and expensive to realize with traditional crowbar type devices because their designs were optimized for the ability to turn off in the presence of a low-current DC bias. While that is appropriate for protecting a telecom line, additional components (such as a series resistor or parallel-connected series-RC network) were required to ensure that the gas tube surge arrester would extinguish when placed across an AC power line with its relatively low source impedance and the resultant follow-on currents (Note 4). These components invariably decreased the performance of the protector while increasing its installed cost.

These shortcomings have been resolved with the Harris HAC series of gas tube surge arresters specifically designed for AC power line applications. These devices provide the low impedance switching action and high peak current capabilities of traditional gas tube surge arresters while optimizing the ability to extinguish in the presence of AC follow-on currents in excess of 300A. In most applications, no additional components are required other than those of the basic surge protection circuit. A surge protection circuit with sub-nanosecond response time, precise control of transient energy let-through, and a peak current rating of 20,000A is now practical even for cost-sensitive applications such as power supplies, home stereos, monitors, and printers.

A typical installation is illustrated in Figure 3A (next page). This is a two stage hybrid circuit consisting of a gas tube surge arrester as the primary protector and a Metal Oxide Varistor (MOV) as the secondary protector. These elements must be separated by an isolating impedance. This impedance may be either resistive (>10Ω) or inductive (>0.1mH) to ensure proper coordination of the protective devices. Most AC applications utilize an inductive element to minimize power dissipation and voltage drop during normal operation.

The inductor used in this example is part of the RFI filter already required by the design. The output of the protection circuit during a transient is illustrated in Figure 3B.

The following sequence of events is depicted in Figure 3B:

A. The leading edge of the transient is clamped by the MOV to a value just above the normal operating voltage.

B. As the current through the MOV increases, a voltage is developed across the inductor which causes the gas tube surge arrester to fire. The energy of the transient is now quickly shunted through the gas tube surge arrester and away from the protected circuit.

C. The gas tube surge arrester remains in full conduction for the duration of the transient.

D. When the transient has passed, the gas tube surge arrester extinguishes—ready for the next transient.

This circuit uses each component to do what each does best: the gas tube surge arrester diverts the high-energy portion of the transient and the MOV provides the fast, accurate clamping of the low energy leading edge.

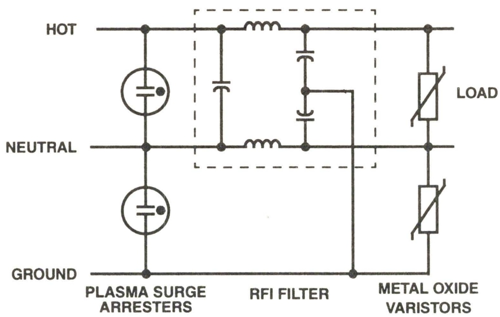


FIGURE 3A. HYBRID SURGE PROTECTION CIRCUIT

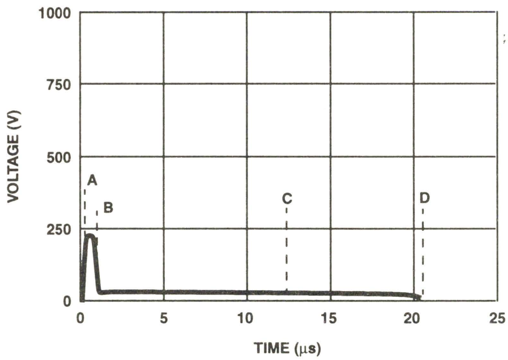


FIGURE 3B. TRANSIENT RESPONSE OF HYBRID CIRCUIT

The cost effectiveness of this protection circuit is enhanced by three factors:

1. The use of an HAC Series gas tube surge arrester eliminates the need for additional components to ensure turn-off.
2. The isolating impedance is supplied by an existing component (the RFI filter).
3. A small diameter MOV (lowest cost) is used since the gas tube surge arrester handles the high-energy portion of the transient.

The example duplicates the circuit between Neutral and Ground in addition to the Hot-to-Neutral circuit. This provides protection against Common Mode (both lines surged relative to ground) as well as Normal Mode (Hot-to-Neutral) transients. This is important because both types of transients are frequent occurrences in the real world. The failure to provide Common Mode protection is one of the leading causes of failure in many otherwise solid designs.

The critical points in the selection of the gas tube surge arrester are the minimum DC breakdown voltage (which must be higher than the highest normal voltage expected on the protected line) and the follow-on current rating (which must be higher than the expected fault current of the incoming supply line). In this example, the minimum DC breakdown voltage is calculated by multiplying the normal line voltage (120VRMS) by 1.414 to obtain the peak voltage and then adding an appropriate guard band to allow for normal variations in the supply voltage.

$$120V_{RMS} \times 1.414 = 170V_{PEAK}$$

$$170V_{PEAK} \times (15\%\ \text{Guardband}) = 196V\ \text{Minimum}$$

The MOV should be selected using the same formula. When used in a properly designed hybrid circuit, a 7mm device is normally adequate to handle the small leading-edge currents until the gas tube surge arrester goes into conduction.

The inductor should have a value of at least 0.1mH. If the inductance is too low, the MOV may clamp the transient voltage at a level that does not allow the gas tube surge arrester to go into conduction. The result is usually the overloading and destruction of the MOV. Tests have been conducted using several common RFI filters having inductances or 1-2mH with excellent results.

Hybrid surge protection circuits incorporating HAC Series gas tube surge arresters can provide cost-effective protection against transients that exceed even the tough guidelines of IEEE C62.41-1991 for Location Categories A and B.

Notes

1. The exact value is a function of the Location Category and System Exposure level. See the IEEE spec for more detailed information.
2. The rise time for an open-circuit voltage waveform is defined as 1.67 x (t_{90} - t_{30}) where t_{30} and t_{90} are the 30% and 90% amplitude points on the leading edge of the waveform. The duration is defined as the time from the virtual origin, t_0 (where a line through t_{30} and t_{90} intersects the zero voltage axis), to the 50% amplitude point of the trailing edge of the waveform, t_{50}.
3. The rise time for an short-circuit current waveform is defined as 1.25 x (t_{90} - t_{10}) where t_{10} and t_{90} are the 10% and 90% amplitude points on the leading edge of the waveform. The duration is defined as the time from the virtual origin, t_0 (where a line through t_{10} and t_{90} intersects the zero current axis), to the 50% amplitude point of the trailing edge of the waveform, t_{50}.
4. If the current supplied by the AC power line exceeds the maximum follow-on current of the gas tube surge arrester (typically, ~20A), the device will continue to conduct, even at a zero crossing of the AC voltage signal, causing the gas tube surge arrester to overheat and fail.

IEC Electromagnetic Compatibility Standards for Industrial Process Measurement and Control Equipment

Introduction

The purpose of the International Electrotechnical Commission IEC 1000-4 (previously known as IEC-801) standard is to establish a common reference for evaluating the performance of industrial-process measurement and control instrumentation when exposed to electric or electromagnetic interference. The types of interference considered are those arising from sources external to the equipment.

The interference susceptibility tests are essentially designed to demonstrate the capability of equipment to function correctly when installed in its working environment. The type of test required should be determined on the basis of the interference to which the equipment may be exposed when installed while taking into consideration the electrical circuit (i.e., the way the circuit and shields are tied to earth ground), the quality of shielding applied, and the environment in which the system is required to work.

The IEC 1000-4 standard is divided into six sections:

IEC 1000-4-1. Introduction

IEC 1000-4-2. Electrostatic Discharge Requirements

IEC 1000-4-3. Radiated Electromagnetic Field Requirements

IEC 1000-4-4. Electrical Fast Transient (Burst) Requirements

IEC 1000-4-5. Surge Voltage Immunity Requirements

IEC 1000-4-6. Immunity to Conducted Disturbances Induced by Radio Frequency Fields Above 9kHz

Sections IEC 1000-4-2 through IEC 1000-4-5 will be discussed in this application note.

TEST SEVERITY LEVEL

LEVEL	TEST VOLTAGE: CONTACT DISCHARGE	TEST VOLTAGE: AIR DISCHARGE
1	2kV	2kV
2	4kV	4kV
3	6kV	8kV
4	8kV	15kV
X	Special	Special

NOTES:

1. "X" is an open level.
2. The test severity levels shall be selected in accordance with the most realistic installation and environmental conditions.

Electrostatic Discharge (ESD) Requirements

The purpose of this test is to find the reaction of the equipment when subjected to electrostatic discharges which may occur from personnel to objects near vital instrumentation.

In order to test the equipment's susceptibility to ESD, the test setup conditions must be established. Direct and indirect application of discharges to the Equipment Under Test (EUT) are possible, in the following manner:

a) Contact discharges to the conductive surfaces and to coupling planes.

b) Air discharge at insulating surfaces.

Two different types of tests can be conducted:

1. Type (conformance) tests performed in laboratories.
2. Post installation tests performed on equipment in its installed conditions.

CHARACTERISTICS OF THE ESD GENERATOR

LEVEL	INDICATED VOLTAGE	FIRST PEAK CURRENT OF DISCHARGE (±10%)	RISE TIME WITH DISCHARGE SWITCH	CURRENT AT 30ns (±30%)	CURRENT AT 60ns (±30%)
1	2kV	7.5A	0.7 to 1ns	4A	2A
2	4kV	15A	0.7 to 1ns	8A	4A
3	6kV	22.5A	0.7 to 1ns	12A	6A
4	8kV	30A	0.7 to 1ns	16A	8A

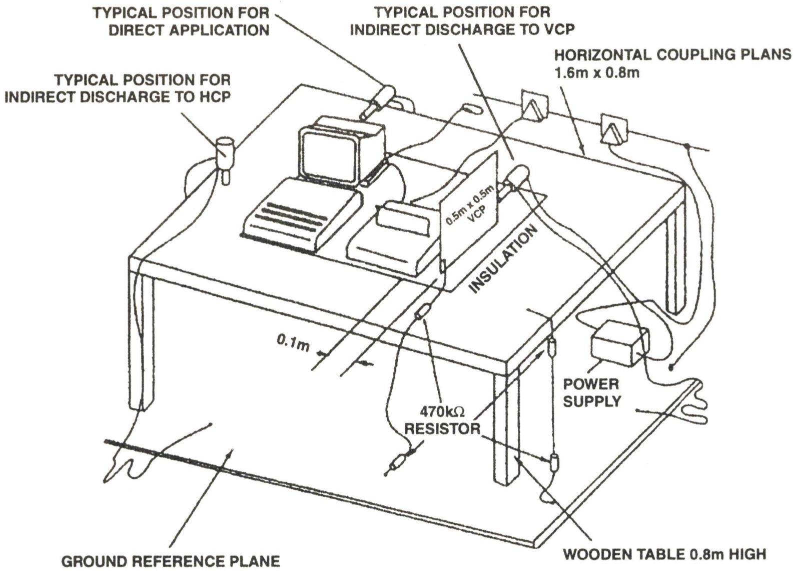


FIGURE 1. EXAMPLE OF TEST SETUP FOR TABLETOP EQUIPMENT, LABORATORY TESTS

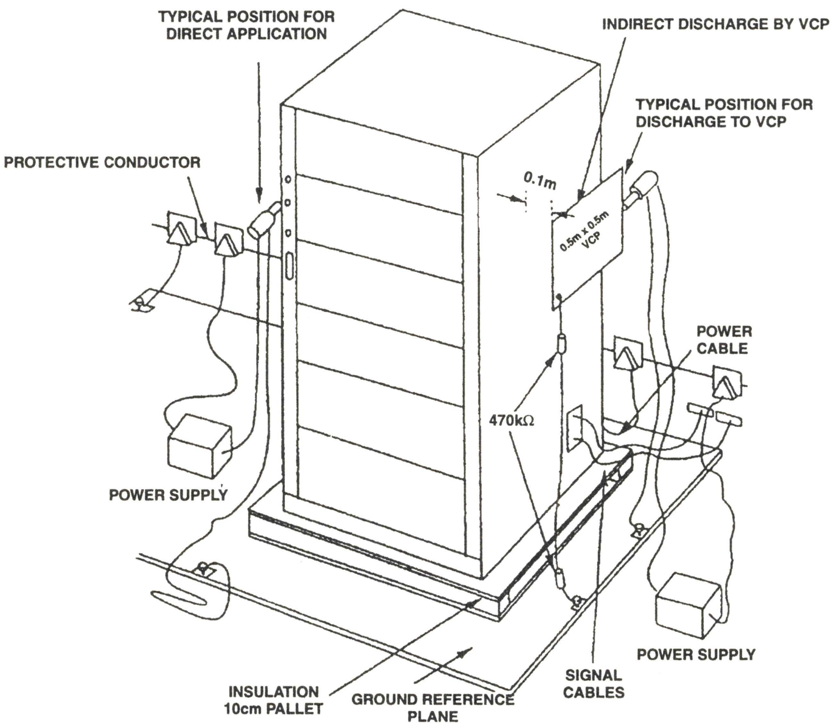


FIGURE 2. EXAMPLE OF TEST SETUP FOR FLOOR STANDING EQUIPMENT, LABORATORY TESTS

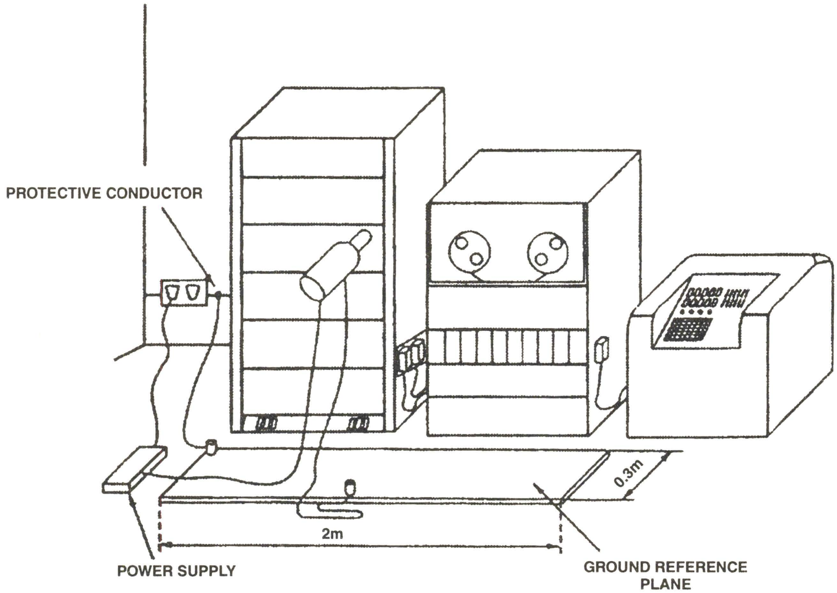


FIGURE 3. EXAMPLE OF TEST SETUP FOR EQUIPMENT, POST-INSTALLATION TESTS

The only accepted method of demonstrating conformance to the standard is the of type tests performed in laboratories. The EUT, however, shall be arranged as closely as possible to the actual installation conditions.

Examples of laboratory ESD test setups can be seen in Figure 1 for tabletop equipment and in Figure 2 for floor standing equipment.

Post installation tests are optional and not mandatory for certification. If a manufacturer and customer agree post installation tests are required, a typical test setup can be found in Figure 3.

Test Procedure

- For conformance testing, the EUT shall be continually operated in its most sensitive mode which shall be determined by preliminary testing.
- The test voltage shall be increased from the minimum to the selected test severity level.
- Number: at least 10 single discharges (in the most sensitive polarity).
- Time interval: initial value 1 second, longer intervals may be necessary.
- Direct application of discharge to the EUT: The static electricity discharges shall be applied only to those points and surfaces of the EUT which are accessible to the human operator during normal usage.
- Indirect application of the discharge: Discharges to objects placed or installed near the EUT shall be simulated by applying the discharges to a coupling plane (a horizontal coupling plane under the EUT or a vertical coupling plane).

Test Results

The results of the ESD tests are reported as follows:

1. Normal performance within the specification limits.
2. Temporary degradation or loss of function or performance which is self-recoverable.
3. Temporary degradation or loss of function or performance which requires operator intervention or system reset.
4. Degradation or loss of function which is not recoverable, due to damage of equipment (component) or software, or loss of date.

IEC 1000-4-3

Radiated Electromagnetic Field Requirements

This test shows the susceptibility of instrumentation when subjected to electromagnetic fields such as those generated by portable radio transceivers or any other device that will generate continuous wave (CW) radiated electromagnetic energy.

TEST SEVERITY LEVELS

Frequency band: 27MHz to 500MHz

LEVEL	TEST FIELD STRENGTH (V/M)
1	1
2	3
3	10
X	Special

NOTES:

3. "X" is an open class.
4. The test severity levels shall be selected in accordance with the electromagnetic radiation environment to which the EUT may be exposed when finally installed.

Test Setup

Examples of the test configuration for radiated electromagnetic fields can be found in Figure 4 and Figure 5.

- The procedure requires the generation of electromagnetic fields within which the test sample is placed and its operation observed. The tests shall be carried out in a shielded enclosure or anechoic chamber The test procedure assumes the use of biconical and log-spiral antennae or stripline.
- All testing of the equipment shall be performed in conditions as close as possible to the actual installation.

Small objects (25cm x 25cm x 25cm) can be tested using a stripline antennae. This is a parallel plate transmission line to generate an electromagnetic field as shown in Figure 6.

Test Procedure

- The test is performed with the EUT in the most sensitive physical orientation.
- The frequency range is swept from 27 MHz to 500 MHz. The sweep rate is in the order of 1.5 x 10-3 decades/sec.

Test Results

The results of the radiated electromagnetic field include:

- The effect of the electromagnetic field on the output of the EUT
  - As a consistent measurable effect.
  - As a random effect, not repeatable, and possibly further classified as a transient effect occurring during the application of the electromagnetic field and as a permanent or semipermanent field after the application of the electromagnetic field.
- Any damage to the EUT resulting from the application of the electromagnetic field.

The qualitative evaluation of the resultant data needs to be assessed in terms of the existing local ambient electromagnetic level and the specific operating frequencies.

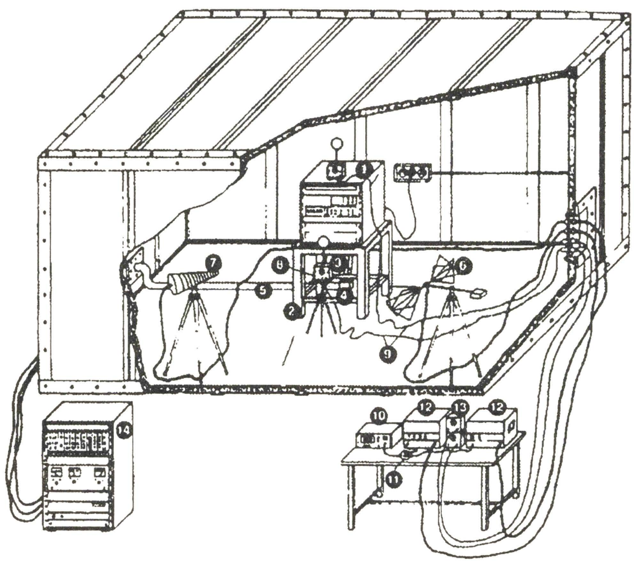


FIGURE 4. TEST SETUP FOR RADIATED ELECTROMAGNETIC FIELD TESTS IN A SHIELDED ROOM WHERE THE ANTENNAE, FIELD STRENGTH MONITORS AND EUT ARE INSIDE AND THE MEASURING INSTRUMENTS AND ASSOCIATED EQUIPMENT ARE OUTSIDE THE SHIELDED ROOM

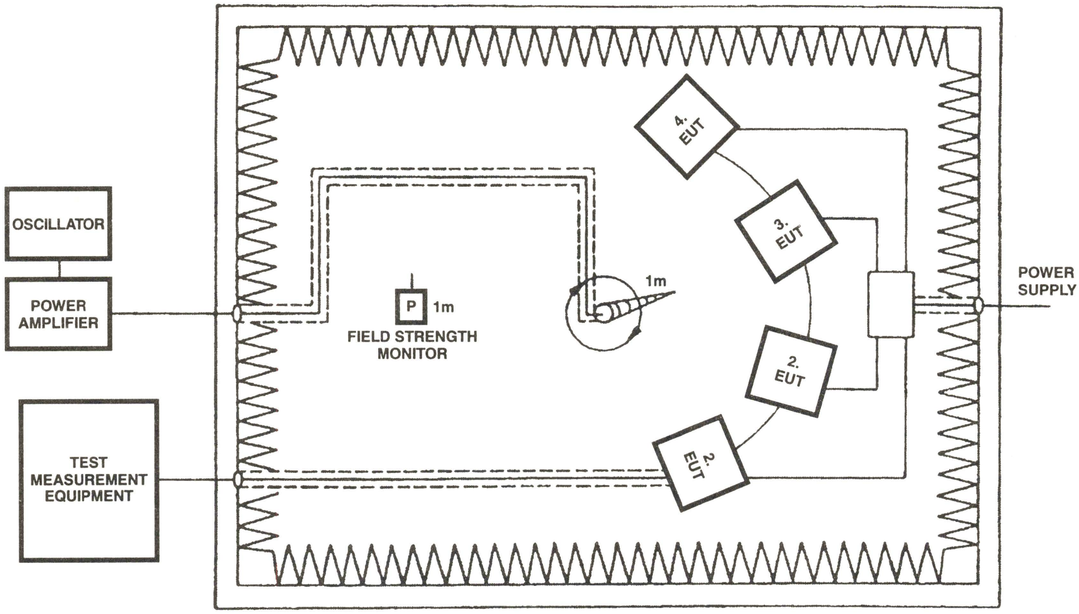
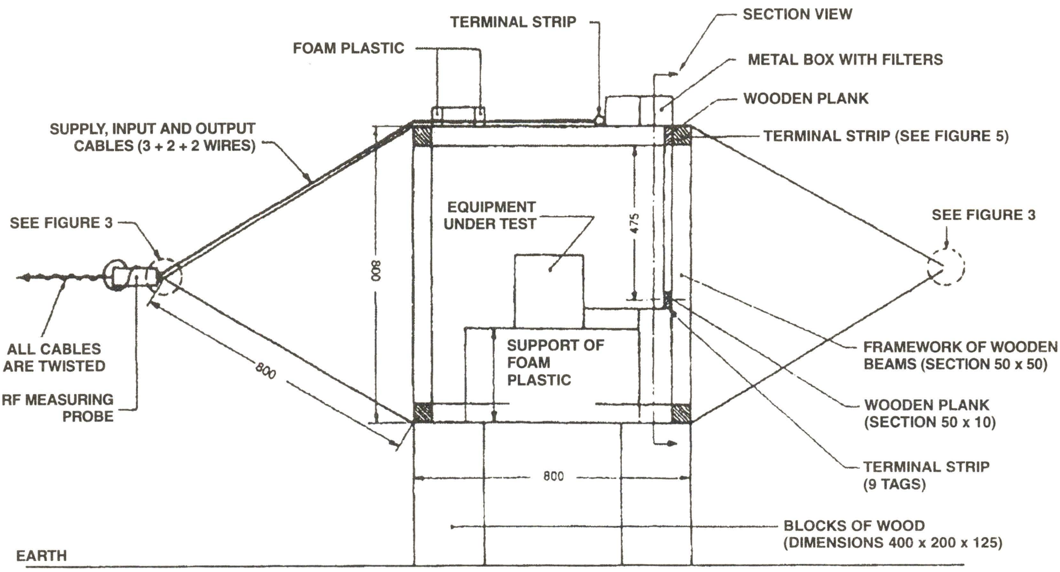


FIGURE 5. TEST SETUP FOR RADIATED ELECTROMAGNETIC FIELD TESTS IN AN ANECHOIC CHAMBER, GENERAL ARRANGEMENT OF THE EUT, FIELD STRENGTH MONITOR AND ANTENNAE



NOTE: Dimensions in millimeters.

FIGURE 6. TEST SETUP WITH STRIPLINE CIRCUIT

11 APPLICATION NOTES

IEC 1000-4-4

Electrical Fast Transient (Burst) Requirements

This test is intended to demonstrate the immunity of the equipment when subjected to interference originating from switching transients

TEST SEVERITY LEVELS

Open circuit output test voltage:

LEVEL	ON POWER SUPPLY	ON INPUT/OUTPUT SIGNAL DATA AND CONTROL LINES
1	0.5kV	0.25kV
2	1kV	0.5kV
3	2kV	1kV
4	4kV	2kV
X	Special	Special

NOTES:

5. "X" is an open level.
6. The test severity levels shall be selected in accordance with the most realistic installation and environmental conditions.

Characteristics of the Fast Transient/Burst Generator

- Rise time of one pulse: 5ns ±30%
- Impulse duration (50% value): 50ns ±30%
- Repetition rate of the impulses and peak values of the output voltage:
  5kHz ±20% at 0.125kV
  5kHz ±20% at 0.25kV
  5kHz ±20% at 0.5kV
  5kHz ±20% at 1.0kV
  5kHz ±20% at 2.0kV
- Burst duration: 15ms ±20%
- Burst period: 300ms ±20%

Test Setup

For laboratory testing, the test setup for type testing can be shown in Figure 7 and Figure 8.

- Power supply lines (See Figure 7): If the line current is higher than 100A, the "field test" shall be used.
- Earth connections of the cabinets: The test point on the cabinet shall be the terminal for the protective earth conductor (See Figure 7).
- Input/Output circuits and communication lines (See Figure 8).

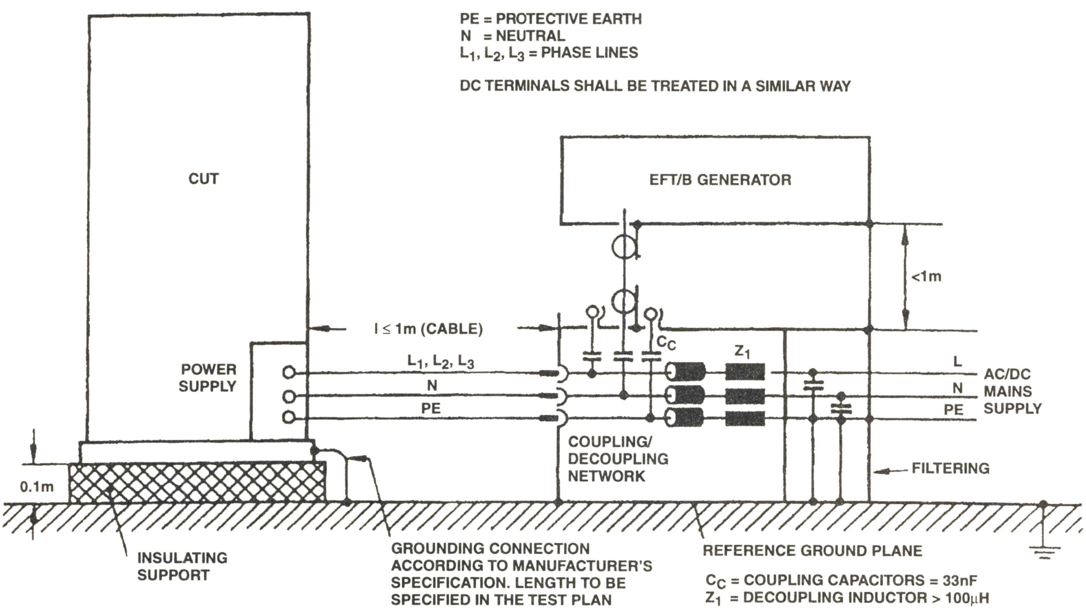


FIGURE 7. EXAMPLE OF TEST SETUP FOR DIRECT COUPLING OF THE TEST VOLTAGE TO AC/DC POWER SUPPLY LINES/TERMINALS FOR LABORATORY TEST PURPOSES

IEC 1000-4-4

Electrical Fast Transient (Burst) Requirements

For field testing, the equipment or system shall be tested in the final installed conditions without coupling/decoupling networks.

- Power supply lines and protective earth terminals
  - Stationary, floor-mounted EUT: The test voltage shall be applied between a reference ground plane and each of the power supply terminals, AC or DC, and on the terminals for the protective or function earth on the cabinet of the EUT. (See Figure 9).
  - Non-stationary mounted EUT, connected to the mains supply by flexible cord and plugs: The test voltage shall be applied between each of the power supply conductors and the protective earth at the power supply outlet to which the EUT is to be connected. (See Figure 10).

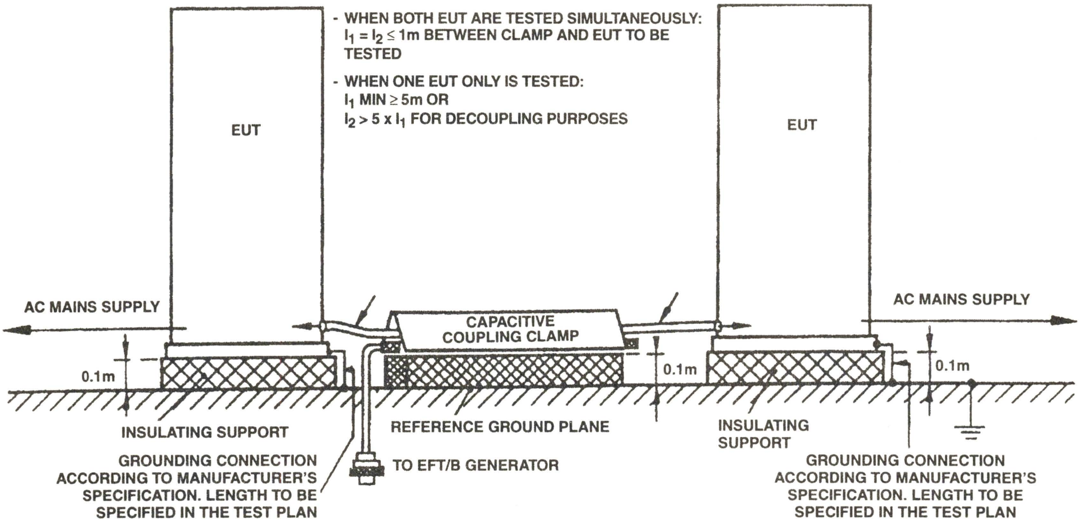
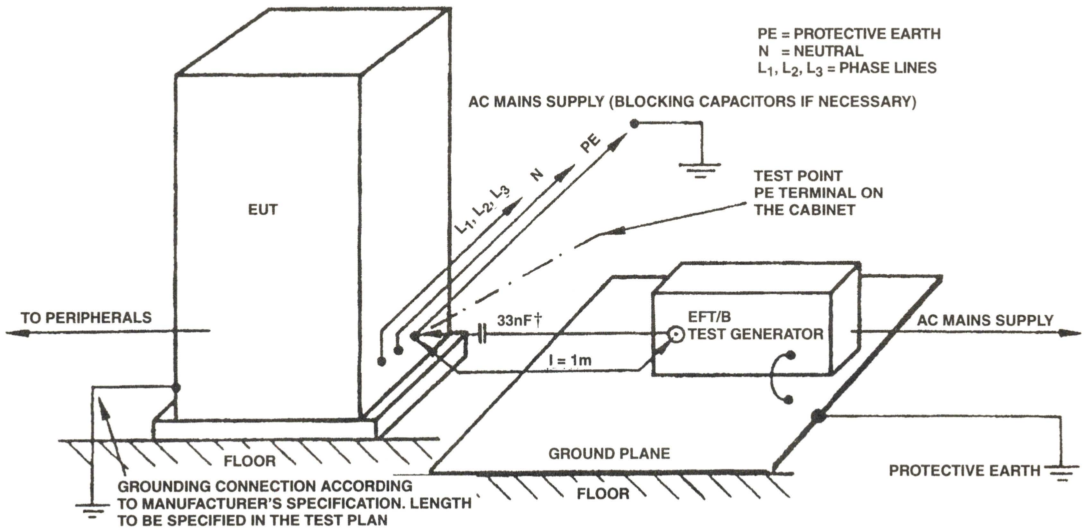


FIGURE 8. EXAMPLE OF TEST SETUP FOR APPLICATION OF THE TEST VOLTAGE BY THE CAPACITIVE COUPLING CLAMP FOR LABORATORY TEST PURPOSES



†DC terminals shall be treated in a similar way.

FIGURE 9. EXAMPLE OF FIELD TEST ON AC/DC POWER SUPPLY LINES AND PROTECTIVE EARTH TERMINALS FOR STATIONARY, FLOOR MOUNTED EUT

- Input/Output circuits and communication lines:
  - A capacitive clamp shall be used for coupling the test voltage into the lines. However, if the clamp cannot be used due to mechanical problems in the cabling, it may be replaced by a tape or a conductive foil enveloping the lines under test. (See Figure 11).

Test Procedure

- Polarity of the test voltage: both polarities are mandatory
- Duration of the test: at least 1 minute

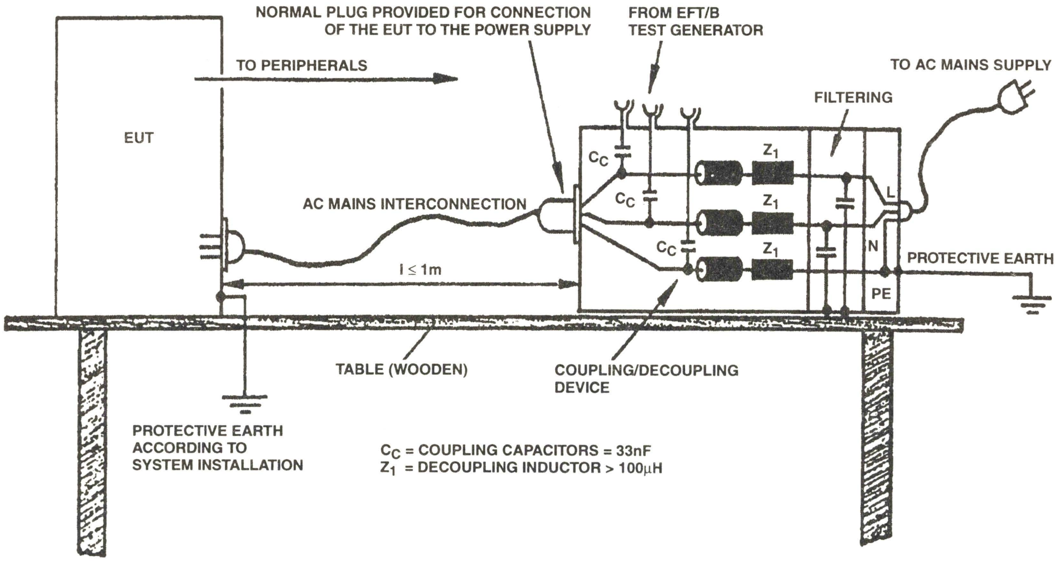


FIGURE 10. EXAMPLE OF FIELD TEST ON AC MAINS SUPPLY AND PROTECTIVE EARTH TERMINALS FOR NON-STATIONARY MOUNTED EUT

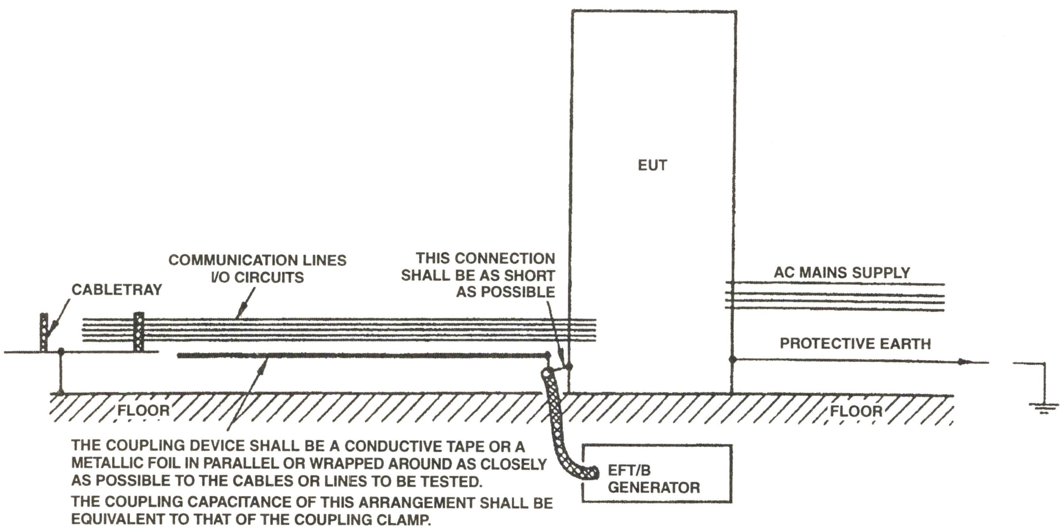


FIGURE 11. EXAMPLE OF FIELD TEST ON COMMUNICATIONS AND I/O CIRCUITS WITHOUT THE CAPACITIVE COUPLING CLAMP

Test Results

The results are reported as:

1. Normal performance within the specification limits.
2. Temporary degradation or loss of function or performance which is self-recoverable.
3. Temporary degradation or loss of function or performance which requires operator intervention or system reset.
4. Degradation or loss of function which is not recoverable, due to damage of equipment (component) or software, or loss of data.

IEC 1000-4-5

Surge Voltage Immunity Requirements

The goal of the laboratory test is to determine the equipment's susceptibility to damage caused by overvoltage surges caused by circuit switching and lightning strikes.

TEST SEVERITY LEVELS

CLASS	POWER SUPPLY		UNSYM LINES LONG DATA BUS		SYMMETRICAL LINES	DATA BUS SHORT (DIST)
	LINE TO LINE Z = 2	LINE TO GROUND Z = 12	LINE TO LINE Z = 42	LINE TO GROUND Z = 42	LINE TO GROUND Z = 42	LINE TO GROUND
0	No Test is Advised					
1	-	0.5kV	-	0.5kV	1.0kV	-
2	0.5kV	1.0kV	0.5kV	1.0kV	1.0kV	0.5kV
3	1.0kV	2.0kV	1.0kV	2.0kV	2.0kV	-
4	2.0kV	4.0kV	2.0kV	4.0kV	-	-
5	(Note 8)	(Note 8)	2.0kV	4.0kV	4.0kV	-
X	Special					

NOTES:

7. Z is the source impedance.
8. Depends on the class of the local power supply system. "X" is an open level that has to be specified in the product specification. The class depends on the installation conditions.

Characteristics of the Test Instrumentation

- Combination wave test generator
  - Open circuit output voltage . . . . 0.5kV to 4.0kV
  - Short circuit output current . . . . 0.25kA to 2.0kA

	IN ACCORDANCE WITH IEC60-2		IN ACCORDANCE WITH IEC469-1	
	FRONT TIME	TIME TO HALF VALUE	RISE TIME (10%-90%)	DURATION (50%-50%)
Open Circuit Voltage	1.2μs	50μs	1μs	50μs
Short Circuit Current	8μs	20μs	6.4μs	16μs

- Test generator 10/700 μs (according to CCITT):
  - Open circuit output voltage . . . . .0.5kV to 4.0kV
  - Short circuit output current . . . . 12.5A to 100A

	IN ACCORDANCE WITH IEC60-2		IN ACCORDANCE WITH IEC469-1	
	FRONT TIME	TIME TO HALF VALUE	RISE TIME (10%-90%)	DURATION (50%-50%)
Open Circuit Voltage	10μs	700μs	6.5μs	700μs
Short Circuit Current	-	-	4μs	300μs

NOTE: The surges (and test generators) related to the different classes are:
Class 1 to 4: 1.2/50μs (8/20μs)
Class 5: 1.2/50μs (8/20ms) and 10/700μs

Test Setup

A decoupling network is used to prevent surge energy from being propagated to the other equipment operating from the same source during testing of the EUT. The test setup for evaluating the EUT power supply is shown in Figures 12 - 15. A capacitive coupling network (preferred) or an inductive coupling network is used for this test.

The test setup for evaluating the unshielded interconnection lines of the EUT is illustrated in Figures 16-20. Usually, capacitive coupling is used, but inductive coupling or coupling via gas discharge tube (GDT) surge arrestors is also possible.

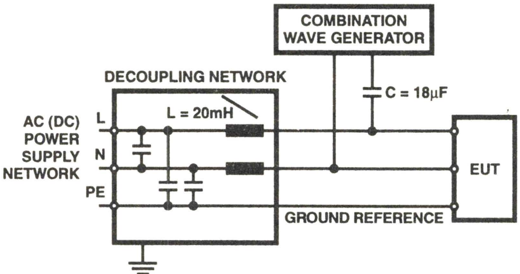


FIGURE 12. TEST SETUP FOR CAPACITIVE COUPLING ON AC/DC LINES; LINE TO LINE COUPLING ACCORDING TO 7.2

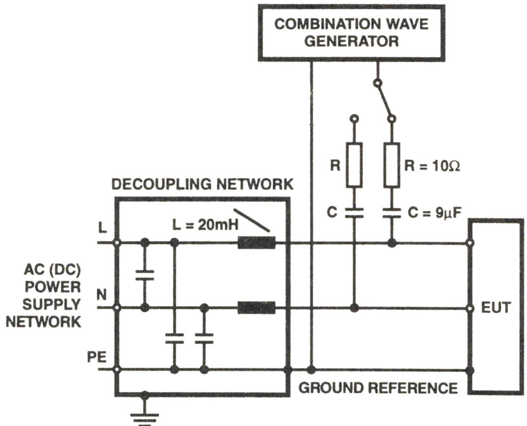


FIGURE 13. TEST SETUP FOR CAPACITIVE COUPLING ON AC/DC LINES; LINE TO GROUND COUPLING ACCORDING TO 7.2 (GENERATOR OUTPUT FLOATING OR EARTHED)

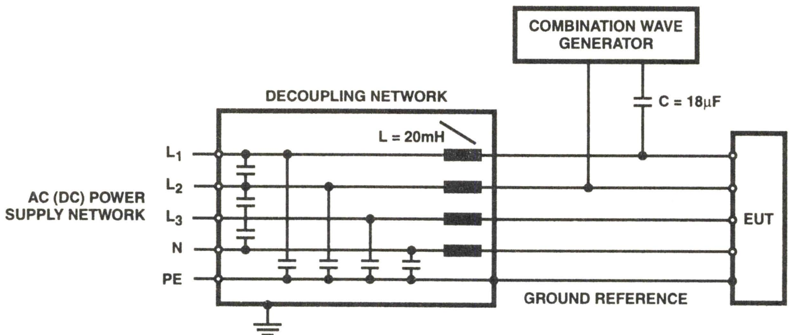


FIGURE 14. TEST SETUP FOR CAPACITIVE COUPLING ON AC LINES (3 PHASES); LINE TO LINE COUPLING ACCORDING TO 7.2

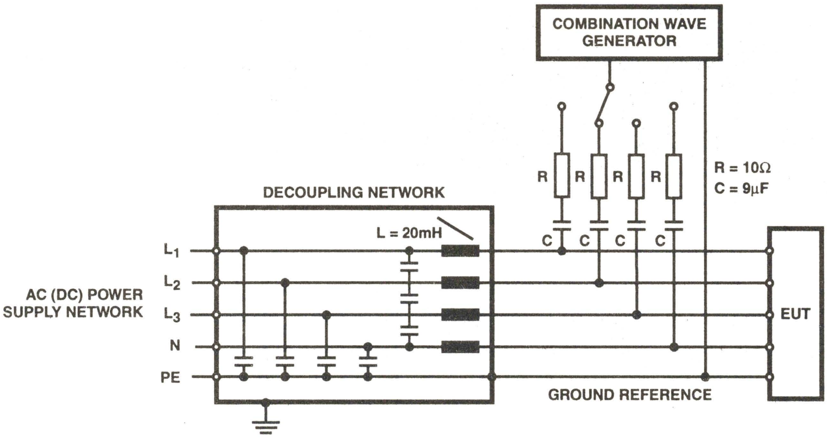


FIGURE 15. TEST SETUP FOR CAPACITIVE COUPLING ON AC LINES (3 PHASES); LINE TO GROUND COUPLING ACCORDING TO 7.2

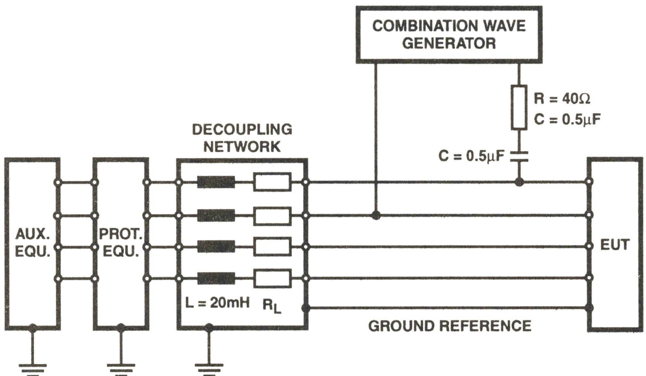


FIGURE 16. TEST SETUP FOR UNSHIELDED INTERCONNECTION LINES; LINE TO LINE COUPLING ACCORDING TO 7.3; COUPLING VIA CAPACITORS

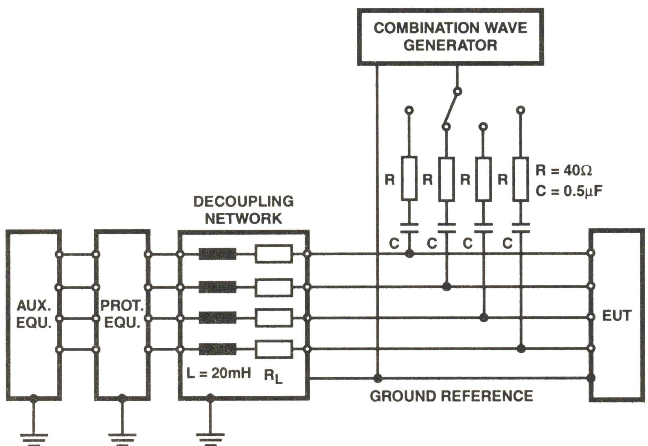


FIGURE 17. TEST SETUP FOR UNSHIELDED INTERCONNECTION LINES; LINE TO GROUND COUPLING TO 7.3; COUPLING VIA CAPACITORS

11

APPLICATION NOTES

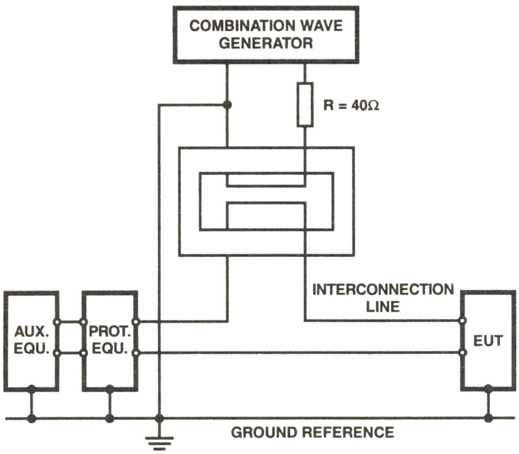


FIGURE 18. TEST SETUP FOR UNSHEILDED INTERCONNECTION LINES; LINE TO LINE COUPLING ACCORDING TO 7.3; INDUCTIVE COUPLING FOR HIGH IMPEDANCE CIRCUITS

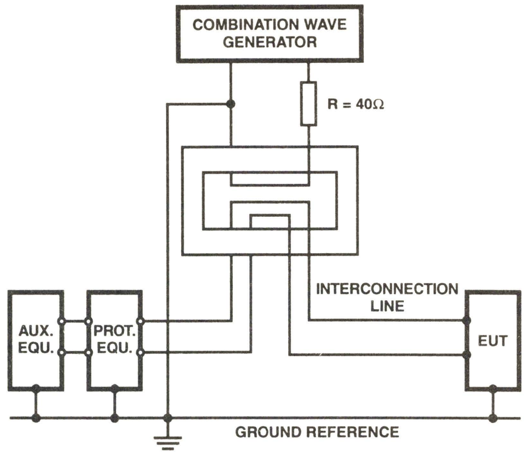


FIGURE 19. SIMPLIFIED TEST SETUP FOR UNSHIELDED INTERCONNECTION LINES; LINE TO GROUND COUPLING ACCORDING TO 7.3; INDUCTIVE COUPLING FOR LOW IMPEDANCE CIRCUITS

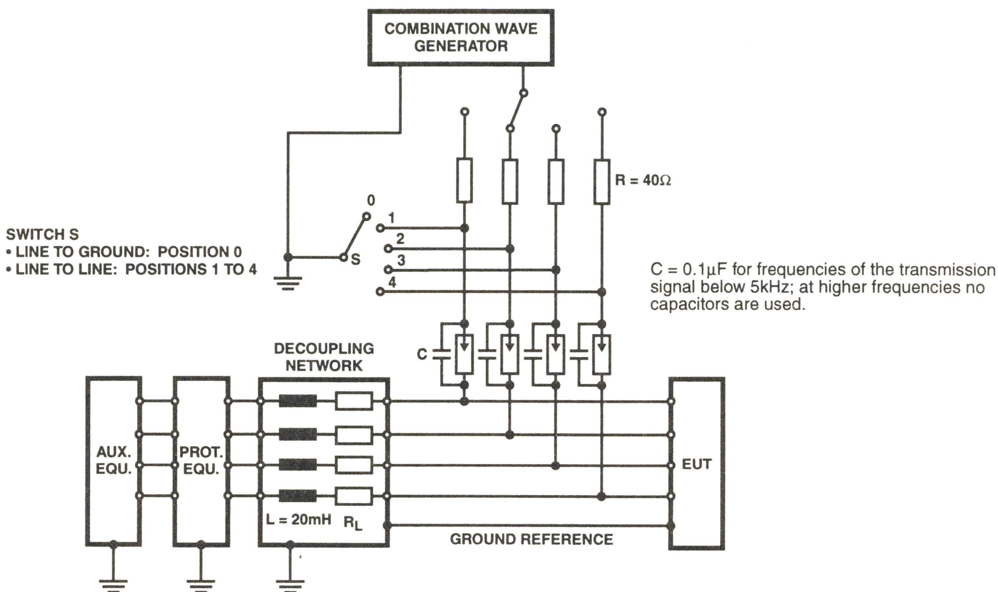


FIGURE 20. TEST SETUP FOR UNSHIELDED UNSYMMETRICALLY OPERATED LINES; LINE TO GROUND COUPLING ACCORDING TO 7.3; COUPLING VIA GAS ARRESTORS

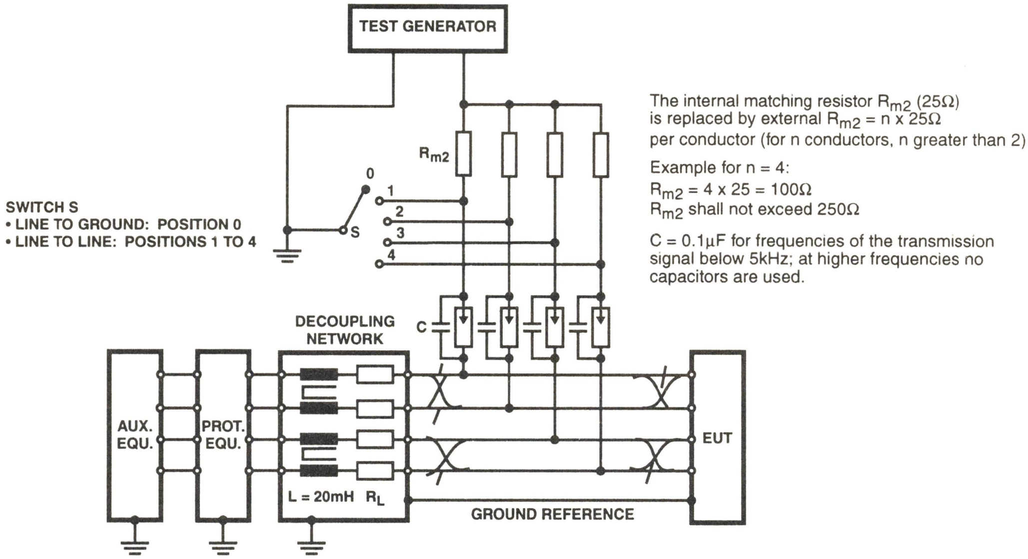


FIGURE 21. TEST SETUP FOR UNSHIELDED SYMMETRY OPERATED LINES (TELECOMMUNICATION LINES); LINE TO GROUND COUPLING ACCORDING TO 7.4; COUPLING VIA GAS ARRESTORS

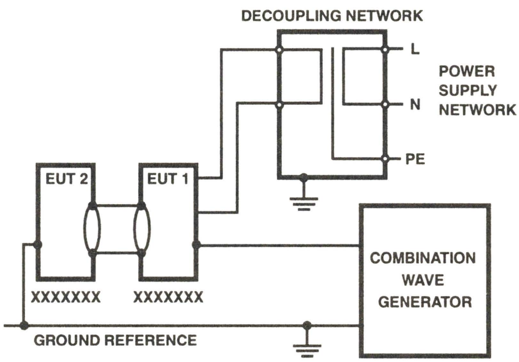


FIGURE 22. TEST SETUP FOR TESTS APPLIED TO SHIELDED LINES AND TO APPLY POTENTIAL DIFFERENCES ACCORDING TO 7.5 AND 7.6; GALVANIC COUPLING

Test Procedure

- Number of tests: at least 5 positive and 5 negative at the selected points.
- Pulse repetition: max. 1/min.
- The maximum repetition rate depends on the built-in protection devices of the EUT.
- The surge will be applied between lines and between lines and ground.
- All lower levels including the selected test level must be satisfied. For testing the secondary protection, the output voltage of the generator must be increased up to the worst case voltage break down of the primary protection.

Test Results

The results of the test are reported as follows:

1. Normal performance within the specification limits.
2. Temporary degradation or loss of function or performance which is self-recoverable.
3. Temporary degradation or loss of function or performance which requires operator intervention or system reset.
4. Degradation or loss of function which is not recoverable, due to damage of equipment (component) or software, or loss of data.

Harris Semiconductor

APPNOTE

No. AN9735 September 1997

Harris Suppression Products

How to Test Gas Discharge Tubes

This Application Note describes how to design and build instruments for performing several of the more common tests for Gas Discharge Tubes (GDT).

DC Breakdown Voltage

This is the voltage level at which the spark discharge occurs when the voltage across the gap is slowly increased. A linear ramp rate is usually specified and typically increases at a rate of 1000 volts per second or less. For most purposes, any adjustable voltage DC power supply (with adequate voltage output) can be used for DC breakdown voltage testing by slowly increasing the output voltage.

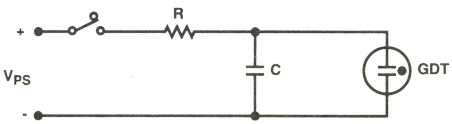


FIGURE 1. SIMPLE DC BREAKDOWN VOLTAGE TEST CIRCUIT USING AN R-C CIRCUIT TO SET THE RAMP RATE

For more repeatability of the ramp rate, consider adding an R-C circuit to the output of the power supply as depicted in Figure 1. If the output voltage of the power supply is quickly increased to V_{PS}, then the voltage across the capacitor, $V_C(t)$, is given by:

$$V_C(t) = V_{PS}\left(1 - e^{-\frac{t}{RC}}\right) \quad \text{(EQ. 1)}$$

The instantaneous ramp rate is given by:

$$\frac{dV_C}{dt} = \frac{V_{PS}}{RC}e^{-\frac{t}{RC}} \quad \text{(EQ. 2)}$$

If Equation 1 is solved for $e^{-\frac{t}{RC}}$ and substituted into Equation 2, then

$$\frac{dV_C}{dt} = \frac{V_{PS}}{RC}\left(1 - \frac{V_C(t)}{V_{PS}}\right) \quad \text{(EQ. 3)}$$

If the power supply voltage is set to 150% of the nominal breakdown voltage, then the quantity in parentheses in Equation 3 is equal to 1/3 at breakdown. Substituting this into Equation 3 yields

$$\left.\frac{dV_c}{dt}\right|_{\text{at BDV}} = \frac{V_{PS}}{RC} \times \frac{1}{3} = \frac{1.5V_{BDV}}{RC} \times \frac{1}{3} = \frac{V_{BDV}}{2RC} \quad \text{(EQ. 4)}$$

If the circuit uses a 0.01μF capacitor and a 25MΩ resistor (with the spark gap to be tested connected across the capacitor) and a 375V power supply to test a 250V spark gap, then the ramp rate will be 500V/s according to Equation 4. Equation 3 can be used to check the ramp rate for breakdowns different from the nominal value. For a 212.5V (0.85 x 250V) breakdown, the ramp rate using the values given above would be 650V/s. For a 287.5V (1.15 x 250V) breakdown, the ramp rate using the values given above would be 350V/s.

For a more linear ramp, we suggest using a power supply with remotely controlled output voltage (which can function essentially like an operational amplifier) controlled with a low voltage linear ramp generator.

Impulse Breakdown Voltage

Building test equipment for impulse breakdown voltage testing is not as straightforward as for DC testing. One common approach is to use a pulse transformer. In its simplest form, the tester consists of a 0V to 500V DC power supply which charges a capacitor that is discharged through the primary of the pulse transformer. The GDT under test is connected directly across the secondary of the pulse transformer. Coarse adjustment of the ramp rate can be accomplished by adding a capacitor (a few picofarad) across the GDT under test. Fine adjustment can be accomplished by adjusting the output of the DC power supply.

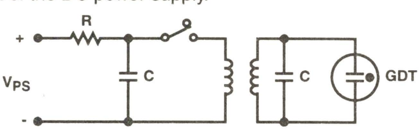


FIGURE 2. SIMPLE CIRCUIT FOR GENERATING IMPULSE BREAKDOWN VOLTAGE WAVEFORMS

Insulation Resistance

To make this measurement at the rated voltage (often 100V, but never exceeding the breakdown voltage of the gap) requires specialized equipment. A megohmmeter can be used to directly measure insulation resistance. A power supply and a sensitive ammeter can be used to measure the leakage current at the rated voltage. Dividing the leakage current into the voltage will yield the insulation resistance. For example, if a GDT with 100V across it yields a leakage current of 10nA, then its insulation resistance is 10GΩ (100V/10nA).

In situations where the insulation resistance limit is much lower (during life testing), insulation resistance measurements can often be reasonably made using a basic ohmmeter.

Harris Semiconductor

APPNOTE

No. AN9767 January 1998

Harris Suppression Products

Harris Varistors - Basic Properties, Terminology and Theory

What Is A Harris Varistor?

Varistors are voltage dependent, nonlinear devices which have an electrical behavior similar to back-to-back zener diodes. The symmetrical, sharp breakdown characteristics shown in Figure 1 enable the varistor to provide excellent transient suppression performance. When exposed to high voltage transients the varistor impedance changes many orders of magnitude from a near open circuit to a highly conductive level, thus clamping the transient voltage to a safe level. The potentially destructive energy of the incoming transient pulse is absorbed by the varistor, thereby protecting vulnerable circuit components.

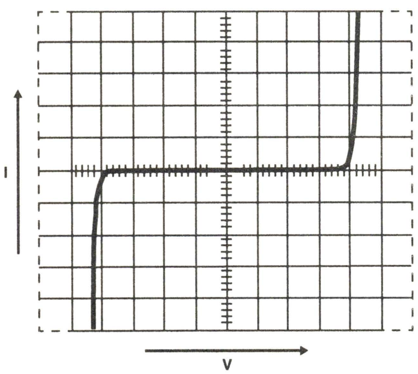


FIGURE 1. TYPICAL VARISTOR V-I CHARACTERISTIC

The varistor is composed primarily of zinc oxide with small additions of bismuth, cobalt, manganese and other metal oxides. The structure of the body consists of a matrix of conductive zinc oxide grains separated by grain boundaries providing P-N junction semiconductor characteristics. These boundaries are responsible for blocking conduction at low voltages and are the source of the nonlinear electrical conduction at higher voltages.

Since electrical conduction occurs, in effect, between zinc oxide grains distributed throughout the bulk of the device, the Harris Varistor is inherently more rugged than its single P-N junction counterparts, such as zener diodes. In the varistor, energy is absorbed uniformly throughout the body of the device with the resultant heating spread evenly through its volume. Electrical properties are controlled mainly by the physical dimensions of the varistor body which is sintered in various form factors such as discs, chips and tubes. The energy rating is determined by volume, voltage rating by thickness or current flow path length, and current capability by area measured normal to the direction of current flow.

Harris Varistors are available with AC operating voltages from 2.5V to 6000V. Higher voltages are limited only by packaging ability. Peak current handling exceeds 70,000A and energy capability extends beyond 10,000J for the larger units. Package styles include the tiny multilayer surface mount suppressors, tubular devices for use in connectors, and progress in size up to the rugged industrial device line.

Physical Properties

Introduction

An attractive property of the metal oxide varistor, fabricated from zinc oxide (ZnO), is that the electrical characteristics are related to the bulk of the device. Each ZnO grain of the ceramic acts as if it has a semiconductor junction at the grain boundary. A cross-section of the material is shown in Figure 2, which illustrates the ceramic microstructure. The ZnO grain boundaries can be clearly observed. Since the nonlinear electrical behavior occurs at the boundary of each semiconducting ZnO grain, the varistor can be considered a "multi-junction" device composed of many series and parallel connections of grain boundaries. Device behavior may be analyzed with respect to the details of the ceramic microstructure. Mean grain size and grain size distribution play a major role in electrical behavior.

11

APPLICATION NOTES

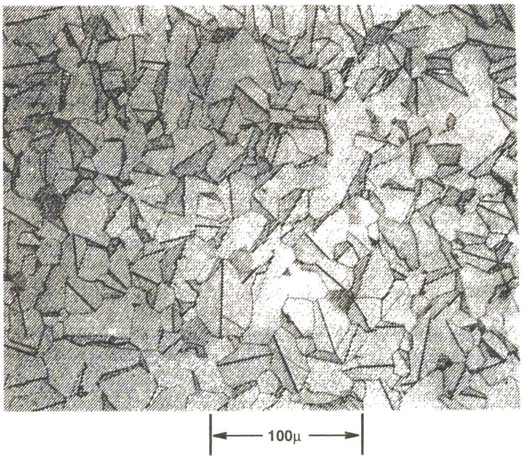


FIGURE 2. OPTICAL PHOTOMICROGRAPH OF A POLISHED AND ETCHED SECTION OF A VARISTOR

Varistor Microstructure

Varistors are fabricated by forming and sintering zinc oxide-based powders into ceramic parts. These parts are then electroded with either thick film silver or arc/flame sprayed metal. The bulk of the varistor between contacts is comprised of ZnO grains of an average size "d" as shown in the schematic model of Figure 3. Resistivity of the ZnO is <0.3Ω-cm.

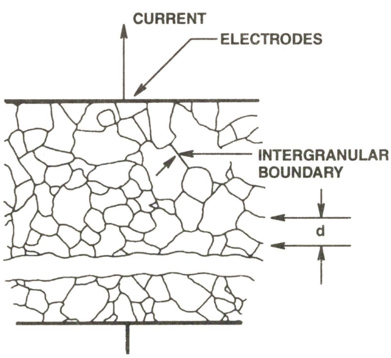


FIGURE 3. SCHEMATIC DEPICTION OF THE MICROSTRUCTURE OF A METAL-OXIDE VARISTOR. GRAINS OF CONDUCTING ZnO (AVERAGE SIZE d) ARE SEPARATED BY INTERGRANULAR BOUNDARIES

Designing a varistor for a given nominal varistor voltage, V_N, is basically a matter of selecting the device thickness such that the appropriate number of grains, n, are in series between electrodes. In practice, the varistor material is characterized by a voltage gradient measured across its thickness by a specific volts/mm value. By controlling composition and manufacturing conditions the gradient remains fixed. Because there are practical limits to the range of thicknesses achievable, more than one voltage gradient value is desired. By altering the composition of the metal oxide additives it is possible to change the grain size "d" and achieve the desired result.

A fundamental property of the ZnO varistor is that the voltage drop across a single interface "junction" between grains is nearly constant. Observations over a range of compositional variations and processing conditions show a fixed voltage drop of about 2V-3V per grain boundary junction. Also, the voltage drop does not vary for grains of different sizes.

It follows, then, that the varistor voltage will be determined by the thickness of the material and the size of the ZnO grains. The relationship can be stated very simply as follows:

Varistor Voltage, $V_N(DC) = (3V)n$

Where, n = average number of grain boundaries between electrodes

and, varistor thickness, $D = (n + 1)d \approx \dfrac{V_N \times d}{3}$

where, d = average grain size

The varistor voltage, V_N, is defined as the voltage across a varistor at the point on its V-I characteristic where the transition is complete from the low-level linear region to the highly nonlinear region. For standard measurement purposes, it is arbitrarily defined as the voltage at a current of 1mA.

Some typical values of dimensions for Harris varistors are given in Table 1.

TABLE 1.

VARISTOR VOLTAGE	AVERAGE GRAIN SIZE		GRADIENT	DEVICE THICKNESS
VOLTS	MICRONS	n	V/mm AT ImA	mm
$150V_{RMS}$	20	75	150	1.5
$25V_{RMS}$	80 (Note)	12	39	1.0

NOTE: Low voltage formulation.

Theory of Operation

Because of the polycrystalline nature of metal-oxide semiconductor varistors, the physical operation of the device is more complex than that of conventional semiconductors. Intensive measurement has determined many of the device's electrical characteristics, and much effort continues to better define the varistor's operation. In this application note we will discuss some theories of operation, but from the user's viewpoint this is not nearly as important as understanding the basic electrical properties as they relate to device construction.

The key to explaining metal-oxide varistor operation lies in understanding the electronic phenomena occurring near the grain boundaries, or junctions between the zinc oxide grains. While some of the early theory supposed that electronic tunneling occurred through an insulating second phase layer at

the grain boundaries, varistor operation is probably better described by a series-parallel arrangement of semiconducting diodes. In this model, the grain boundaries contain defect states which trap free electrons from the n-type semiconducting zinc oxide grains, thus forming a space charge depletion layer in the ZnO grains in the region adjacent to the grain boundaries.[6]

Evidence for depletion layers in the varistor is shown in Figure 4 where the inverse of the capacitance per boundary squared is plotted against the applied voltage per boundary.[7] This is the same type of behavior observed for semiconductor abrupt P-N junction diodes. The relationship is:

$$\frac{1}{C^2} = \frac{2(V_b + V)}{q\varepsilon sN}$$

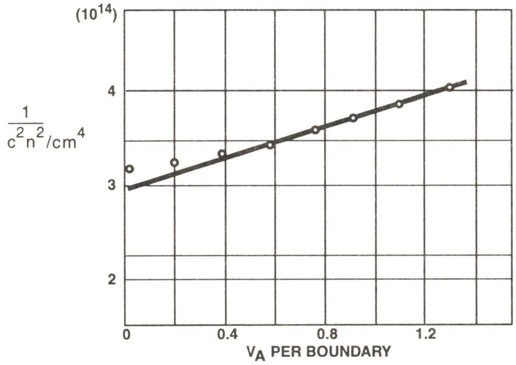


FIGURE 4. CAPACITANCE-VOLTAGE BEHAVIOR OF VARISTOR RESEMBLES A SEMICONDUCTOR ABRUPT-JUNCTION REVERSED BIASED DIODE Nd ~ 2 x 10^{17}/cm^3

Where V_b is the barrier voltage, V the applied voltage, q the electron charge, εs the semiconductor permittivity and N is the carrier concentration. From this relationship the ZnO carrier concentration, N, was determined to be about 2 x 10^{17} per cm^3.[7] In addition, the width of the depletion layer was calculated to be about 1000 Angstrom units. Single junction studies also support the diode model.[9]

It is these depletion layers that block the free flow of carriers and are responsible for the low voltage insulating behavior in the leakage region as depicted in Figure 5. The leakage current is due to the free flow of carriers across the field lowered barrier, and is thermally activated, at least above about 25°C.

Figure 5 shows an energy band diagram for a ZnO-grain boundary-ZnO junction.[10] The left-hand grain is forward biased, V_L, and the right side is reverse biased to V_R. The depletion layer widths are X_L and X_R, and the respective barrier heights are ϕ_L and ϕ_R. The zero biased barrier height is ϕ_O. As the voltage bias is increased, ϕ_L is decreased and ϕ_R is increased, leading to a lowering of the barrier and an increase in conduction.

The barrier height ϕ_L of a low voltage varistor was measured as a function of applied voltage[11], and is presented in Figure 6. The rapid decrease in the barrier at high voltage represents the onset of nonlinear conduction.[12]

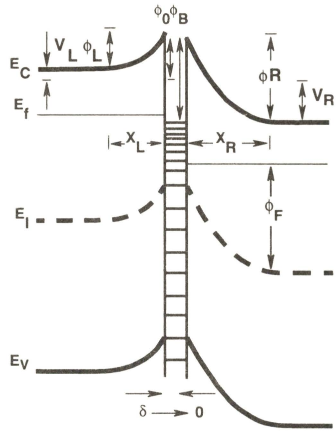


FIGURE 5. ENERGY BAND DIAGRAM OF A ZnO-GRAIN-BOUNDARY-ZnO JUNCTION

Transport mechanisms in the nonlinear region are very complicated and are still the subject of active research. Most theories draw their inspiration from semiconductor transport theory and the reader is referred to the literature for more information.[3, 5, 13, 14, 15]

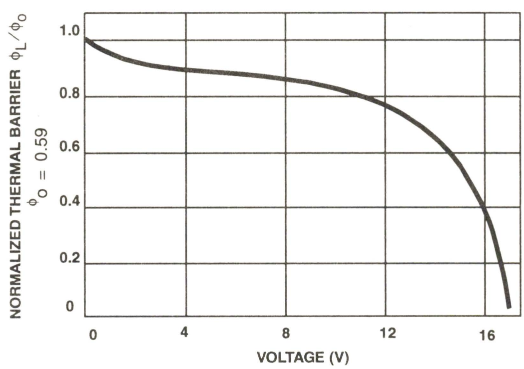


FIGURE 6. THERMAL BARRIER AS A FUNCTION OF APPLIED VOLTAGE

Turning now to the high current upturn region in Figure 10, we see that the V-I behavior approaches an ohmic characteristic. The limiting resistance value depends upon the electrical conductivity of the body of the semiconducting ZnO grains, which have carrier concentrations in the range of 10^{17} to 10^{18} per cm^3. This would put the ZnO resistivity below 0.3Ωcm.

Varistor Construction

The process of fabricating a Harris Varistor is illustrated in the flow chart of Figure 7. The starting material may differ in the composition of the additive oxides, in order to cover the voltage range of product.

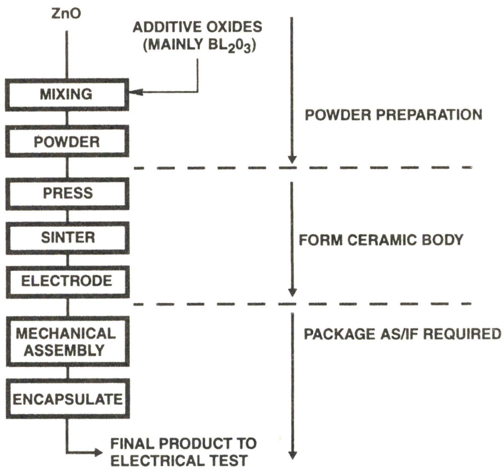


FIGURE 7. SCHEMATIC FLOW DIAGRAM OF HARRIS VARISTOR FABRICATION

Device characteristics are determined at the pressing operation. The powder is pressed into a form of predetermined thickness in order to obtain a desired value of nominal voltage. To obtain the desired ratings of peak current and energy capability, the electrode area and mass of the device are varied. The range of diameters obtainable in disc product offerings is listed here:

Nominal Disc Diameter - mm	3	5	7	10	14	20	32	40	62

Of course, other shapes, such as rectangles, are also possible by simply changing the press dies. Other ceramic fabrication techniques can be used to make different shapes. For example, rods or tubes are made by extruding and cutting to length. After forming, the green (i.e., unfired) parts are placed in a kiln and sintered at peak temperatures in excess of 1200°C. The bismuth oxide is molten above 825°C, assisting in the initial densification of the polycrystalline ceramic. At higher temperatures, grain growth occurs, forming a structure with controlled grain size.

Electroding is accomplished, for radial and chip devices, by means of thick film silver fired onto the ceramic surface. Wire leads or strap terminals are then soldered in place. A conductive epoxy is used for connecting leads to the axial 3mm discs. For the larger industrial devices (40mm and 60mm diameter discs) the contact material is arc sprayed aluminum, with an overspray of copper if necessary to give a solderable surface.

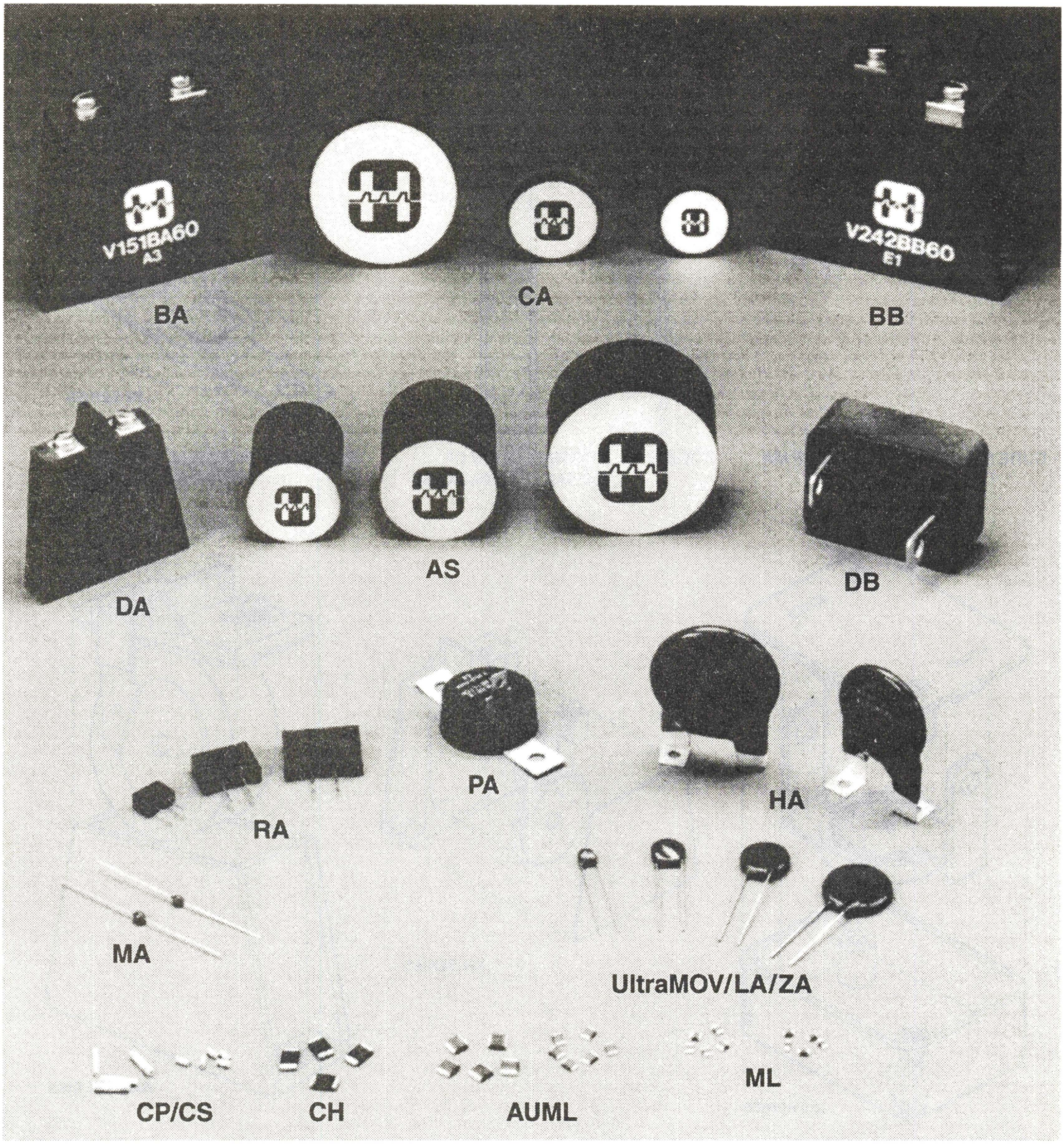
Many encapsulation techniques are used in the assembly of the various Harris Varistor packages. Most radials and some industrial devices (HA Series) are epoxy coated in a fluidised bed, whereas epoxy is "spun" onto the axial device. Radials are also available with phenolic coatings applied using a wet process. The PA series package consists of plastic molded around a 20mm disc subassembly. The RA, DA, and DB series devices are all similar in that they all are composed of discs or chips, with tabs or leads, encased in a molded plastic shell filled with epoxy. Different package styles allow variation in energy ratings, as well as in mechanical mounting. Figures 8 and 9 illustrate several package forms.

Figure 9 shows construction details of some packages. Dimensions of the ceramic, by package type, are given in Table 2.

TABLE 2. BY-TYPE CERAMIC DIMENSIONS

PACKAGE TYPE	SERIES	CERAMIC DIMENSIONS
Leadless Surface Mount	CH, AUML†, ML†, MLE† Series	5mm x 8mm Chip, 0603, 0805, 1206, 1210, 1812, 2220
Connector Pin	CP, CS Series	22, 20, 16 ID Gauge Tube
Axial Leaded	MA Series	3mm Diameter Disc
Radial Leaded	ZA, LA, "C" III, UltraMOV™ Series	5mm, 7mm, 10mm, 14mm, 20mm Diameter Discs
Boxed, Low Profile	RA Series	5mm x 8mm, 10mm x 16mm, 14 x 22 Chips
Industrial Packages	PA Series HA Series DA, DB Series BA, BB Series	20mm Diameter Disc 32mm, 40mm Diameter Disc 40mm Diameter Disc 60mm Diameter Disc
Industrial Discs	CA, NA Series	32mm, 40mm, 60mm Diameter Discs, 34mm Square
Arrester	AS Series	32mm, 42mm, 60mm Diameter Discs

†Harris multilayer suppressor technology devices.



HARRIS
SEMICONDUCTOR

FIGURE 8. PACKAGE FORMS

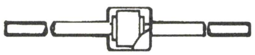


FIGURE 9A. CROSS-SECTION OF MA PACKAGE

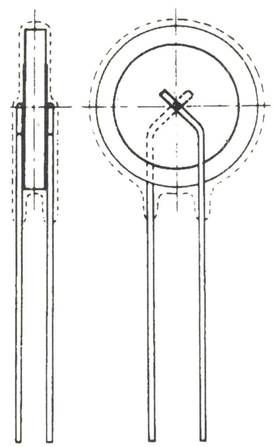


FIGURE 9B. CROSS-SECTION OF RADIAL LEAD PACKAGE

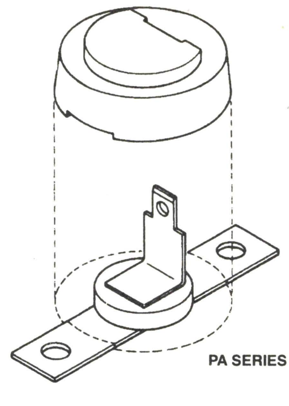


FIGURE 9C. PICTORIAL VIEW OF POWER MOV PACKAGE

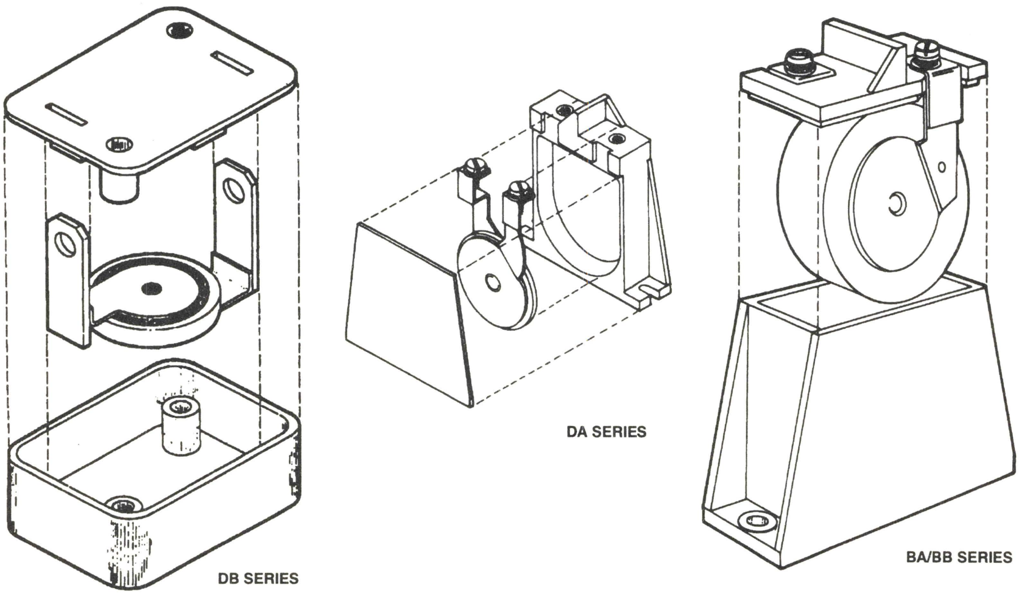


FIGURE 9D. PICTORIAL VIEW OF HIGH ENERGY PACKAGES, DA, DB, AND BA/BB SERIES

Electrical Characterization

Varistor VI Characteristics

Varistor electrical characteristics are conveniently displayed using log-log format in order to show the wide range of the V-I curve. The log format also is clearer than a linear representation which tends to exaggerate the nonlinearity in proportion to the current scale chosen. A typical V-I characteristic curve is shown in Figure 10. This plot shows a wider range of current than is normally provided on varistor data sheets in order to illustrate three distinct regions of electrical operation.

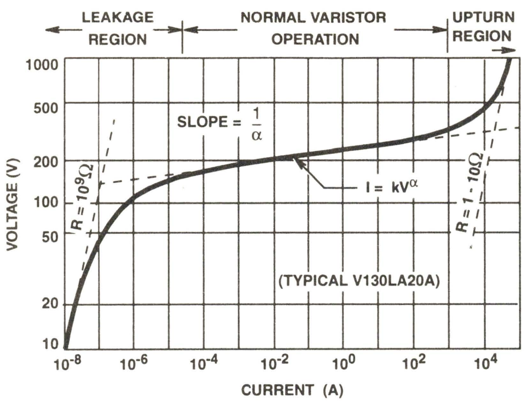


FIGURE 10. TYPICAL VARISTOR V-I CURVE PLOTTED ON LOG-LOG SCALE

Equivalent Circuit Model

An electrical model for the varistor can be represented by the simplified equivalent circuit of Figure 11.

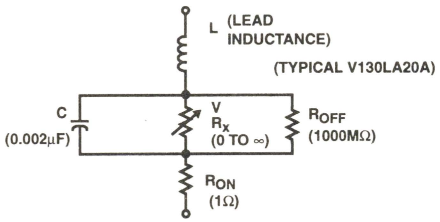


FIGURE 11. VARISTOR EQUIVALENT CIRCUIT MODEL

Leakage Region of Operation

At low current levels, the V-I Curve approaches a linear (ohmic) relationship and shows a significant temperature dependence. The varistor is in a high resistance mode (approaching $10^9\Omega$) and appears as an open circuit. The nonlinear resistance component, R_X, can be ignored because R_{OFF} in parallel will predominate. Also, R_{ON} will be insignificant compared to R_{OFF}.

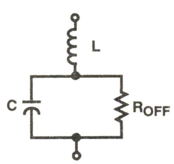


FIGURE 12. EQUIVALENT CIRCUIT AT LOW CURRENTS

For a given varistor device, capacitance remains approximately constant over a wide range of voltage and frequency in the leakage region. The value of capacitance drops only slightly as voltage is applied to the varistor. As the voltage approaches the nominal varistor voltage, the capacitance abruptly decreases. Capacitance remains nearly constant with frequency change up to 100kHz. Similarly, the change with temperature is small, the 25°C value of capacitance being well within ±10% from -40°C to 125°C.

The temperature effect of the V-I characteristic curve in the leakage region is shown in Figure 13. A distinct temperature dependence is noted.

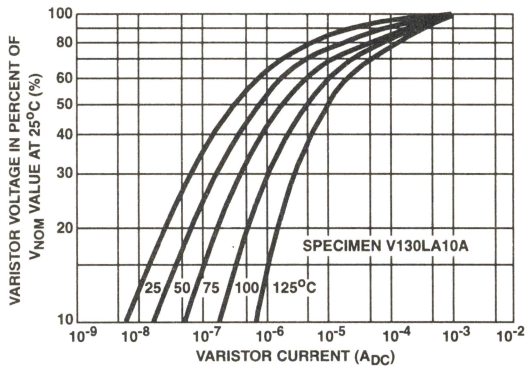


FIGURE 13. TEMPERATURE DEPENDENCE OF THE CHARACTERISTIC CURVE IN THE LEAKAGE REGION

The relation between the leakage current, I, and temperature, T, is:

$$I = I_O \varepsilon^{-V_B/kT}$$

where:
- I_O = constant
- k = Boltzmann's Constant
- V_B = 0.9eV

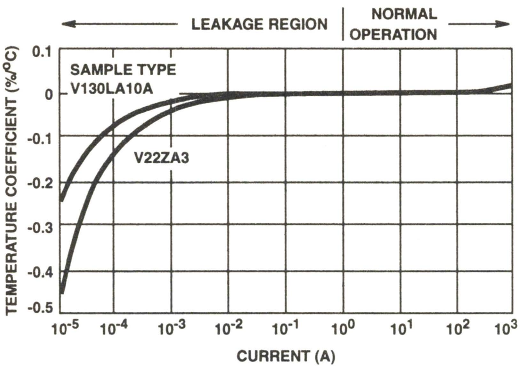
The temperature variation, in effect, corresponds to a change in R_{OFF}. However, R_{OFF} remains at a high resistance value even at elevated temperatures. For example, it is still in the range of 10MΩ to 100MΩ at 125°C.

Although R_{OFF} is a high resistance it varies with frequency. The relationship is approximately linear with inverse frequency.

$$R_{OFF} \sim \frac{1}{f}$$

However, the parallel combination of R_{OFF} and C is predominantly capacitive at any frequency of interest. This is because the capacitive reactance also varies approximately linearly with 1/f.

At higher currents, at and above the milliamp range, temperature variation becomes minimal. The plot of the temperature coefficient (DV/DT) is given in Figure 14. It should be noted that the temperature coefficient is negative and decreases as current rises. In the clamping voltage range of the varistor (I > 1A), the temperature dependency approaches zero.



NOTE: Typical Temperature Coefficient of Voltage vs Current, 14mm Size, 55°C to 125°C.

FIGURE 14. RELATION OF TEMPERATURE COEFFICIENT DV/DT TO VARISTOR CURRENT

Normal Varistor Region of Operation

The varistor characteristic follows the equation $I = kV^{\alpha}$, where k is a constant and the exponent α defines the degree of nonlinearity. Alpha is a figure of merit and can be determined from the slope of the V-I curve or calculated from the formula:

$$\alpha = \frac{\log(I_2/I_1)}{\log(V_2/V_1)}$$

$$= \frac{1}{\log(V_2/V_1)} \text{ for } I_2/I_1 = 1$$

In this region the varistor is conducting and R_X will predominate over C, R_{ON} and R_{OFF} . R_X becomes many orders of magnitude less than R_{OFF} but remains larger than R_{ON}.

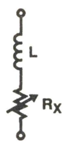


FIGURE 15. EQUIVALENT CIRCUIT AT VARISTOR CONDUCTION

During conduction the varistor voltage remains relatively constant for a change in current of several orders of magnitude. In effect, the device resistance, R_X, is changing in response to current. This can be observed by examining the static or dynamic resistance as a function of current. The static resistance is defined by:

$$R_X = \frac{V}{I}$$

and the dynamic resistance by:

$$Z_X = \frac{dv}{di} = V/\alpha I = R_X/\alpha$$

Plots of typical resistance values vs current, I, are given in Figure 16.

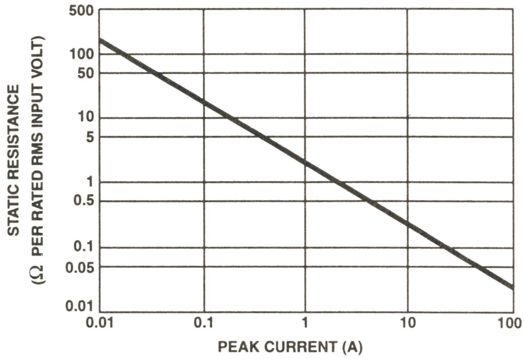


FIGURE 16A. R_X STATIC VARISTOR RESISTANCE FIGURE

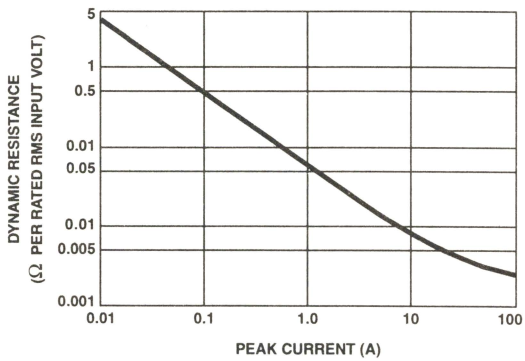


FIGURE 16B. Z_X DYNAMIC VARISTOR RESISTANCE

Upturn Region of Operation

At high currents, approaching the maximum rating, the varistor approximates a short-circuit. The curve departs from the nonlinear relation and approaches the value of the material bulk resistance, about 1Ω-10Ω. The upturn takes place as R_X approaches the value of R_{ON}. Resistor R_{ON} represents the bulk resistance of the zinc oxide grains. This resistance is linear (which appears as a steeper slope on the log plot) and occurs at currents 50A to 50,000A, depending on the varistor size.

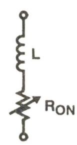


FIGURE 17. EQUIVALENT CIRCUIT AT VARISTOR UPTURN

Speed of Response and Rate Effects

The varistor action depends on a conduction mechanism similar to that of other semiconductor devices. For this reason, conduction occurs very rapidly, with no apparent time lag - even into the nanosecond range. Figure 18 shows a composite photograph of two voltage traces with and without a varistor inserted in a very low inductance inpulse generator. The second trace (which is not synchronized with the first, but merely superimposed on the oscilloscope screen) shows that the voltage clamping effect of the varistor occurs in less than one nanosecond.

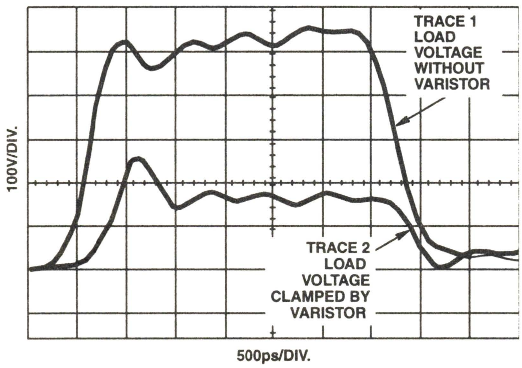


FIGURE 18. RESPONSE OF A ZnO VARISTOR TO A FAST RISE TIME (500ps) PULSE

In the conventional lead-mounted devices, the inductance of the leads would completely mask the fast action of the varistor; therefore, the test circuit for Figure 18 required insertion of a small piece of varistor material in a coaxial line to demonstrate the intrinsic varistor response.

Tests made on lead mounted devices, even with careful attention to minimizing lead length, show that the voltages induced in the loop formed by the leads contribute a substantial part of the voltage appearing across the terminals of a varistor at high current and fast current rise. Fortunately, the currents which can be delivered by a transient source are invariably slower in rise time than the observed voltage transients. The applications most frequently encountered for varistors involve current rise times longer than 0.5µs.

Voltage rate-of-rise is not the best term to use when discussing the response of a varistor to a fast impulse (unlike spark gaps where a finite time is involved in switching from non-conducting to conducting state). The response time of the varistor to the transient current that a circuit can deliver is the appropriate characteristic to consider.

The V-I characteristic of Figure 19A shows how the response of the varistor is affected by the current waveform. From such data, an "overshoot" effect can be defined as being the relative increase in the maximum voltage appearing across the varistor during a fast current rise, using the conventional 8/20µs current wave as the reference. Figure 19B shows typical clamping voltage variation with rise time for various current levels.

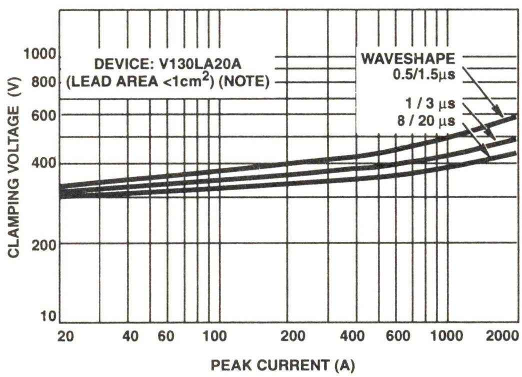


FIGURE 19A. V-I CHARACTERISTICS FOR VARIOUS CURRENT RISE TIMES

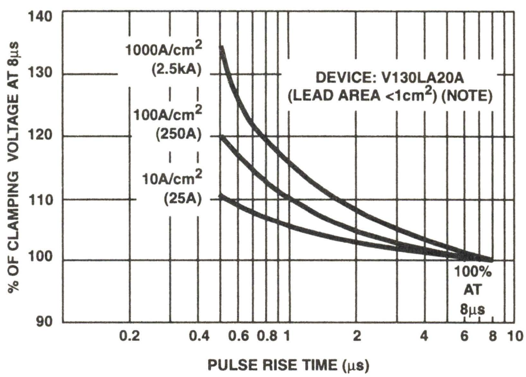


FIGURE 19B. OVERSHOOT DEFINED WITH REFERENCE TO THE BASIC 8/20µs CURRENT PULSE

NOTE: Refer to the Maximum Clamping Voltage section of DB450, Transient Voltage Suppression Devices.

FIGURE 19. RESPONSE OF LEAD-MOUNTED VARISTORS TO CURRENT WAVEFORM

Varistor Terminology

The following tabulation defines the terminology used in varistor specifications. Existing standards have been followed wherever possible.

Definitions (IEEE Standard C62.33, 1982)

A characteristic is an inherent and measurable property of a device. Such a property may be electrical, mechanical, or thermal, and can be expressed as a value for stated conditions.

A rating is a value which establishes either a limiting capability or a limiting condition (either maximum or minimum) for operation of a device. It is determined for specified values of environment and operation. The ratings indicate a level of stress which may be applied to the device without causing degradation or failure. Varistor symbols are defined on the linear V-I graph illustrated in Figure 20.

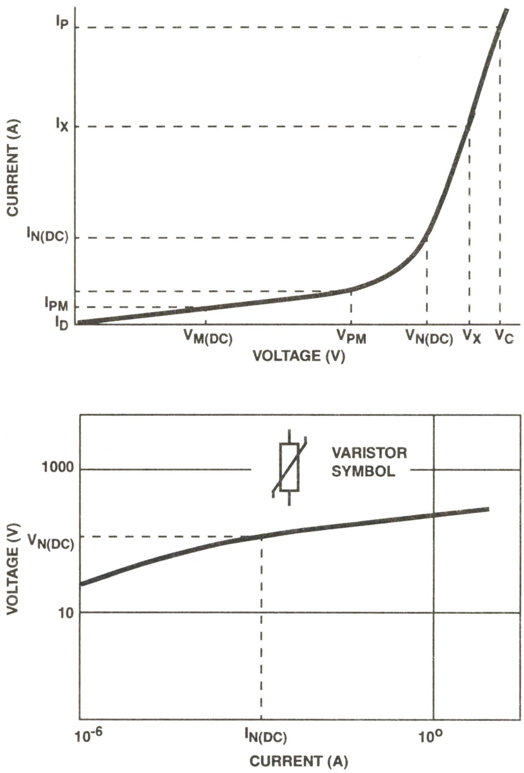


FIGURE 20. I-V GRAPH ILLUSTRATING SYMBOLS AND DEFINITIONS

Test Waveform

At high current and energy levels, varistor characteristics are measured, of necessity, with an impulse waveform. Shown in Figure 21 is the ANSI Standard C62.1 waveshape, an exponentially decaying waveform representative of lightning surges and the discharge of stored energy in reactive circuits.

The 8/20μs current wave (8μs rise and 20μs to 50% decay of peak value) is used as a standard, based on industry practices, for the characteristics and ratings described. One exception is the energy rating (W_{TM}), where a longer waveform of 10/1000μs is used. This condition is more representative of the high energy surges usually experienced from inductive discharge of motors and transformers. Varistors are rated for a maximum pulse energy surge that results in a varistor voltage (V_N) shift of less than ±10% from initial value.

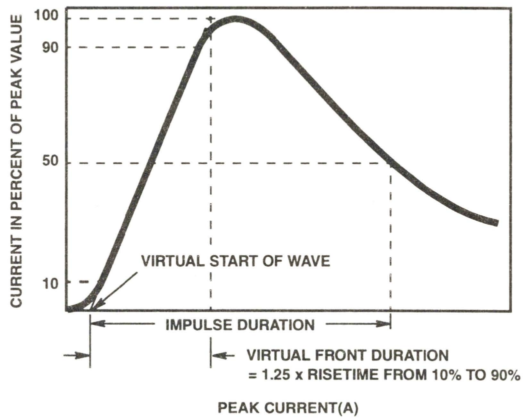


FIGURE 21. DEFINITION OF PULSE CURRENT WAVEFORM

TABLE 3. VARISTOR CHARACTERISTICS (IEEE STANDARD C62.33-1982 SUBSECTION 2.3 AND 2.4)

TERMS AND DESCRIPTIONS	SYMBOL
Clamping Voltage. Peak voltage across the varistor measured under conditions of a specified peak V_C pulse current and specified waveform. NOTE: Peak voltage and peak currents are not necessarily coincidental in time.	V_C
Rated Peak Single Pulse Transient Currents (Varistor). Maximum peak current which may be applied for a single 8/20μs impulse, with rated line voltage also applied, without causing device failure.	I_{TM}
Lifetime Rated Pulse Currents (Varistor). Derated values of I_{TM} for impulse durations exceeding that of an 8/20μs waveshape, and for multiple pulses which may be applied over device rated lifetime.	-
Rated RMS Voltage (Varistor). Maximum continuous sinusoidal RMS voltage which may be applied.	$V_{M(AC)}$
Rated DC Voltage (Varistor). Maximum continuous DC voltage which may be applied.	$V_{M(DC)}$
DC Standby Current (Varistor). Varistor current measured at rated voltage, $V_{M(DC)}$.	I_D
For certain applications, some of the following terms may be useful.	
Nominal Varistor Voltage. Voltage across the varistor measured at a specified pulsed DC current, $I_{N(DC)}$, of specific duration. $I_{N(DC)}$ of specific duration. $I_{N(DC)}$ is specified by the varistor manufacturer.	$V_{N(DC)}$
Peak Nominal Varistor Voltage. Voltage across the varistor measured at a specified peak AC current, $I_{N(AC)}$, of specific duration. $I_{N(AC)}$ is specified by the varistor manufacturer.	$V_{N(AC)}$
Rated Recurrent Peak Voltage (Varistor). Maximum recurrent peak voltage which may be applied for a specified duty cycle and waveform.	V_{PM}
Rated Single Pulse Transient Energy (Varistor). Energy which may be dissipated for a single impulse of maximum rated current at a specified waveshape, with rated RMS voltage or rated DC voltage also applied, without causing device failure.	W_{TM}
Rated Transient Average Power Dissipation (Varistor). Maximum average power which may be dissipated due to a group of pulses occurring within a specified isolated time period, without causing device failure.	$P_{T(AV)M}$
Varistor Voltage. Voltage across the varistor measured at a given current, I_X.	V_X
Voltage Clamping Ratio (Varistor). A figure of merit measure of the varistor clamping effectiveness as defined by the symbols $V_C/V_{M(AC)}$, $V_C/V_{M(DC)}$.	$\frac{V_C}{V_{PM}}$
Nonlinear Exponent. A measure of varistor nonlinearity between two given operating currents, I_1 and I_2, as described by $I = kV^{\alpha}$ where k is a device constant, $I_1 \le I \le I_2$, and $\alpha_{12} = \frac{\log I_2/I_1}{\log V_2/V_1}$	α
Dynamic Impedance (Varistor). A measure of small signal impedance at a given operating point as defined by: $Z_X = \frac{dV_X}{dI_X}$	Z_X
Resistance (Varistor). Static resistance of the varistor at a given operating point as defined by: $R_X = \frac{V_X}{I_X}$	R_X
Capacitance (Varistor). Capacitance between the two terminals of the varistor measured at C specified frequency and bias.	C
AC Standby Power (Varistor). Varistor AC power dissipation measured at rated rms voltage $V_{M(AC)}$.	P_D
Voltage Overshoot (Varistor). The excess voltage above the clamping voltage of the device for a given current that occurs when current waves of less than 8μs virtual front duration are applied. This value may be expressed as a % of the clamping voltage (V_C) for an 8/20 current wave.	V_{OS}
Response Time (Varistor). The time between the point at which the wave exceeds the clamping voltage level (V_C) and the peak of the voltage overshoot. For the purpose of this definition, clamping voltage as defined with an 8/20μs current waveform of the same peak current amplitude as the waveform used for this response time.	-
Overshoot Duration (Varistor). The time between the point voltage level (V_C) and the point at which the voltage overshoot has decayed to 50% of its peak. For the purpose of this definition, clamping voltage is defined with an 8/20μs current waveform of the same peak current amplitude as the waveform used for this overshoot duration.	-

How to Connect a Harris Varistor

Transient suppressors can be exposed to high currents for short durations in the nanoseconds to millisecond time frame.

Harris Varistors are connected in parallel to the load, and any voltage drop in the leads to the varistor will reduce its effectiveness. Best results are obtained by using short leads that are close together to reduce induced voltages and a low ohmic resistance to reduce I • R drops.

Electrical Connections

Single Phase

This is the most complete protection one can select, but in many cases only Varistor 1 or Varistor 1 and 2 are selected.

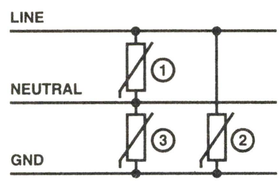


FIGURE 22.

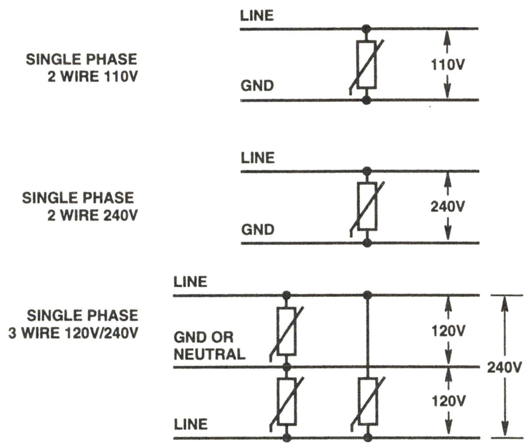


FIGURE 23.

3 Phase

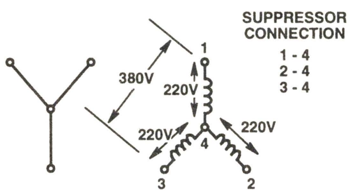


FIGURE 24A. 3 PHASE 220V/380V, UNGROUNDED

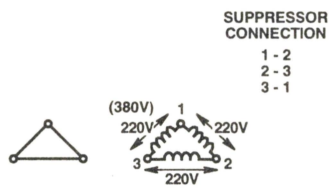


FIGURE 24B. 3 PHASE 220V OR 380V, UNGROUNDED

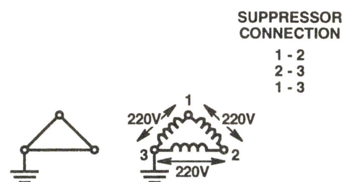


FIGURE 24C. 3 PHASE 220V, ONE PHASE GND

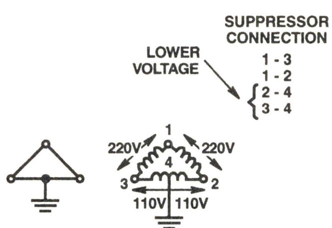
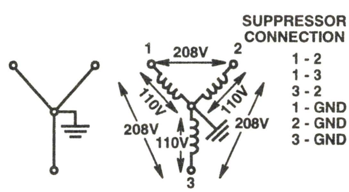
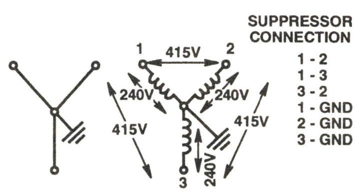


FIGURE 24D. 3 PHASE 220V



If only 3 suppressor use 1-GND, 2-GND, 3-GND

FIGURE 24E. 3 PHASE 120V/208V, 4 WIRE



If only 3 suppressor use 1-GND, 2-GND, 3-GND

FIGURE 24F. 3 PHASE 240V/415V

For higher voltages use same connections, but select varistors for the appropriate voltage rating.

DC Applications

DC applications require connection between plus and minus or plus and ground and minus and ground.

For example, if a transient towards ground exists on all 3 phases (common mode transients) only transient suppressors connected phase to ground would absorb energy. Transient suppressors connected phase to phase would not be effective.

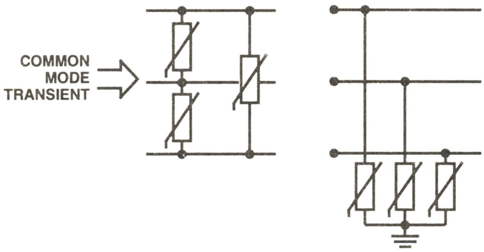


FIGURE 25A. INCORRECT FIGURE 25B. CORRECT

FIGURE 25. COMMON MODE TRANSIENT AND CORRECT SOLUTION

On the other hand if a differential mode of transient (phase to phase) exists then transient suppressors connected phase to phase would be the correct solution.

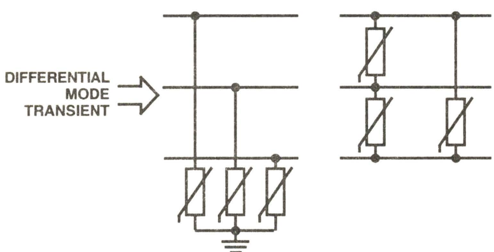


FIGURE 26A. INCORRECT FIGURE 26B. CORRECT

FIGURE 26. DIFFERENTIAL MODE TRANSIENT AND CORRECT SOLUTION

This is just a selection of some of the more important variations in connecting transient suppressors.

The logical approach is to connect the transient suppressor between the points of the potential difference created by the transient. The suppressor will then equalize or reduce these potentials to lower and harmless levels.

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For Harris documents available on the web, see http://www.semi.harris.com/
Harris AnswerFAX (407) 724-7800.

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No. AN9768 January 1998 **Harris Suppression Products**

Transient Suppression Devices and Principles

Transient Suppression Devices

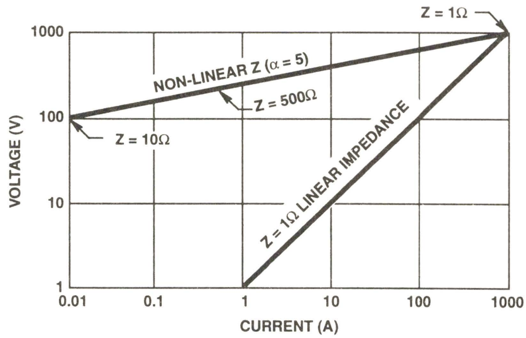
There are two major categories of transient suppressors: a) those that attenuate transients, thus preventing their propagation into the sensitive circuit; and b) those that divert transients away from sensitive loads and so limit the residual voltages.

Attenuating a transient, that is, keeping it from propagating away from its source or keeping it from impinging on a sensitive load is accomplished with filters inserted in series within a circuit. The filter, generally of the low-pass type, attenuates the transient (high frequency) and allows the signal or power flow (low-frequency) to continue undisturbed.

Diverting a transient can be accomplished with a voltage-clamping type device or with a “crowbar” type device. The designs of these two types, as well as their operation and application, are different enough to warrant a brief discussion of each in general terms. A more detailed description will follow later in this section.

A voltage-clamping device is a component having a variable impedance depending on the current flowing through the device or on the voltage across its terminal. These devices exhibit a nonlinear impedance characteristic that is, ohm's law is applicable but the equation has a variable R. The variation of the impedance is monotonic; in other words, it does not contain discontinuities in contrast to the crowbar device, which exhibits a turn-on action. The volt-ampere characteristic of these clamping devices is somewhat time-dependent, but they do not involve a time delay as do the sparkover of a gap or the triggering of a thyristor.

With a voltage-clamping device, the circuit is essentially unaffected by the presence of the device before and after the transient for any steady-state voltage below the clamping level. The voltage clamping action results from the increased current drawn through the device as the voltage tends to rise. If this current increase is greater than the voltage rise, the impedance of the device is nonlinear (Figure 1). The apparent “clamping” of the voltage results from the increased voltage drop (IR) in the source impedance due to the increased current. It should be clearly understood that the device depends on the source impedance to produce the clamping. One is seeing a voltage divider action at work, where the ratio of the divider is not constant but changes. However, if the source impedance is very low, then the ratio is low. The suppressor cannot be effective with zero source impedance (Figure 2) and works best when the voltage divider action can be implemented.



LINEAR IMPEDANCE: $I = \frac{V}{R}$

NON-LINEAR IMPEDANCE (POWER LAW): $I = KV^{\alpha}$

FIGURE 1. VOLTAGE/CURRENT CHARACTERISTIC FOR A LINEAR 1Ω RESISTOR AND NONLINEAR VARISTOR

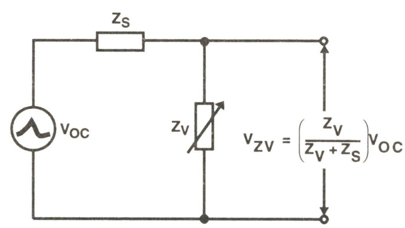


FIGURE 2A. VOLTAGE CLAMPING DEVICE

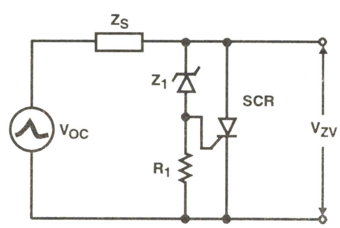


FIGURE 2B. CROWBAR DEVICE

FIGURE 2. DIVISION OF VOLTAGE WITH VARIABLE IMPEDANCE SUPPRESSOR

Crowbar-type devices involve a switching action, either the breakdown of a gas between electrodes or the turn-on of a thyristor, for example. After switching on, they offer a very low impedance path which diverts the transient away from the parallel-connected load.

These types of crowbar devices can have two limitations. One is delay time, which could leave the load unprotected during the initial transient rise. The second is that a power current from the voltage source will follow the surge discharge (called "follow-current" or "power-follow"). In AC circuits, this power-follow current may not be cleared at a natural current zero unless the device is designed to do so; in DC circuits the clearing is even more uncertain. In some cases, additional means must be provided to "open" the crowbar.

Filters

The frequency components of a transient are several orders of magnitude above the power frequency of an AC circuit and, of course, a DC circuit. Therefore, an obvious solution is to install a low-pass filter between the source of transients and the sensitive load.

The simplest form of filter is a capacitor placed across the line. The impedance of the capacitor forms a voltage divider with the source impedance, resulting in attenuation of the transient at high frequencies. This simple approach may have undesirable side effects, such as a) unwanted resonances with inductive components located elsewhere in the circuit leading to high peak voltages; b) high inrush currents during switching, or, c) excessive reactive load on the power system voltage. These undesirable effects can be reduced by adding a series resistor hence, the very popular use of RC snubbers and suppression networks. However, the price of the added resistance is less effective clamping.

Beyond the simple RC network, conventional filters comprising inductances and capacitors are widely used for interference protection. As a bonus, they also offer an effective transient protection, provided that the filter's front-end components can withstand the high voltage associated with the transient.

There is a fundamental limitation in the use of capacitors and filters for transient protection when the source of transients in unknown. The capacitor response is indeed nonlinear with frequency, but it is still a linear function of current.

To design a protection scheme against random transients, it is often necessary to make an assumption about the characteristics of the impinging transient. If an error in the source impedance or in the open-circuit voltage is made in that assumption, the consequences for a linear suppressor and a nonlinear suppressor are dramatically different as demonstrated by the following comparison.

A Simplified Comparison Between Protection with Linear and Nonlinear Suppressor Devices

Assume an open-circuit voltage of 3000V (see Figure 2):

1. If the source impedance is $Z_S = 50\Omega$
   With a suppressor impedance of $Z_V = 8\Omega$
   The expected current is:

$$1 = \frac{3000}{50+8} = 51.7\text{A and } V_R = 8 \times 51.7 = 414\text{V}$$

The maximum voltage appearing across the terminals of a typical nonlinear V130LA20A varistor at 51.7A is 330V.

Note that:

$$\begin{aligned} Z_S \times I &= 50 \times 51.7 = 2586\text{V} \\ Z_V \times I &= 8 \times 51.7 = \underline{414\text{V}} \\ &= 3000\text{V} \end{aligned}$$

2. If the source impedance is only 5Ω (a 10:1 error in the assumption), the voltage across the same linear 8Ω suppressor is:

$$V_R = 3000\ \frac{8}{5+8} = 1850\text{V}$$

However, the nonlinear varistor has a much lower impedance; again, by iteration from the characteristic curve, try 400V at 500A, which is correct for the V130LA20A; to prove the correctness of our "educated guess" we calculate I,

$$I = \frac{3000\text{-}400\text{V}}{5} = 520\text{A} \qquad \begin{aligned} Z_S \times I &= 5 \times 520 = 2600\text{V} \\ V_C &= \underline{400\text{V}} \\ &= 3000\text{V} \end{aligned}$$

which justifies the "educated guess" of 500A in the circuit.

Summary

TABLE 1. 3000V "OPEN-CIRCUIT" TRANSIENT VOLTAGE

	ASSUMED SOURCE IMPEDANCE	
	50Ω	5Ω
PROTECTIVE DEVICE	PROTECTIVE LEVEL ACHIEVED	
Linear 8Ω	414V	1850V
Nonlinear Varistor	330V	400V

Similar calculations can be made, with similar conclusions, for an assumed error in open-circuit voltage at a fixed source impedance. In that case, the linear device is even more sensitive to an error in the assumption. The calculations are left for the interested reader to work out.

The example calculated in the simplified comparison between protection with linear and nonlinear suppression devices shows that a source impedance change from an assumed 50Ω to 5Ω can produce a change of about 414V to 1850V for the protective voltage of a typical linear suppressor. With a typical nonlinear suppressor, the corresponding change is only 330V to 400V. In other words, a variation of only 21% in the protective level achieved with a nonlinear suppressor occurs for a 10 to 1 error in the assumption made on the transient parameters, in contrast to a 447% variation in the protective level with a linear suppressor for the same error in assumption. Nonlinear voltage-clamping devices give the lowest clamping voltage, resulting in the best protection against transients.

Crowbar Devices

This category of suppressors, primarily gas tubes or carbon-block protectors, is widely used in the communication field where power-follow current is less of a problem than in power circuits. Another form of these suppressors is the hybrid circuit which uses solid-state or MOV devices.

In effect, a crowbar device short-circuits a high voltage to ground. This short will continue until the current is brought to a low level. Because the voltage (arc or forward-drop) during the discharge is held very low, substantial currents can be carried by the suppressor without dissipating a considerable amount of energy within it. This capability is a major advantage.

Volt-Time Response - When the voltage rises across a spark gap, no significant conduction can take place until transition to the arc mode has occurred by avalanche breakdown of the gas between the electrodes.

Power-Follow - The second characteristic is that a power current from the steady-state voltage source will follow the surge discharge (called "follow-current" or "power-follow").

Voltage-Clamping Devices

To perform the voltage limiting function, voltage-clamping devices at the beginning of the section depend on their non-linear impedance in conjunction with the transient source impedance. Three types of devices have been used: reverse selenium rectifiers, avalanche (zener) diodes and varistors made of different materials, i.e., silicon carbide, zinc oxide, etc. [1]

Selenium Cells - Selenium transient suppressors apply the technology of selenium rectifiers in conjunction with a special process allowing reverse breakdown current at high-energy levels without damage to the polycrystalline structure. These cells are built by developing the rectifier elements on the surface of a metal plate substrate which gives them good thermal mass and energy dissipation performance. Some of these have self-healing characteristics which allows the device to survive energy discharges in excess of the rated values for a limited number of operations characteristics that are useful, if not "legal" in the unsure world of voltage transients.

The selenium cells, however, do not have the clamping ability of the more modern metal-oxide varistors or avalanche diodes. Consequently, their field of application has been considerably diminished.

Zener Diodes - Silicon rectifier technology, designed for transient suppression, has improved the performance of regulator-type zener diodes. The major advantage of these diodes is their very effective clamping, which comes closest to an ideal constant voltage clamp.

Since the diode maintains the avalanche voltage across a thin junction area during surge discharge, substantial heat is generated in a small volume. The major limitation of this type of device is its energy dissipation capability.

Silicon Carbide Varistors - Until the introduction of metal-oxide varistors, the most common type of "varistor" was made from specially processed silicon carbide. This material was very successfully applied in high-power, high-voltage surge arresters. However, the relatively low a values of this material produce one of two results. Either the protective level is too high for a device capable of withstanding line voltage or, for a device producing an acceptable protective level, excessive standby current would be drawn at normal voltage if directly connected across the line. Therefore, a series gap is required to block the normal voltage.

In lower voltage electronic circuits, silicon carbide varistors have not been widely used because of the need for using a series gap, which increases the total cost and reproduces some of the characteristics of gaps described earlier. However, this varistor has been used as a current-limiting resistor to assist some gaps in clearing power-follow current.

Metal-Oxide Varistors - A varistor functions as a nonlinear variable impedance. The relationship between the current in the device, I, and the voltage across the terminals, V is typically described by a power law: $I = kV^{\alpha}$. While more accurate and more complete equations can be derived to reflect the physics of the device, [2, 3] this definition will suffice here. A more detailed discussion will be found in Application Note AN9767, "Harris Varistors - Basic Properties, Terminology and Theory".

The term α (alpha) in the equation represents the degree of nonlinearity of the conduction. A linear resistance has an $\alpha = 1$. The higher the value of a, the better the clamp, which explains why α is sometimes used as a figure of merit. Quite naturally, varistor manufacturers are constantly striving for higher alphas.

This family of transient voltage suppressors are made of sintered metal oxides, primarily zinc oxide with suitable additives. These varistors have α values considerably greater than those of silicon carbide varistors, typically in the range of an effective value of 15 to 30 measured over several decades of surge current.

The high exponent values (α) of the metal-oxide varistors have opened completely new fields of applications by providing a sufficiently low protective level and a low standby current. The opportunities for applications extend from low-power electronics to the largest utility-type surge arresters.

Transient Suppressors Compared

Because of diversity of characteristics and nonstandardized manufacturer specifications, transient suppressors are not easy to compare. A graph (Figure 3) shows the relative volt-ampere characteristics of the four common devices that are used in 120V AC circuits. A curve for a simple ohmic resistor is included for comparison. It can be seen that as the alpha factor increases, the curve's voltage-current slope becomes less steep and approaches an almost constant voltage. High alphas are desirable for clamping applications that require operation over a wide range of currents.

It also is necessary to know the device energy-absorption and peak-current capabilities when comparisons are made. Table 2 includes other important parameters of commonly used suppressors.

Standby Power - The power consumed by the suppressor unit at normal line voltage is an important selection criterion. Peak standby current is one factor that determines the standby power of a suppressor. The standby power dissipation depends also on the alpha characteristic of the device.

As an example, a selenium suppressor in Table 2 can have a 12mA peak standby current and an alpha of 8 (Figure 3). Therefore, it has a standby power dissipation of about 0.5W on a $120V_{RMS}$ line (170V peak). A zener-diode suppressor has standby power dissipation of less than a milliwatt. And a silicon-carbide varistor, in a 0.75" diameter disc, has standby power in the 200mW range. High standby power in the lower alpha devices is necessary to achieve a reasonable clamping voltage at higher currents.

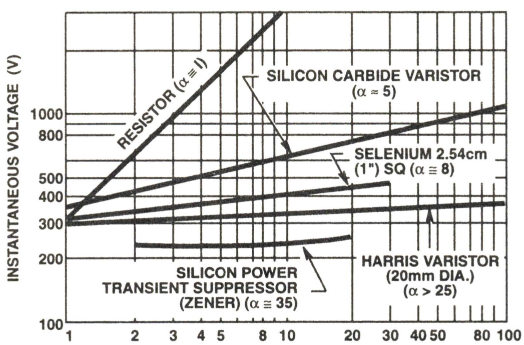


FIGURE 3. V-I CHARACTERISTIC OF FOUR TRANSIENT SUPPRESSOR DEVICE

The amount of standby power that a circuit can tolerate may be the deciding factor in the choice of a suppressor. Though high-alpha devices have low standby power at the nominal design voltage, a small line-voltage rise would cause a dramatic increase in the standby power. Figure 4 shows that for a zener-diode suppressor, a 10% increase above rated voltage increases the standby power dissipation above its rating by a factor of 30. But for a low-alpha device, such as silicon carbide, the standby power increases by only 1.5 times.

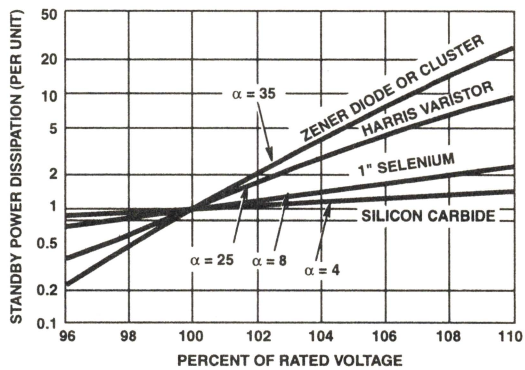
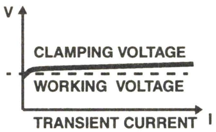
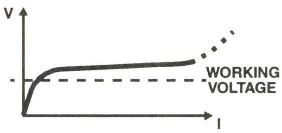
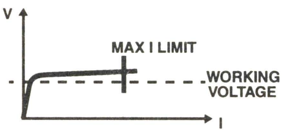
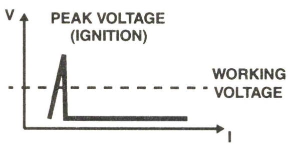
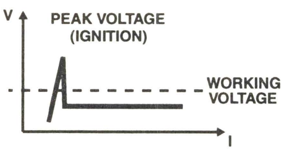
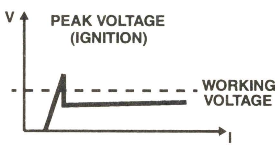
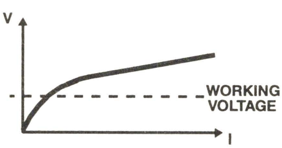
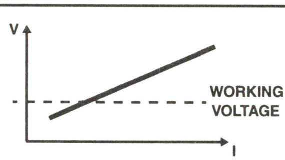


FIGURE 4. CHANGES IN STANDBY POWER ARE CONSIDERABLY GREATER WHEN THE SUPPRESSOR'S ALPHA IS HIGH

Typical volt-time curves of a gas discharge device are shown in Figure 5 indicating an initial high clamping voltage. The gas-discharge suppressor turns on when the transient pulse exceeds the impulse sparkover voltage. Two representative surge rates 1kV/μs and 20kV/μs are shown in Figure 5. When a surge voltage is applied, the device turns on at some point within the indicated limits. At 20kV/μs, the discharge unit will sparkover between 600V and 2500V. At 1kV/μs, it will sparkover between 390V and 1500V.

TABLE 2. CHARACTERISTICS AND FEATURES OF TRANSIENT VOLTAGE SUPPRESSOR TECHNOLOGY

V-I CHARACTERISTICS	DEVICE TYPE	LEAK-AGE	FOLLOW ON I	CLAMPING VOLTAGE	ENERGY CAPA-BILITY	CAPACI-TANCE	RE-SPONSE TIME	COST
	Ideal Device	Zero To Low	No	Low	High	Low Or High	Fast	Low
	Zinc Oxide Varistor	Low	No	Moderate To Low	High	Moderate To High	Fast	Low
	Zener	Low	No	Low	Low	Low	Fast	High
	Crowbar (Zener - SCR Combination)	Low	Yes (Latching Holding I)	Low	Medium	Low	Fast	Moder-ate
	Spark Gap	Zero	Yes	High Ignition Voltage Low Clamp	High	Low	Slow	Low To High
	Triggered Spark Gap	Zero	Yes	Lower Ignition Voltage Low Clamp	High	Low	Moderate	Moderate
	Selenium	Very High	No	Moderate To High	Moderate To High	High	Fast	High
	Silicon Carbide Varistor	High	No	High	High	High	Fast	Low

The gas discharge device may experience follow-current. As the AC voltage passes through zero at the end of every half cycle the arc will extinguish, but if the electrodes are hot and the gas is ionized, it may reignite on the next cycle. Depending on the power source, this current may be sufficient to cause damage to the electrodes. The follow current can be reduced by placing a limiting resistor in series with the device, or, selecting a GDT specifically designed for this application with a high follow-current threshold.

The gas discharge device is useful for high current surges and it is often advantageous to provide another suppression device in a combination that allows the added suppressor to protect against the high initial impulse. Several hybrid combinations with a varistor or avalanche diode are possible.

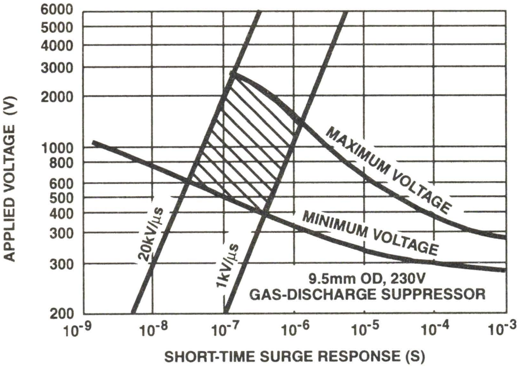


FIGURE 5. IMPULSE BREAKOVER OF A GAS-DISCHARGE DEVICE DEPENDS UPON THE RATE OF VOLTAGE RISE AS WELL AS THE ABSOLUTE VOLTAGE LEVEL

Comparison of Zener Diode and Harris Varistor Transient Suppressors

Peak Pulse Power

Transient suppressors have to be optimized to absorb large amounts of power or energy in a short time duration: nanoseconds, microseconds, or milliseconds in some instances.

Electrical energy is transformed into heat and has to be distributed instantaneously throughout the device. Transient thermal impedance is much more important than steady state thermal impedance, as it keeps peak junction temperature to a minimum. In other words, heat should be instantly and evenly distributed throughout the device.

The varistor meets these requirements: an extremely reliable device with large overload capability. Zener diodes dissipate electrical energy into heat in the depletion region of the die, resulting in high peak temperature.

Figure 6 shows Peak Pulse Power vs Pulse width for the V8ZA2 and the P6KE 6.8, the same devices compared for leakage current.

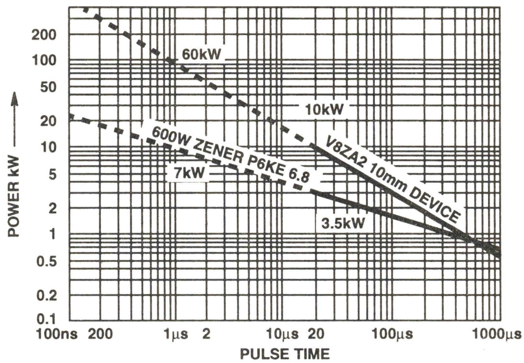


FIGURE 6. PEAK PULSE POWER vs PULSE TIME

At 1ms, the two devices are almost the same. At 2µs the varistor is almost 10 times greater, 7kW for the P6KE 6.8 Zener vs 60kW for the varistor V8ZA2.

Clamping Voltage

Clamping voltage is an important feature of a transient suppressor. Zener diode type devices have lower clamping voltages than varistors. Because these protective devices are connected in parallel with the device or system to be protected, a lower clamping voltage can be advantageous in certain applications.

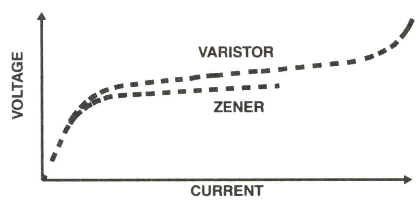


FIGURE 7. CHARACTERISTICS OF ZENER AND VARISTOR

Speed of Response

Response times of less than 1ps are sometimes claimed for zener diodes, but these claims are not supported by data in practical applications. For the varistor, measurements were made down to 500ps with a voltage rise time (dv/dt) of 1 million volts per microsecond. These measurements are described in Application Note AN9767. Another consideration is the lead effect. Detailed information on the lead effect can be found further in this section and in Application Note AN9773. In summary, both devices are fast enough to respond to real world transient events.

Leakage Current

Leakage current can be an area of misconception when comparing a varistor and zener diode, for example. Figure 8 shows a P6KE 6.8 and a V8ZA2, both recommended by their manufacturers for protection of integrated circuits having 5V supply voltages.

The zener diode leakage is about 100 times higher at 5V than the varistor, 200µA vs less than 2µA, in this example.

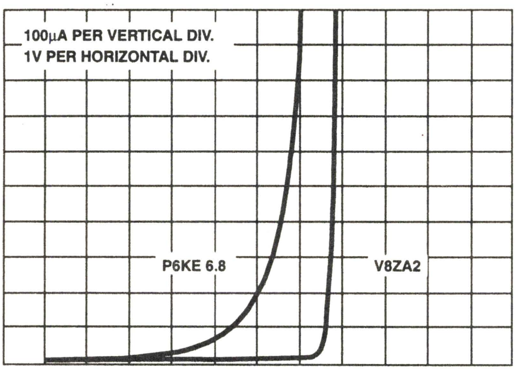


FIGURE 8. CHARACTERISTIC OF ZENER P6KE 6.8 vs HARRIS VARISTOR V8ZA2

The leakage current of a zener can be reduced by specifying a higher voltage device.

"Aging"

It has been stated that a varistor's V-I characteristic changes every time high surge current or energy is subjected to it. That is not the case.

As illustrated in Figure 9, the V-I characteristic initially changed on some of the devices, but returned to within a few percent of its original value after applying a second or third pulse. To be conservative, peak pulse limits have been established on data sheets. In many cases, these limits have been exceeded many fold without harm to the device. This does not mean that established limits should be exceeded, but rather, viewed in perspective of the definition of a failed device. A "failed" varistor device shows a ±10% change of the V-I characteristic at the 1mA point.

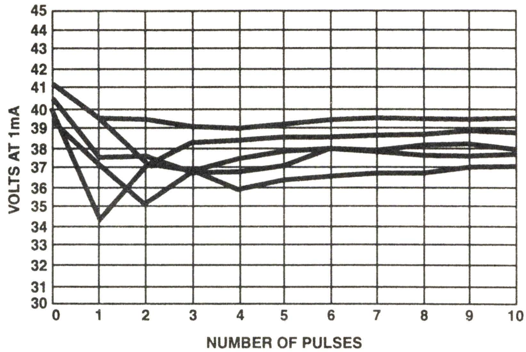


FIGURE 9. 250A PULSE WITHSTAND CAPABILITIES

Failure Mode

Varistors subjected to energy levels beyond specified ratings may be damaged. Varistors fail in the short circuit mode. Subjected to high enough energy, however, they may physically rupture or explode, resulting in an open circuit condition. These types of failures are quite rare for properly selected devices because of the large peak pulse capabilities inherent in varistors.

Zeners can fail either short or open. If the die is connected by a wire, it can act as a fuse, disconnecting the device and resulting in an Open circuit. Designers must analyze which failure mode, open or short, is preferred for their circuits.

When a device fails during a transient, a short is preferred, as it will provide a current path bypassing and will continue to protect the sensitive components. On the other hand, if a device fails open during a transient, the remaining energy ends up in the sensitive components that were supposed to be protected.

Another consideration is a hybrid approach, making use of the best features of both types of transient suppressors (See Figure 10).

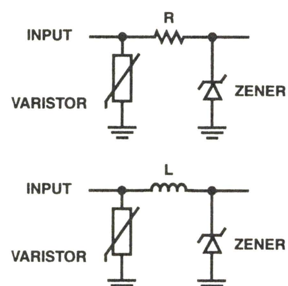


FIGURE 10. HYBRID PROTECTION USING VARISTORS, ZENERS, R AND L

Capacitance

Depending on the application, transient suppressor capacitance can be a very desirable or undesirable feature. Varistors in comparison to zener diodes have a higher capacitance. In DC circuits capacitance is desirable, the larger the better. Decoupling capacitors are used on IC supply voltage pins and can in many cases be replaced by varistors, providing both the decoupling and transient voltage clamping functions.

The same is true for filter connectors where the varistor can perform the dual functions of providing both filtering and transient suppression.

There are circuits however, where capacitance is less desirable, such as high frequency digital or some analog circuits.

As a rule the source impedance of the signal and the frequency as well as the capacitance of the transient suppressor should be considered.

The current through C_P is a function of dv/dt and the distortion is a function of the signal's source impedance. Each case must be evaluated individually to determine the maximum allowable capacitance.

The structural characteristics of metal-oxide varistors unavoidably result in an appreciable capacitance between the device terminals, depending on area, thickness and material processing. For the majority of power applications, this capacitance can be of benefit. In high-frequency applications, however, the effect must be taken into consideration in the overall system design.

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For Harris documents available on the web, see http://www.semi.harris.com/
Harris AnswerFAX (407) 724-7800.

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[2] Philipp, H.R. and L.M. Levinson, "Low Temperature Electrical Studies in Metal Oxide Varistors - A Clue to Conduction Mechanisms," Journal of Applied Physics, Vol. 48, April 1977, pp. 1621-1627.

[3] Philipp, H.R. and L.M. Levinson, "Zinc Oxide for Transient Suppression," IEEE Trans. PHP, December 1977.

[4] "Surge Arresters for Alternating Current Power Circuits," ANSI Standard C62.1, IEEE Standard 28.

[5] "Lightning Arresters. Part I: Nonlinear Resistor Type Arresters for AC Systems," IEC Recommendation 99-1,1970.

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[8] Martzloff, F.D., "The Development of a Guide on Surge Voltages in Low - Voltage AC Power Circuits," Report 81CRD047, General Electric, Schenectady, New York, 1981.

[9] Martzloff, F.D., "Varistor versus Environment: Winning the Rematch," Report 85CRD037, General Electric, Schenectady, New York, May 1985.

Harris Semiconductor

APP NOTE

No. AN9769 January 1998 Harris Suppression Products

An Overview of Electromagnetic and Lightning Induced Voltage Transients

Introduction

This Note is an overview of the sources and nature of various transient overvoltages, and the problems that may result.

Transients in electrical circuits result from the sudden release of previously stored energy. This energy can be stored within the circuit and released by a voluntary or controlled switching action or it can be outside the circuit and injected or coupled into the circuit of interest.

Transients may occur either in repeatable fashion or as random impulses. Repeatable transients, such as commutation voltage spikes, inductive load switching, etc., are more easily observed, defined and suppressed. Random transients occur at unpredictable times, at remote locations, and may require installation of monitoring instruments to detect their occurrence. Experience has been accumulated to provide reasonable guidelines of the transient environments in low voltage AC power circuits, [1, 2] telecommunications equipment [3] and automotive electrical systems.[4]

Effective transient overvoltage protection from a clamping device requires that the impulse energy be dissipated in the suppressor and the voltage held low enough to ensure the survival of circuit components. The following sections will discuss in detail the two categories of transients, how they occur, their effects and their detection.

Repeatable Transients

A sudden change in the electrical conditions of any circuit will cause a transient voltage to be generated from the energy stored in circuit inductance and capacitance. The rate of change in current (di/dt) in an inductor (L) will generate a voltage equal to -L di/dt, and it will be of a polarity that causes current to continue flowing in the same direction.

It is this effect that accounts for most switching-induced transient overvoltages. It occurs as commutating spikes in power conversion circuits, when switching loads and under fault conditions. The effect is brief, since the source is limited to the energy stored in the inductance ($1/2Li^2$), and it is generally dissipated at a high instantaneous power (Energy = power x time). But the simple effect of one switching operation can be repeated several times during a switching sequence (consider arcing in the contact gap of a switch), so that cumulative effects can be significant.

Energizing the Transformer Primary

When a transformer is energized at the peak of the supply voltage, the coupling of this voltage step function to the stray capacitance and inductance of the secondary winding can generate an oscillatory transient voltage with a peak amplitude up to twice the normal peak secondary voltage (Figure 1).

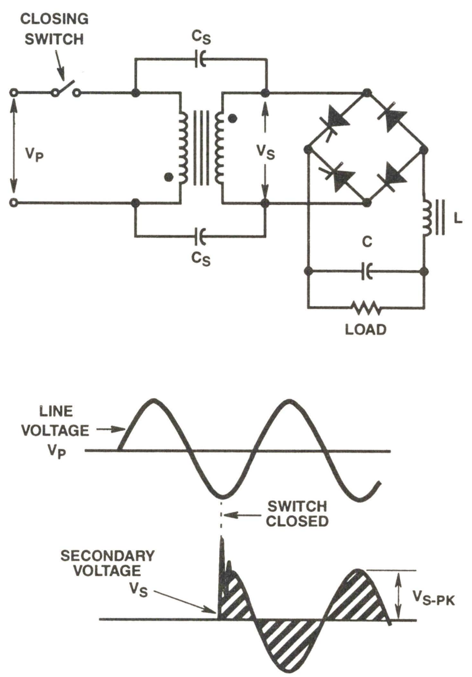


FIGURE 1. VOLTAGE TRANSIENT CAUSED BY ENERGIZING TRANSFORMER PRIMARY

Subsequent oscillations depend on the L and C parameters of the circuit. Another important point to remember is that the secondary side will be part of a capacitive divider network in series with the transformer interwinding capacitance (C_S). This capacitively coupled voltage spike has no direct relationship to the turns ratio of the transformer, so that it is conceivable that the secondary circuit can see a substantial fraction of the peak applied primary voltage.

De-Energizing the Transformer Primary

The opening of the primary circuit of a transformer generates extreme voltage transients, especially if the transformer drives a high impedance load. Transients in excess of ten times normal voltage have been observed across power semiconductors when this type of switching occurs.

Interrupting the transformer magnetizing current, and the resulting collapse of the magnetic flux in the core, couples a high voltage transient into the transformer secondary winding, as shown in Figure 2.

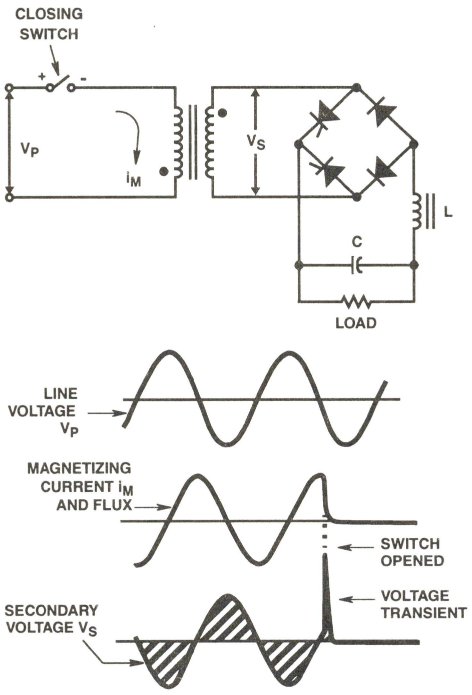


FIGURE 2. VOLTAGE TRANSIENT CAUSED BY INTERRUPTION OF TRANSFORMER MAGNETIZING CURRENT

Unless a low-impedance discharge path is provided, this burst of transient energy appears across the load. If this load is a semiconductor device or capacitor with limited voltage capabilities, that component may fail. The transients produced by interrupting the magnetizing current are usually quite severe. For example, the stored energy in the magnetizing field of a 150kVA transformer can be 9J.

Fault with Inductive Power Source

If a short develops on any power system, devices parallel to the load may be destroyed as the fuse clears.

When the fuse or circuit breaker of Figure 3 opens, it interrupts the fault currents causing the slightly inductive power source to generate a high voltage (-L di/dt), and high energy ($1/2Li^2$), transient across any parallel devices. Suddenly interrupting a high current load will have a similar effect.

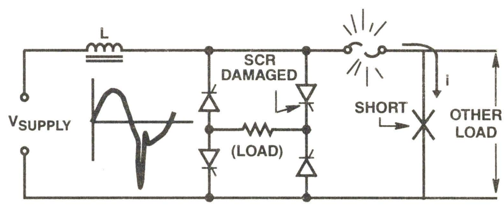


FIGURE 3. VOLTAGE TRANSIENT CAUSED BY FUSE BLOWING DURING POWER FAULT

Switch Arcing

When current in an inductive circuit, such as a relay coil or a filter reactor, is interrupted by a contactor, the inductance tries to maintain its current by charging the stray capacitance. Similar action can take place during a closing sequence if the contacts bounce open after the initial closing as in Figure 4. The high initial charging current will oscillate in the inductance and capacitance at a high frequency. When the voltage at the contact rises, breakdown of the gap is possible since the distance is still very small during the opening motion of the contact. The contact arc will clear at the current zero of the oscillation but it will restrike as the contact voltage rises again. As the contacts are moving farther apart, each restrike must occur at a higher and higher voltage until the contact succeeds in interrupting the current.

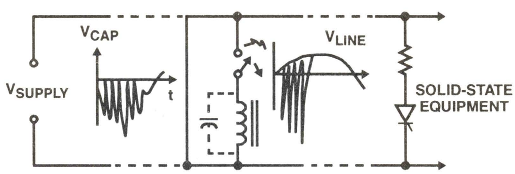
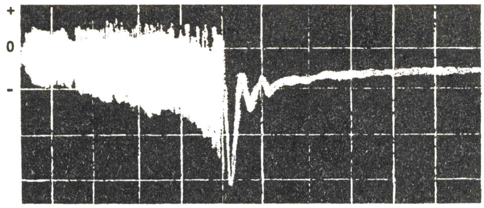


FIGURE 4. VOLTAGE TRANSIENTS CAUSED BY SWITCH ARCING

This restrike and escalation effect is particularly apparent in Figure 5, where a switch opens a relay coil of 1H, having about 0.001μF of distributed (stray) capacitance in the winding. Starting with an initial DC current of a 100mA, the circuit produces hundreds of restrikes (hence, the "white" band on the oscillogram) at high repetition rate, until the circuit clears, but not before having reached a peak of 3kV in contrast to the initial 125V in the circuit.



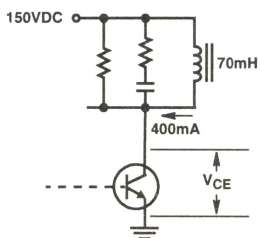
HORIZONTAL -t, 500μs/DIV., VERTICAL -V, 1.0kV/DIV

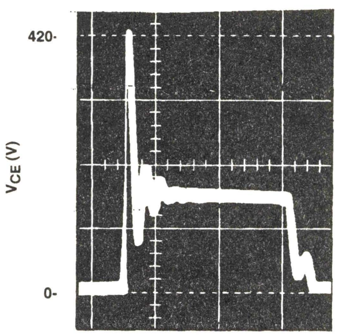
FIGURE 5. VOLTAGE ESCALATION DURING RESTRIKES

Electromechanical contacts generate transients which they generally can survive. However, in the example just discussed, the 2.5ms long sequence of restrikes and attendant high current may be damaging to the contacts. Also, the transients injected into the power system during the restrike can be damaging to other loads.

In an attempt to eliminate electromechanical switches and their arcing problem, solid-state switches are recommended with good reason! However, if these switches are applied without discrimination in inductive circuits, the very effectiveness of the interruption can lead to the generation of high voltage transients.

In the example of Figure 6, the transistor used for switching 400mA in a 70mH solenoid is exposed to 420V spikes, although the circuit voltage is only 150V.





50ms/DIVISION

FIGURE 6. TRANSISTOR SWITCHING TRANSIENT

Whenever possible, a system should be examined for potential sources of transient overvoltage so they can be eliminated at the source, for one source can affect many components. If the sources are many (or unidentifiable) and the susceptible components few, it may be more practical then to apply suppression at the components.

Random Transients

Frequently, transient problems arise from the power source feeding the circuit. These transients create the most consternation because it is difficult to define their amplitude, duration and energy content. The transients are generally caused by switching parallel loads on the same branch of a distribution system, although they also can be caused by lightning. Communication lines, such as alarm and telephone systems, are also affected by lightning and power system faults.

To deal with random transients, a statistical approach has been taken to identify the nature of line overvoltages. While recordings of transients have been made, one cannot state that on a specific system there is an “X” probability of encountering a transient voltage of “Y” amplitude. Therefore, one is limited to quoting an “average” situation, while being well aware that large deviations from this average can occur, depending on the characteristics of the specific system.

In the following sections, the recorded experiences of three types of systems will be described. These are: 1) AC power lines (up to 1000V); 2) telecommunication systems; and 3) automotive systems.

Transients on AC Power Lines

Data collected from various sources has provided the basis for this guide to transient overvoltages.[1, 5, 6, 7, 8]

Amplitude and Frequency of Occurrence

The amplitude of transient recordings covers the range from harmless values just above normal voltage to several kilovolts. For 120V AC lines, flashover of the typical wiring spacing produces an upper limit between 6kV and 8kV. Ironically, the better the wiring practices, the higher the flashover, allowing higher transients to exist in the wiring system. Studies of the frequency of occurrence and amplitude agree on an upper limit and a relative frequency of occurrence. Figure 7 shows frequency as a function of amplitude. Experience indicates that devices with less than 2kV withstand capability will have poor service life in the unprotected residential environment. Prudent design will aim for 3kV capability, although, where safety is of the utmost concern, designing for 6kV can cope with these rare but possible occurrences.

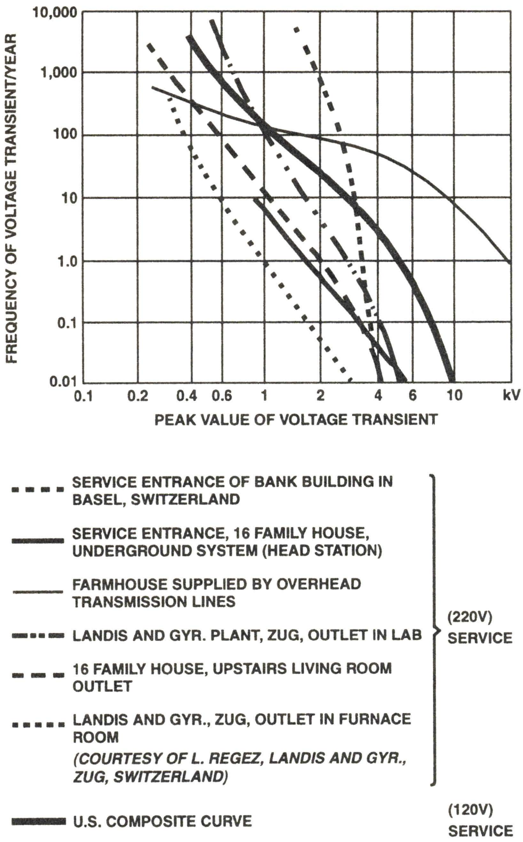


FIGURE 7. FREQUENCY OF OCCURRENCE OF TRANSIENT OVER-VOLTAGES IN 220V AND 120V SYSTEMS

For systems of higher voltages (220V, 240V, 480V), limited data is available for U.S. systems. However, the curves of Figure 8 indicate the difference between the two classes, 120V and 220V systems, is smaller than the differences within each class.[8] One can conclude that the amplitude of the transient depends more upon the amount of externally coupled energy and the system impedance than upon the system voltage.

For internal switching transients in the power system, Figure 8 shows the relationship (computed and measured) between system voltage and transient peaks.[8] Clearly, there is no direct linear increase of the transient amplitude as the system voltage is increased.

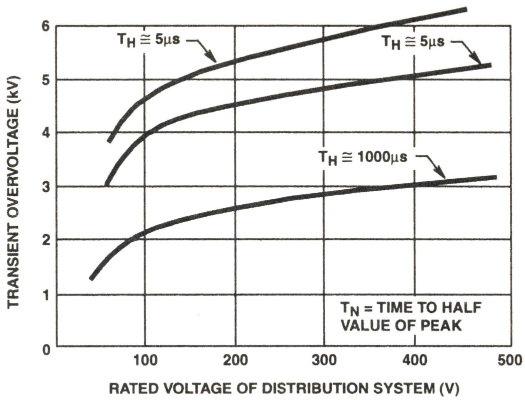


FIGURE 8. SWITCHING VOLTAGE TRANSIENTS AS A FUNCTION OF THE SYSTEM VOLTAGE FOR THREE VALUES OF THE TRANSIENT TAIL (TIME TO HALF-VALUE) - (DATA COURTESY OF L. REGEZ, LANDIS AND GYR., ZAG, SWITZERLAND)

Some indication of the uncertainty concerning the expected transient level can be found in the industrial practice of choosing semiconductor ratings. Most industrial users of power semiconductors choose semiconductor voltage ratings from 2.0 to 2.5 times the applied peak steady-state voltage, in conjunction with rudimentary transient suppression, in order to ensure long-term reliability. Whether or not this ratio is realistically related to actual transient levels has not been established; the safety factor is simply chosen by experience. While it is dangerous to argue against successful experience, there are enough cases where this rule of thumb is insufficient and thus a more exact approach is justified. Another objection to the indiscriminate rule of thumb is economic. Specifying 2.5 times the peak system voltage results in a high price penalty for these components. It is normally unrealistic and uneconomical to specify semiconductors that should withstand transients without protection. The optimum situation is a combination of low cost transient protection combined with lower cost semiconductors having lower voltage ratings.

Duration, Waveform and Source Impedance

There is a lack of definitive data on the duration, waveform and source impedance of transient overvoltages in AC power circuits. These three parameters are important for estimating the energy that a transient can deliver to a suppressor. It is desirable to have a means of simulating the environment through a model of the transient overvoltage pulse. Suggestions have been made to use standard impulses initially developed for other applications. For instance, the classical 1.2 x 50μs unidirectional voltage impulse specified in high voltage systems has been proposed.[9] Also the repetitive burst of 1.5MHz oscillations ("SWC") specified for low-voltage and control systems exposed to transients induced by high-voltage disconnect switches in utility switch yards is another suggestion.[10]

Working Groups of the IEEE and the International Electrotechnical Commission have developed standard test waves and source impedance definitions. These efforts are aiming at moving away from a concept whereby one should duplicate environmental conditions and towards a concept of one standard wave or a few standard waves arbitrarily specified. The justifications are that equipments built to meet such standards have had satisfactory field experience and provide a relative standard against which different levels of protection can be compared. A condition for acceptance of these standard waves is that they be easy to produce in the laboratory.[11] This is the central idea of the TCL (Transient Control Level) concept which is currently being proposed to users and manufacturers in the electronics industry. Acceptance of this concept will increase the ability to test and evaluate the reliability of devices and systems at acceptable cost.

Telecommunication Line Transients

Transient overvoltages occurring in telephone lines can usually be traced to two main sources: lightning and 50Hz/60Hz power lines. Lightning overvoltage is caused by a strike to the conductor of an open wire system or to the shield of a telephone cable. Most modern telephone lines are contained in shielded cables. When lightning or other currents flow on the shield of a cable, voltages are induced between the internal conductors and the shield.[12] The magnitude of the induced voltages depend on the resistance of the shield material, openings in its construction, and on the dielectric characteristics and surge impedance of the cable.

The close proximity of telephone cables and power distribution systems, often sharing right-of-way-poles and even ground wires, is a source of transient overvoltages for the telephone system. Overvoltages can arise from physical contact of falling wires, electromagnetic induction, and ground potential rise. Application Note AN9774 presents a detailed discussion of lightning-induced and power system-induced transients.

Automobile Transients

Four principal types of voltage transients are encountered in an automobile. These are "load dump," alternator field decay, inductive switching and mutual coupling.[4] In addition, service "Jump starts" with 24V batteries may occur.

The load dump transient is the most severe and occurs when the alternator current loading is abruptly reduced. The most demanding case is often initiated by the disconnection of a partially discharged battery due to defective terminal connections. Transient voltages have been reported over 100V lasting up to 500ms with energy levels in the range of tens to hundreds of joules.

Switching of inductive loads, such as motors and solenoids, will create negative polarity transient voltages with a smaller positive excursion. The voltage waveform has been observed to rise to a level of -210V and +80V and last as long as 320μs. The impedance to the transient is unknown, leading some designers to test with very low impedance, resulting in the use of more expensive components than necessary.

The alternator field decay transient is essentially an inductive load switching transient. When the ignition switch is turned off, the decay of the alternator field produces a negative voltage spike, whose amplitude is dependent on the voltage regulator cycle and load. It varies between -40V to -100V and can last 200ms.

Application Note AN9312 provides a comprehensive review of automotive transients and practical suppression techniques to protect automotive electronics.

Effects of Voltage Transients

Effects on Semiconductors

Frequently, damage occurs when a high reverse voltage is applied to a non-conducting PN junction. The junction may avalanche at a small point due to the non-uniformity of the electric field. Also, excess leakage current can occur across the passivated junction between the terminations on the die surface. The current can create a low resistance channel that degrades the junction blocking voltage capability below the applied steady-state voltage. In the avalanche case, thermal runaway can occur because of localized heating building up to cause a melt-through which destroys the junction.

If the base-emitter junction of a transistor is repetitively "avalanched" or "zenered" to a high current level by a reverse pulse, the forward current gain may be degraded. The triggering sensitivity of a thyristor can be reduced in the same manner by "zenering" the gate-cathode junction. Thyristors can also be damaged if turned on by a high voltage spike (forward breakover) under bias conditions that allow a rate of current increase (di/dt) beyond device capability. This will occur in virtually all practical circuits because the discharge of the RC dv/dt protection circuits will exceed device capability for di/dt and destroy the thyristor.

Effects on Electromechanical Contacts

The high voltage generated by breaking current to an inductor with a mechanical switch will ultimately cause pitting, welding, material transfer, or erosion of the contacts. The nature of ultimate failure of the contacts depends upon such factors as the type of metal used, rate of opening, contact bounce, atmosphere, temperature, steady-state and inrush currents, and AC or DC operation. Perhaps most important is the amount of energy dissipated in each operation of the contacts.

The actual breaking of current by a set of contacts is a complex operation. The ultimate break occurs at a microscopic bridge of metal which, due to the inductive load, is forced to carry nearly all the original steady-state current. Ohmic heating of this bridge causes it to form a plasma, which will conduct current between the contacts when supplied with a current and voltage above a certain threshold. The inductor, of course, is more than happy to supply adequate voltage ($E_L = -L\ di/dt$). As the contacts separate and the current decreases, a threshold is reached, and the current stops abruptly ("chopping"). Inductor current then charges stray

capacitances up to the breakdown voltage of the atmosphere between the contacts. (For air, this occurs at 30kV/in.) The capacitance discharges and recharges repeatedly until all the energy is dissipated. This arc causes sufficient contact heating to melt, oxidize, or "burn" the metal, and when the contacts close again, the contacts may form a poorer connection. If they "bounce," or are closed soon after arcing, the contacts may be sufficiently molten to weld closed. Welding can also occur as a result of high inrush currents passing through the initially formed bridges upon closing.

Good suppression techniques can significantly reduce the amount of energy dissipated at the contacts, with a proportional increase in operating life. Suppression can also reduce the noise generated by this arcing. Voltage-limiting devices are particularly suited to preventing the noisy high-voltage "showering" arc described above and illustrated in Figure 4.

Effects on Insulation

Transient overvoltages can cause breakdown of insulation, resulting in either a temporary disturbance of device operation or instantaneous failure. The insulating level in the former case will be weakened leading to premature failure.

The severity of the breakdown varies with the type of insulation air, liquid, or solid. The first two tend to be self-healing, while breakdown of solid insulation (generally organic materials) is generally a permanent condition.

Air clearances between metal parts in electrical devices and power wiring constitute air gaps, which behave according to the usual physics of gap breakdown (pressure, humidity, shape of electrodes, spacing). The International Electrotechnical Commission Working Group on Low Voltage Insulation Coordination has developed a table listing the minimum clearances in air for optimum and worst case electric field conditions existing between electrodes.[13] Breakdown of the clearance between metal parts can be viewed as a form of protection, limiting the overvoltage on the rest of the circuit. However, this protection is dependent upon the likelihood of AC line current that may follow during the arc breakdown. Normally, power-follow current should cause the system fuse or breaker to function. If the power-follow current heat is limited by circuit impedance, then the system fusing may not operate. In that case, sufficient heat could be generated to cause a fire. Experience with power wiring has shown that metal clearances can flash-over harmlessly under transient voltage conditions, and power-follow problems are rare, but can occur.

In liquid dielectrics, an impulse breakdown not followed by a high current is normally harmless. However, this type of breakdown is of limited interest in low-voltage systems, where liquid insulation systems are seldom used, except in combination with some degree of solid insulation.

Breakdown of solid insulation generally results in local carbonization of an organic material. Inorganic insulation materials are generally mechanically and permanently damaged. When no power-follow current takes place, the system can recover and continue operating. However, the degraded insulating characteristic of the material leads to breakdown at progressively lower levels until a mild overvoltage, even within AC line overvoltage tolerances, brings about the ultimate permanent short circuit.

Breakdown along surfaces of insulation is the concern of "creepage" specifications. The working group of IEC cited above is also generating recommendations on creepage distances. The behavior of the system where creepage is concerned is less predictable than is breakdown of insulation in the bulk because the environment (dust, humidity) will determine the withstand capability of the creepage surface.

Noise Generation

With the proliferation of low level logic circuits, electrical noise problems are of concern, especially in environments with electromechanical devices. Noise can upset automatic manufacturing equipment, medical equipment, computers, alarms and thyristor-controlled machinery. Such disruption can cause loss of product, time, money, and even human life.

Noise enters a system either directly on wires or grounds connected to the source or through coupling to adjacent wires. Noise problems are dealt with by suppression at the source, at the receiver, or by isolation. Noise is induced when stray capacitance or mutual inductance links the susceptible system to the noise-generating system. The amplitude of the induced noise is then related to the rate-of-change of either the current or the voltage of the noise source. The low-frequency components of the induced noise (which are hardest to filter out) are a result of the amplitude of the original transient impulses.

Frequently, the source of noise is the arcing of contacts breaking current through an inductor, such as a relay coil. A low-current, high-voltage arc creates a series of brief discharges of a damped oscillatory nature, occurring at kHz to MHz frequencies with amplitudes of from 300V to several thousand volts. These pulses and their reflections from loads and line discontinuities travel along the power wires, easily inducing noise in adjacent wiring. This interference is best eliminated by preventing it at the source (the inductance) with voltage-limiting devices such as varistors.

Rate of Rise vs Amplitude

Interference coupled into electronic systems, as opposed to damage, is most often associated with the rate of rise of the interfering signal rather than its peak amplitude. Consequently, low-amplitude fast-rise interference which is dealt only by the capacitance of a varistor until the clamping level is reached by the impinging interference may still be a problem with the circuit if attempts are made to suppress it with a retrofit varistor at the location of the victim. A much more effective cure would be to install the appropriate varistor near the source of the offending surge, so that the interference radiated or coupled by the surge would be confined to the immediate vicinity of the offending source.

Transient Testing and Standards

It is desirable to have test criteria and definitions that provide a common engineering language beneficial to both the user and manufacturer of surge protective devices. Regretfully, different terms have come into use through industry practice over the years. Testing standards have tended to proliferate as the measurement objective defines either the characteristics of the protective device or the environment of the application.

Standards vary depending on system usage, whether protection is intended for power lines, telecommunications, automotive, or aircraft, to name a few. Each environment also has been defined with less than full precision leading to additional diversity on choice of waveshape, amplitude and duration.

Several organizations such as ANSI/IEEE, IEC, UL, NEMA are currently developing guidelines and standards to describe what the environment is likely to be, on the basis of accumulated recording and field experience. From this, test specifications are being prepared[16, 17, 18, 19] that will allow objectives are realistic evaluation of suppressor applications.

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The Development of a Guide† on Surge Voltages in Low-Voltage AC Power Circuits

Author: F.D. Martzloff, Fellow, IEEE

Introduction

Surge voltages occurring in AC power circuits can be the cause of misoperation or product failure for residential as well as industrial systems. The problem has received increased attention in recent years because miniaturized solid state devices are more sensitive to voltage surges (spikes and transients) than were their predecessors.

Although surge voltage amplitudes and their frequency of occurrence on unprotected circuits are well known, their waveshapes and energy content are less well known. On the basis of measurements, statistics, and theoretical considerations, a practical guide for outlining the environment for use in predicting extreme waveshapes and energy content can nevertheless be established. A Working Group of the Surge Protective Devices Committee has completed such a descriptive Guide.†† The Guide proposes two waveforms, one oscillatory, the other unidirectional, depending on the location within the power system. It also includes recommendations for source impedance or short-circuit current. While the major purpose of the Guide is to describe the environment, a secondary purpose is to lead toward standard tests.

The Origins of Surge Voltages

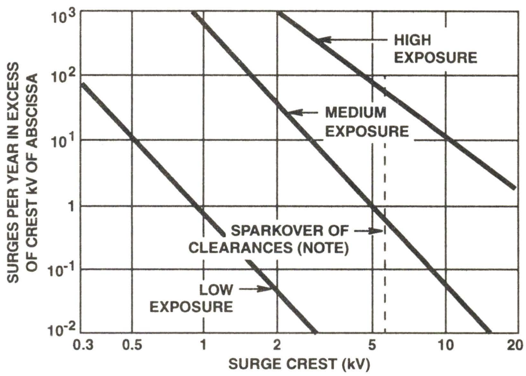
Surge voltages occurring in low-voltage AC power circuits originate from two major sources: system switching transients and direct or indirect lightning effects on the power system. System switching transients can be divided into transients associated with (1) major power system switching disturbances, such as capacitor bank switching; (2) minor switching near the point of interest, such as an appliance turnoff in a household or the turnoff of other loads in an individual system; (3) resonating circuits associated with switching devices, such as thyristors; and (4) various system faults, such as short circuits and arcing faults.

Measurements and calculations of lightning effects have been made to yield data on what levels can be produced, even if the exact mechanism of any particular surge is unknown. While the data have been recorded primarily on 120, 220/380, or 277/480V systems, the general conclusions should be valid for 600V systems. To the extent that surge voltages are produced by a discrete amount of energy being dumped into a power system, low impedance, heavy industrial systems can be expected to experience lower peaks from surge voltages than 120V residential systems, but comparable, or greater, amounts of energy potentially available for deposition in a surge suppressor.

Rate of Occurrence and Voltage Levels In Unprotected Circuits

The rate of occurrence of surges varies over wide limits, depending on the particular power system. Prediction of the rate for a particular system is always difficult and frequently impossible. Rate is related to the level of the surges; low-level surges are more prevalent than high-level surges.

It is essential to recognize that a surge voltage observed in a power system can be either the driving voltage or the voltage limited by the sparkover of some clearance in the system. Hence, the term unprotected circuit must be understood to be a circuit in which no low-voltage protective device has been installed but in which clearance sparkover will eventually limit the maximum voltage. The distribution of surge levels, therefore, is influenced by the surge-producing mechanisms as well as by the sparkover level or clearances in the system. This distinction between actual driving voltage and voltage limited by sparkover is particularly important at the interface between outdoor equipment and indoor equipment. Outdoor equipment has generally higher clearances, hence higher sparkover levels: 10kV may be typical, but 20kV is possible. In contrast, most indoor wiring devices used in 120V-240V systems have sparkover levels of about 6kV; this 6kV level, therefore, can be selected as a typical cutoff for the occurrence of surges in indoor power systems.



NOTE: on some locations, sparkover of clearances may limit the overvoltages.

FIGURE 1. RATE OF SURGE OCCURRENCE vs VOLTAGE LEVEL AT UNPROTECTED LOCATIONS

† Condensed from a paper presented at the 1979 IEEE 14th Electrical/Electronics insulation Conference, Boston, October 9-1, 1979. Reprinted with permission of the Institute of Electrical and Electronics Engineers.

†† ANSI/1EEE C62.4l-l980 Guide on Surge Voltages in Low-Voltage AC Power Circuits.

Data collected from many sources have led to the plot shown in Figure 1. This prediction shows with certainty only a relative frequency of occurrence, while the absolute number of occurrences can be described only in terms of "low exposure," "medium exposure, or "high exposure." These exposure levels can be defined in general terms as follows:

Low Exposure - Systems in geographical areas known for low lightning activity, with little load switching activity.

Medium Exposure - Systems in geographical areas known for high lightning activity, with frequent and severe switching transients.

High Exposure - Rare but real systems supplied by long overhead lines and subject to reflections at line ends, where the characteristics of the installation produce high sparkover levels of the clearances.

The two lower lines of Figure 1 have been drawn at the same slope, since the data base shows reasonable agreement among several sources on that slope. All lines may be truncated by sparkover of the clearances at levels depending on the withstand voltage of these clearances. The "high-exposure" line needs to be recognized, but it should not be applied indiscriminately to all systems. Such application would penalize the majority of installations, where the exposure is lower.

From the relative values of Figure 1, two typical levels can be cited for practical applications. First, the expectation 3kV transient occurrence on a 120V circuit ranges from 0.01 to 10 per year at a given location a number sufficiently high to justify the recommendation of a minimum 3kV withstand capability. Second, the sparkover of wiring devices indicates that a 6kV withstand capability may be sufficient to ensure device survival indoors, but a withstand capability of 10kV, or greater, may be required outdoors.

The voltage and current amplitudes presented in the Guide attempt to provide for the vast majority of lightning strikes but should not be considered as "worst case," since this concept cannot be determined realistically. One should think in terms of the statistical distribution of strikes, accepting a reasonable upper limit for most cases. Where the consequences of a failure are not catastrophic but merely represent an annoying economic loss, it is appropriate to make a trade-off of the cost of protection against the likelihood of failure caused by a high but rare surge. For instance, a manufacturer may be concerned with nationwide failure rates, those at the upper limits of the distribution curve, while the user of a specific system may be concerned with a single failure occurring at a specific location under "worst-case conditions." Rates can be estimated for average systems, however, and even if imprecise, they provide manufacturers and users with guidance. Of equal importance is the observation that surges in the range of 1kV to 2kV are fairly common in residential circuits.

Surges occur at random times with respect to the power frequency, and the failure mode of equipment may be affected by the power frequency follow current. Furthermore, the timing of the surge with respect to the power frequency may affect the level at which failure occurs. Consequently, when the failure mode is likely to be affected, surge testing should be done with the line voltage applied to the test piece.

Waveshape of Representative Surge Voltages

Waveshapes in Actual Occurrences

Indoor - Measurements in the field, measurements in the laboratory, and theoretical calculations indicate that most surge voltages in indoor low-voltage systems have oscillatory waveshapes, unlike the well-known and generally accepted unidirectional waves specified in high-voltage insulation standards. A surge impinging on the system excites the natural resonant frequencies of the conductor system. As a result, not only are the surges typically oscillatory, but surges may have different amplitudes and waveshapes at different places in the system. These oscillatory frequencies of surges range from 5kHz to more than 500kHz. A 30kHz to 100kHz frequency is a realistic measure of a "typical" surge for most residential and light industrial AC line networks.

Outdoor and Service Entrance - Surges encountered in outdoor locations have also been recorded, some oscillatory, other unidirectional. The "classical lightning surge" has been established as 1.2/50ms for a voltage wave and 8/20ms for a current wave, but these waveshapes should not be construed as typical waves for low-voltage circuits. Lightning discharges induce oscillations, reflections, and disturbances that ultimately appear as decaying oscillations in low-voltage systems.

Because the prime concern here is the energy associated with these surges, the waveshape to be selected must involve greater energy than that associated with the indoor environment. Secondary surge arresters have a long history of successful performance, meeting the ANSI C62.1 specification, as detailed below; consequently, these specifications can be adopted as a realistic representation of outdoor waveshapes.

Selection of Representative Waveshapes

The definition of a waveshape to be used as representative of the environment is important for the design of candidate protective devices, since unrealistic requirements, such as excessive duration of the voltage or very low source impedance, place a high energy requirement on the suppressor, with a resulting cost penalty to the end user. The two requirements defined below reflect this trade-off.

Indoor - Based on measurements conducted by several independent organizations in 120V and 240V systems, the wave- shape shown in Figure 2 is reasonably representative of surge voltages in these power circuits. Under the proposed description of a "0.5μs - 100kHz ring wave," this waveshape rises in 0.5μs, then decays while oscillating at 100kHz, each peak being about 60% of the preceding peak.

Outdoor - In the outdoor and service entrance environment, as well as in locations close to the service entrance, substantial energy, or current, is still available, in contrast to the indoor environment, where attenuation has taken place. For these locations, the unidirectional impulses long established for secondary arresters are more appropriate than the oscillatory wave.

Accordingly, the recommended waveshape is 1.2/50µs for the open-circuit voltage or voltage applied to a high-impedance device, and 8/20µs for the discharge current or current in a low-impedance device. The numbers used to describe the impulse, 1.2/50 and 8/20, are those defined in IEEE Standard 28 - ANSI Standard C62.1; Figure 3 presents the waveshape and a graphic description of the numbers.

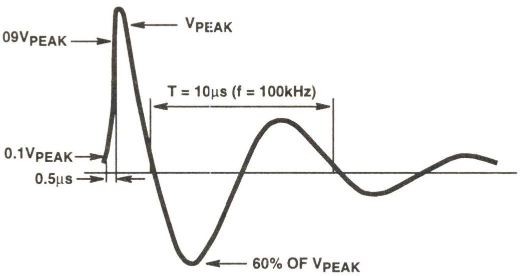


FIGURE 2. THE PROPOSED 0.5µs - 100kHz RING WAVE (OPEN-CIRCUIT VOLTAGE)

Energy and Source Impedance

General

The energy involved in the interaction of a power system with a surge source and a surge suppressor will divide between the source and the suppressor in accordance with the characteristics of the two impedances. In a gap-type suppressor, the low impedance of the arc after sparkover forces most of the energy to be dissipated elsewhere: for instance, in a resistor added in series with the gap for limiting the power-follow current. In an energy-absorber suppressor, by its very nature, a substantial share of the surge energy is dissipated in the suppressor, but its clamping action does not involve the power-follow energy resulting from the short-circuit action of a gap. It is therefore essential to the effective use of suppression devices that a realistic assumption be made about the source impedance of the surge whose effects are to be duplicated.

The voltage wave shown in Figure 2 is intended to represent the waveshape a surge source would produce across an open circuit. The waveshape will be different when the source is connected to a load having a lower impedance, and the degree to which it is lower is a function of the impedance of the source.

To prevent misunderstanding, a distinction between source impedance and surge impedance needs to be made. Surge impedance, also called characteristic impedance, is a concept relating the parameters of a line to the propagation of traveling waves. For the wiring practices of the AC power circuits discussed here, this characteristic impedance would be in the range of 150Ω to 300Ω, but because the durations of the waves being discussed (50µs to 2µs) are much longer than the travel times in the wiring systems being considered, traveling wave analyses are not useful here.

Source impedance, defined as “the impedance presented by a source energy to the input terminals of a device, or network” (IEEE Standard 100), is a more useful concept here. In the conventional Thevenin's description, the open-circuit voltage (at the terminals of the network or test generator) and the source impedance (of the surge source or test generator) are sufficient to calculate the short-circuit current, as well as any current for a specified suppressor impedance.

The measurements from which Figure 1 was derived were of voltage only. Little was known about the impedance of the circuits upon which the measurements were made. Since then, measurements have been reported on the impedance of power systems. Attempts were made to combine the observed 6kV open-circuit voltage with the assumption of a parallel 50Ω/50µH impedance.

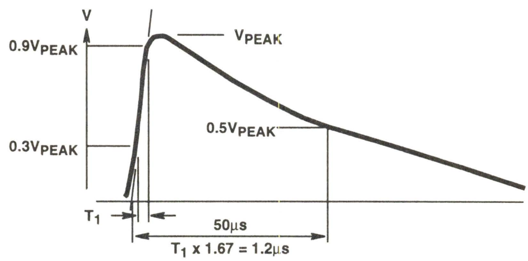


FIGURE 3A. VOLTAGE ESCALATION DURING RESTRIKES

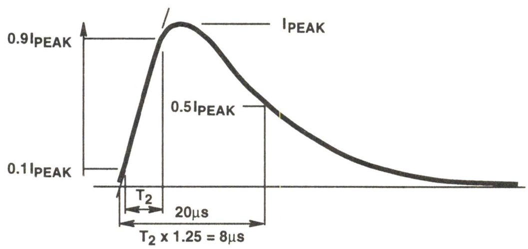


FIGURE 3B. DISCHARGE CURRENT WAVEFORM

FIGURE 3. UNIDIRECTIONAL (ANS1 STANDARD C62.1) WAVESHAPES

This combination resulted in low energy deposition capability, which was contradicted by field experience of suppressor performance. The problem led to the proposed definition of oscillatory waves as well as high-energy unidirectional waves, in order to produce both the effects of an oscillatory wave and the high-energy deposition capability.

The degree to which source impedance is important depends largely on the type of surge suppressors that are used. The surge suppressors must be able to withstand the current passed through them by the surge source. A test generator of too high an impedance may not subject the device under test to sufficient stresses, while a generator of too low an impedance may subject protective devices to unrealistically severe stresses. A test voltage wave specified without reference to source impedance could imply zero source impedance one capable of producing that voltage across any impedance, even a short circuit. That would imply an infinite surge current, clearly an unrealistic situation.

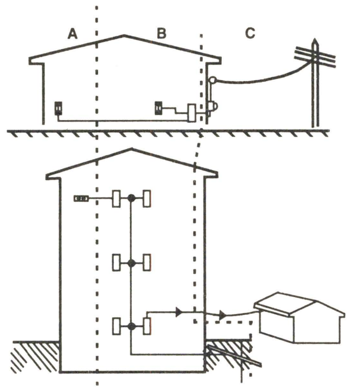
Because of the wide range of possible source impedances and the difficulty of selecting a specific value, three broad categories of building locations are proposed to represent the vast majority of locations, from those near the service entrance to those remote from it. The source impedance of the surge increases from the outside to locations well within the building. Open-circuit voltages, on the other hand, show little variation within a building because the wiring provides little attenuation. Figure 4 illustrates the application of the three categories to the wiring of a building.

For the two most common location categories, Table 1 shows the representative surge voltages and currents, with the waveforms and amplitudes of the surges, and high- or low-impedance specimen. For the discharge current shown, the last two columns show the energy that would be deposited in a suppressor clamping at 500V and 1000V, typical of 120V or 240V applications, respectively. For higher system voltages (assuming the same current values), the energy would increase in proportion to the clamping voltage of a suppressor suitable for that system voltage.

The values shown in Table 1 represent the maximum range and correspond to the "medium exposure" situation of Figure 1. For less exposed systems, or when the prospect of a failure is not highly objectionable, one could specify lower values of open-circuit voltages with corresponding reductions in the discharge currents.

The 6kV open-circuit voltage derives from two facts: the limiting action of wiring device sparkover and the unattenuated propagation of voltages in unloaded systems. The 3kA discharge current in Category B derives from experimental results: field experience in suppressor performance and simulated lightning tests. The two levels of discharge currents from the 0.5μs - 100kHz wave derive from the increasing impedance expected in moving from Category B to Category A.

Location Category C is likely to be exposed to substantially higher voltages than location Category B because the limiting effect of sparkover is not available. The "medium exposure" rates of Figure 1 could apply, with voltage in excess of 10kV and discharge currents of 10kA, or more. Installing unprotected load equipment in location Category C is not recommended; the installation of secondary arresters, however, can provide the necessary protection. Secondary arresters having 10kA ratings have been applied successfully for many years in location Category C (ANSI Standards C62.1 and C62.2).



NOTES:

A Outlets and Long Branch Circuits: All outlets at more than 10m (30 feet) from Category B with wires #14-10; All outlets at more than 20m (60 feet) from Category C with wires #14-10.

B. **Major Feeders and Short Branch Circuits:** Distribution panel devices; Bus and feeder systems in industrial plants; Heavy appliance outlets with "short" connections to the service entrance; Lighting systems in commercial.

C. **Outside and Service Entrance:** Service drop from pole to building entrance; Run between meter and distribution panel; Overhead line to detached buildings; Underground lines to well pumps.

FIGURE 4. LOCATION CATEGORIES

TABLE 1. SURGE VOLTAGES AND CURRENT DEEMED TO REPRESENT THE INDOOR ENVIRONMENT AND SUGGESTED FOR CONSIDERATION IN DESIGNING PROTECTIVE SYSTEMS

LOCATION CATEGORY	COMPARABLE TO IEC 664 CATEGORY	IMPULSE		TYPE OF SPECIMEN OR LOAD CIRCUIT	ENERGY (JOULES) DEPOSITED IN A SUPPRESSOR (NOTE 3) WITH CLAMPING VOLTAGE OF	
		WAVEFORM	MEDIUM EXPOSURE AMPLITUDE		500V (120V SYSTEM)	1000V (240V SYSTEM)
A. Long branch circuits and outlets	II	0.5ms - 100kHz	6kV	High Impedance (Note 1)	-	-
			200A	Low Impedance (Note 2)	0.8	1.6
B. Major feeders short branch circuits, and load center	III	1.2/50μs	6kV	High Impedance (Note 1)	-	-
		8/20μs	3kA	Low Impedance (Note 2)	40	80
		0.5ms - 100kHz	6kV	Low Impedance (Note 1)	-	-
			500A	High Impedance (Note 2)	2	4

NOTES:

1. For high-impedance test specimens or load circuits, the voltage shown represents the surge voltage. In making simulation tests, use that value for the open-circuit voltage of the test generator.
2. For low-impedance test specimens or load circuits, the current shown represents the discharge current of the surge (not the short-circuit current of the power system). In making simulation tests, use that current for the short-circuit current of the test generator.
3. Other suppressors which have different clamping voltages would receive different energy levels.

No. AN9771 January 1998

Harris Suppression Products

Selecting a Harris Varistor

Introduction

The varistor must operate under steady-state and transient conditions. Device ratings allow a selection of the proper size device to ensure reliable operation. The selection process requires a knowledge of the electrical environment. When the environment is not fully defined, some approximations can be made.

For most applications, the selection is a five-step process:

1. Determine the necessary steady-state voltage rating (working voltage)
2. Establish the transient energy absorbed by the varistor
3. Calculate the peak transient current through the varistor
4. Determine power dissipation requirements
5. Select a model to provide the required voltage-clamping characteristic

A final consideration is to choose the appropriate package style to suit the application.

Steady-State Voltage Rating

Consider the maximum steady-state voltage that will be applied to the varistor including any high line conditions (i.e., 110% or more of nominal voltage). Ratings are given for continuous sinusoidal AC and DC voltages. If a nonsinusoidal waveform is applied, the recurrent peak voltage should be limited to $\sqrt{2}$x $V_{M(AC)}$.

Specifications for the UltraMOV™ Series varistor, for example, are shown in Table 1 for 140V AC rated devices to illustrate the use of the ratings and specifications table.

$V_{M(AC)}$ - These models can be operated continuously with up to $140V_{RMS}$ at 50Hz - 60Hz applied. They would be suitable for $120V_{AC}$ nominal line operation and would allow for about a 120% high line condition.

$V_{M(DC)}$ - Operation up to $180V_{DC}$ applied continuously is allowed.

TABLE 1. ULTRAMOV RATINGS AND SPECIFICATIONS EXAMPLE

MODEL NUMBER	DEVICE MODEL NUMBER BRANDING	MAXIMUM RATING (85°C)					CHARACTERISTICS (25°C)				
		CONTINUOUS		TRANSIENT			VARISTOR VOLTAGE AT 1mA DC TEST CURRENT		MAXIMUM CLAMPING VOLTAGE 8 x 20µs		TYPICAL CAPACITANCE
		RMS VOLTS	DC VOLTS	ENERGY 2ms	PEAK CURRENT 8 x 20µs						
		$V_{M(AC)}$	$V_{M(DC)}$	W_{TM}	I_{TM} 2 x PULSE	I_{TM} 1 x PULSE	V_{NOM} MIN	V_{NOM} MAX	V_C	I_{PK}	f = 1MHz
		(V)	(V)	(J)	(A)	(A)	(V)		(V)	(A)	(pF)
V07E140	7V140	140	180	13.5	1200	1750	200	240	360	10	160
V10E140	10V140	140	180	27.5	2500	3500	200	240	360	25	400
V14E140	14V140	140	180	55	4500	6000	200	240	360	50	900
V20E140	20V140	140	180	110	6500	10000	200	240	360	100	1750

Varistor Nomenclature

The varistor part number includes ratings information. Some types include the working voltage, others indicate the nominal voltge. See the varistor ordering nomenclature guides below.

ULTRAMOV TYPES

V XX E XXX LX X X

DEVICE FAMILY:
Harris Varistor

DISC DIAMETER:
07, 10, 14, or 20 (mm)

ENCAPSULATION:
E = Epoxy

$V_{M(AC)RMS}$:
130 to 625 (V)

LEAD FORMATION:
L1 = Straight
L2 = Crimped
L3 = In-Line
L4 = Trim/Crimp (Bulk pack only)

PACKAGING:
B = Bulk Pack
T = Tape and Reel
A = Ammo Pack

NON-STANDARD LEAD SPACING OPTIONS (DO NOT ADD IF STANDARD) (NOTE 2):
5 = 5mm Lead Spacing
7 = 7.5mm Lead Spacing
1 = 10mm Lead Spacing

V (BA, BB, CA, CH, CP, CS, DA, DB, HA, LA, MA, NA, PA, ZA) TYPES

BA, BB, CA, CP, CS, DA, DB, HA, LA, NA, PA, VARISTOR SERIES

V 130 LA 20 A

A: Selection - Clamping Voltage (A or B)
20: Relative Energy Indicator
LA: Product Series
130: Max RMS Applied Voltage
V = Metal-Oxide Varistor (MOV)

CH, MA, ZA, VARISTOR SERIES

V 220 MA 4 A

A: Selection - Clamping Voltage (A or B)
4: Relative Energy Indicator
MA: Product Series
220: V_N(DC) Nominal Varistor Voltage
V: MOV Varistor

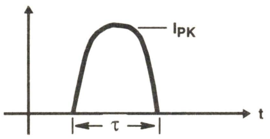
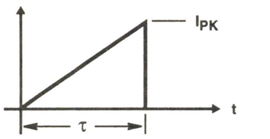
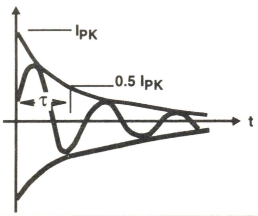
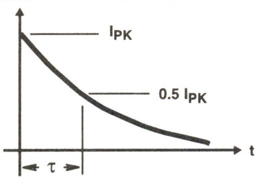
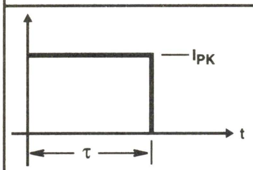
Energy

Transient energy ratings are given in the W_{TM} column of the specifications in joules (watt-second). The rating is the maximum allowable energy for a single impulse of 10/1000μs current waveform with continuous voltage applied. Energy ratings are based on a shift of V_N of less than ±10% of initial value.

When the transient is generated from the discharge of an inductance (i.e., motor, transformer) or a capacitor, the source energy can be calculated readily but, in most cases the transient is from a source external to the equipment and is of unknown magnitude. For this situation an approximation technique can be used to estimate the energy of the transient absorbed by the varistor. The method requires finding the transient current and voltage applied to the varistor. To determine the energy absorbed the following equation applies:

$$E = \int_0^{\tau} V_C(t) I(t) \Delta t = K V_C I \tau$$

where I is the peak current applied, V_C is the clamp voltage which results, τ is the impulse duration and K is a constant. K values are given in Figure 1 for a variety of waveshapes frequently encountered. The K value and pulse width correspond to the current waveform only, assuming the varistor voltage waveform is almost constant during the current impulse. For complex waveforms, this approach also can be used by dividing the shape into segments that can be treated separately.

WAVESHAPE	EQUATION	K†
	$I_{PK} \sin\left(\frac{\Pi}{\tau}t\right)$	0.637
	$I_{PK}\left(\frac{t}{\tau}\right)$	0.5
	$I_{PK}\sin(\pi t)e^{-t/\tau}$	0.86
	$I_{PK}e^{-t/1.44\tau}$	1.4
	I_{PK}	1.0

† Based upon alpha of 25 to 40

FIGURE 1. ENERGY FORM FACTOR CONSTANTS

Consider the condition where the exponential waveform shown below is applied to a V130LA1 type Harris Varistor.

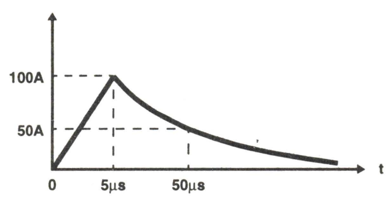


FIGURE 2.

The waveform is divided into two parts that are treated separately using the factors of Figure 1: current waveform Section (1) 0 to 5µs and (2) 5µs to 50µs. The maximum voltage across the V130LA1 at 100A is found to be 500V from the V-I characteristics of the specification sheet.

Section (1) $E = KV_CI\tau = (0.5)(500)(100)(5)(10^{-6}) = 0.13J$

Section (2) $E = KV_CI\tau = (1.4)(500)(100)(50\text{-}5)10^{-6} = \underline{3.15J}$

3.28J Total

Peak Current

The peak current rating can be checked against the transient current measured in the circuit. If the transient is generated by an inductor, the peak current will not be more than the inductor current at the time of switching. Another method for finding the transient current is to use a graphical analysis. When the transient voltage and source impedance is known, a Thevenin equivalent circuit can be modeled. Then, a load line can be drawn on the log - log, V-I characteristic as shown in Figure 3. The two curves intersect at the peak current value.

The rated single pulse current, $\mathbf{I_{TM}}$, is the maximum allowable for a single pulse of 8/20µs exponential waveform (illustrated in Application Note AN9767, Figure 21). For longer duration pulses, I_{TM} should be derated to the curves in the varistor specifications. Figure 4 shows the derating curves for 7mm size, LA series devices. This curve also provides a guide for derating current as required with repetitive pulsing. The designer must consider the total number of transient pulses expected during the life of the equipment and select the appropriate curve.

Where the current waveshape is different from the exponential waveform of Figure 11 of AN9767, the curves of Figure 4 can be used by converting the pulse duration on the basis of equivalent energy. This is easily done using the constants given in Figure 1. For example, suppose the actual current measured has a triangular waveform with a peak current of 10A, a peak voltage of 340V and an impulse duration of 500µs.

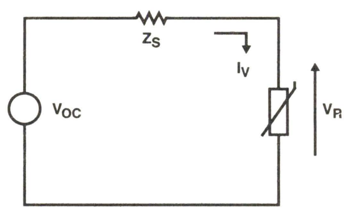


FIGURE 3A. EQUIVALENT CIRCUIT

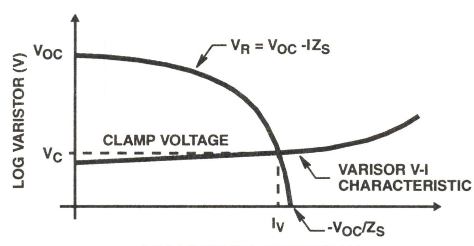


FIGURE 3B. GRAPHICAL ANALYSIS TO DETERMINE PEAK I

FIGURE 3. DETERMINING VARISTOR PEAK CURRENT FROM A VOLTAGE SOURCE TRANSIENT

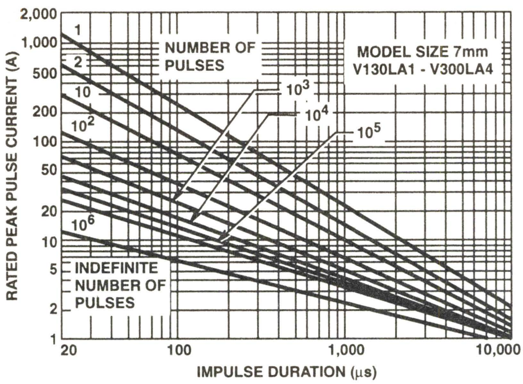


FIGURE 4. PEAK CURRENT DERATING BASED ON PULSE WIDTH AND NUMBER OF APPLIED PULSES

Then:

$E = (.5)(10)(340)(500)(10^{-6})$
$= 850mJ$

The equivalent exponential waveform of equal energy is then found from:

$E_{TRIANGULAR} = E_{EXP}$
$850mJ = 1.4\ V_C I \tau_{EXP}$

The exponential waveform is taken to have equal V_C and I values. Then,

$$\tau_{EXP} = \frac{850mJ}{1.4\ (340)\ (10)}$$
$$= 179\mu s$$

Or:

$$\tau_{EXP} = \frac{K^* \tau^*}{1.4}$$

Where: K^* and τ^* are the values for the triangular waveform and τ_{EXP} is the impulse duration for the equivalent exponential waveform.

The pulse rise portion of the waveform can be ignored when the impulse duration is five times or more longer. The maximum number of pulses for the above example would exceed 10^4 from the pulse derating curves shown in Figure 4.

Varistor Voltage

The varistor nominal voltage **(V_{NOM} or V_N)** represents the applied voltage where the varistor transitions from its "standby" mode to its low impedance "clamping" mode. It is measured at the 1mA conduction point. The minimum and maximum limit values are specified in the ratings table.

Power Dissipation Requirements

Transients generate heat in a suppressor too quickly to be transferred during the pulse interval. Power dissipation capability is of concern for a suppressor if transients will be occurring in rapid succession. Under this condition, the power dissipation required is simply the energy (watt-seconds) per pulse times the number of pulses per second. The power so developed must be within the specifications shown on the ratings tables for the specific device type. It is to be noted that varistors can only dissipate a relatively small amount of average power and are, therefore, not suitable for repetitive applications that involve substantial amounts of average power dissipation (likewise, varistors are not suitable as voltage regulation devices). Furthermore, the operating values need to be derated at temperatures above the absolute maximum limits as shown in Figure 5.

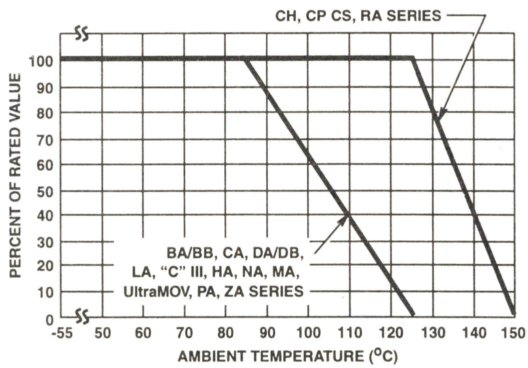


FIGURE 5. CURRENT, ENERGY, POWER DERATING vs TEMPERATURE

Voltage Clamping Selection

Transient V-I characteristics are provided in the specifications for all models of varistors. Shown below in Figure 6 are curves for $130V_{AC}$ rated models of the LA series. These curves indicate the peak terminal voltage measured with an applied 8/20μs impulse current. For example, if the peak impulse current applied to a V130LA2 is 10A, that model will limit the transient voltage to no higher than 340V.

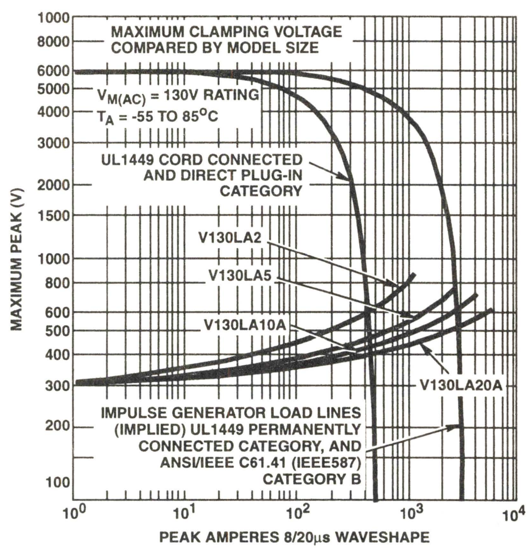


FIGURE 6. TRANSIENT V-I CHARACTERISTICS OF TYPICAL LA SERIES MODELS

If the transient current is unknown, the graphical method of Figure 3 can be utilized. From a knowledge of the transient voltage and source impedance a load line is plotted on the V-I characteristic. The intersection of the load line with the varistor model curve gives the varistor transient current and the value of clamped peak transient voltage.

The ability of the varistor to limit the transient voltage is sometimes expressed in terms of a clamp ratio. For example, consider a varistor applied to protect the power terminals of electrical equipment. If high line conditions will allow a rise to $130V_{AC}$, then 184V peak would be applied. The device selected would require a voltage rating of $130V_{ACRMS}$ or higher. Assume selection of a V130LA2 model varistor. The V130LA2 will limit transient voltages to 340V at currents of 10A. The clamp ratio is calculated to be,

$$\text{Clamp Ratio} = \frac{V_C \text{ at } 10A}{\text{Peak Voltage Applied}}$$

$$= \frac{340V}{184V} = 1.85$$

The clamp ratio can be found for other currents, of course, by reference to the V-I characteristic. In general, clamping ability will be better as the varistor physical size and energy level increases. This is illustrated in Figure 7 which compares the clamping performance of the different Harris Varistor families. It can be seen that the lowest clamping voltages are obtained from the 20mm (LA series) and 60mm (BA series) products. In addition, many varistor models are available with two clamping selections, designated by an A, B, or C at the end of the model number. The A selection is the standard model, with B and C selections providing progressively tighter clamping voltage. For example, the V130LA20A voltage clamping limit is 340V at 100A, while the V130LA20B clamps at not more than 325V.

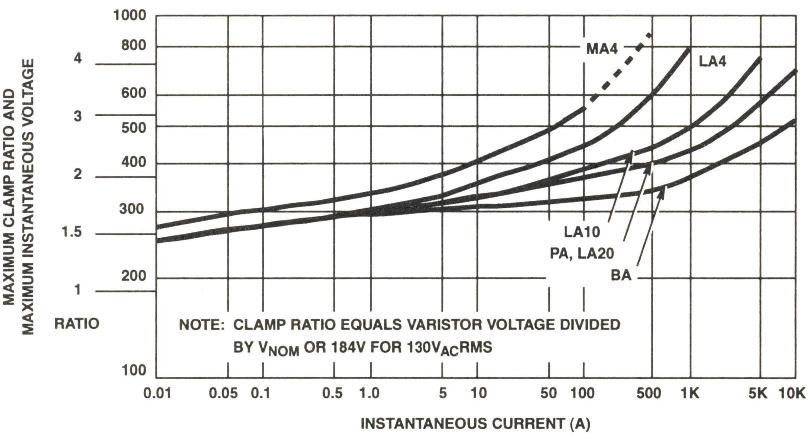
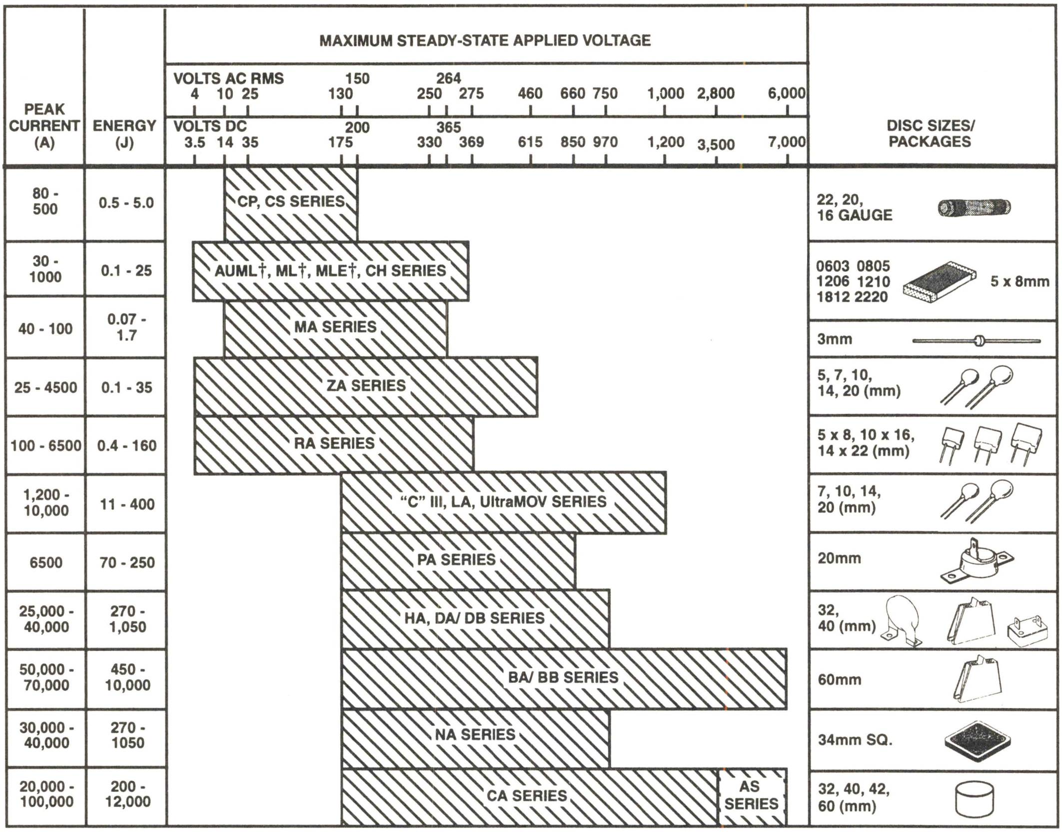


FIGURE 7. VARISTOR V-I CHARACTERISTICS FOR FOUR PRODUCT FAMILIES RATED AT $130V_{AC}$



†Harris multilayer suppression technology.

FIGURE 8. VARISTOR PACKAGE STYLES AND RATINGS RANGE

The five major considerations for varistor selection have been described. The final choice of a model is a balance of these factors with device packaging and cost trade-offs. In some applicaitons a priority requirement such as clamp voltage or energy capability may be so important as to force the selection to a particular model. Figure 8 illustrates the Harris varistor package styles in a matrix that compares energy and current ratings to the working voltage range.

Harris Semiconductor

APP NOTE

No. AN9772 January 1998

Harris Suppression Products

Harris Varistor Design Examples

This note is meant to be a guide for the user in selecting a varistor by describing common application examples, and illustrating the solution process to determine the appropriate varistor. Also described are varistor fusing and series/parallel connection rules.

Applications

Power Supply Protection Against Line Transient Damage

PROBLEM

It is desired to prevent failure of the power supply shown in Figure 1B to be used on residential $117V_{AC}$ lines. A representative transient generator is to be used for testing, as shown in Figure 1A.

If the transient is applied to the existing circuit, the rectifier will receive high negative voltages, transmitted through the filter capacitor. The LC network is there to prevent RFI from being transmitted into the power line (as in a TV set), but also serves to reduce the transient voltage. An analysis shows that the transient will be reduced approximately by half, resulting in about 2.5kV instead of 5kV at the rectifier.

This is still too high for any practical rectifier, so some suppression must be added. It is desirable to use the built-in impedance of the coil to drop the remaining voltage, so the suppressor would best be applied as shown. A selection process for a Harris Varistor is as follows:

SOLUTION

Steady-State Voltage

The $117V_{AC}$, 110% high line condition is 129V. The closest voltage rating available is 130V.

Energy and Current

The 100μH inductor will appear to be about 30Ω to the transient. The 30Ω is derived from the inductive reactance at the transient generator source frequency of $10^5\pi$ rad. Taking a first estimate of peak varistor current, 2500V/80Ω = 31A. (This first estimate is high, since it assumes varistor clamping voltage is zero.) With a tentative selection of a 130V Harris Varistor, we find that a current of 31A yields a voltage of from 325V to 380V, depending on the model size, as shown in Figure 2A and Figure 2B.

Revising the estimate, I ≈ (2500V - 325V)/80Ω = 27.2A. For model V130LA20A, 27.2A coincides closely with a 320V clamping level. There is no need to further refine the estimate of peak current if model 20A remains the final selection.

To arrive at an energy figure, assume a sawtooth current waveform of 27A peak, dropping to zero in two time constants, or 20μs.

Energy is then roughly equal to (27A x 320V x 20μs)/2, the area under the power waveform. The result is 0.086J, well within the capability of the varistor (70J). Peak current is also within the 6500A rating.

Model Selection

The actual varistor selection is a trade-off between the clamping voltage desired and the number of transient current pulses expected in the life of the equipment. A 70J rated varistor will clamp at 315V and be capable of handling over 10^6 such pulses. An 11J unit will clamp to approximately 385V and be capable of handling over 10^5 such pulses. Furthermore, the clamping voltage determines the cost of the rectifier by determining the voltage rating required. A smaller, lower cost varistor may result in a more expensive higher voltage rectifier diode.

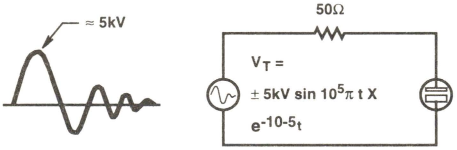


FIGURE 1A. TRANSIENT GENERATOR

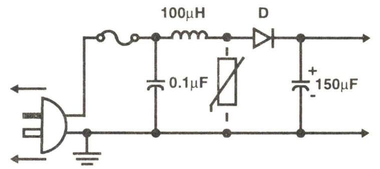


FIGURE 1B. TYPICAL POWER SUPPLY CIRCUIT

FIGURE 1. POWER SUPPLY PROTECTION

11 APPLICATION NOTES

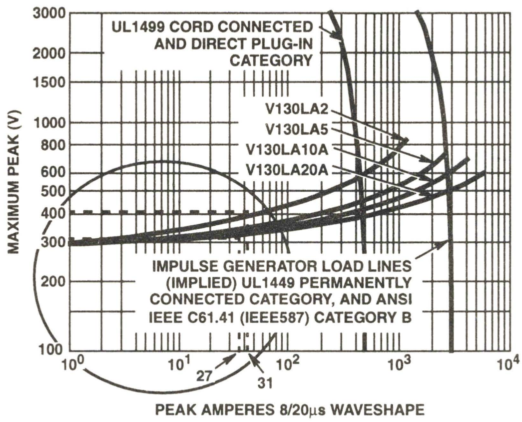


FIGURE 2A.

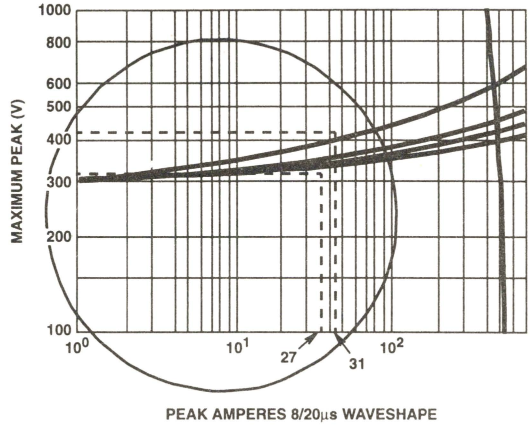


FIGURE 2B.

FIGURE 2. V130LA VARISTOR V-I CHARACTERISTICS

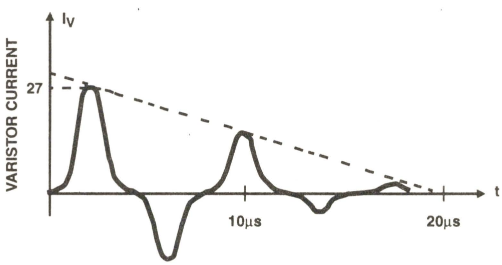


FIGURE 3A.

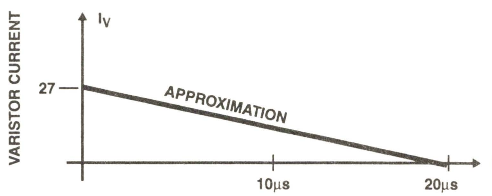


FIGURE 3B.

FIGURE 3. ENERGY APPROXIMATION

SCR Motor Control

PROBLEM

The circuit shown in Figure 4 experiences failures of the rectifiers and SCR when the transformer primary is switched off. The manufacturer has tried 600V components with little improvement.

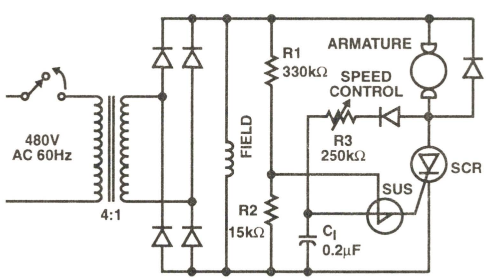


FIGURE 4. SCR MOTOR CONTROL

SOLUTION

Add a varistor to the transformer secondary to clamp the transformer inductive transient voltage spike. Select the lowest voltage Harris Varistor that is equal to or greater than the maximum high line secondary AC voltage. The V130LA types fulfills this requirement.

Determine the peak suppressed transient voltage produced by the transient energy source. This is based on the peak transient current to the suppressor, assuming the worst-case condition of zero load current. Zero load current is normally a valid assumption. Since the dynamic transient impedance of the Harris Varistor is generally quite low, the parallel higher impedance load path can be neglected.

Since transient current is the result of stored energy in the core of the transformer, the transformer equivalent circuit shown in Figure 5 will be helpful for analysis. The stored inductive energy is:

$$E_{L_M} = \frac{1}{2} L_M \hat{i}^2_M$$

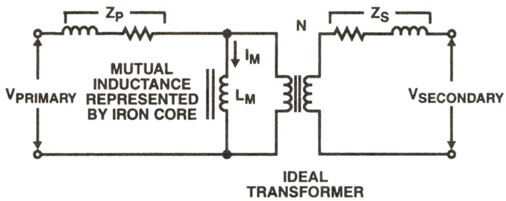


FIGURE 5. SIMPLIFIED EQUIVALENT CIRCUIT OF A TRANSFORMER

The designer needs to know the total energy stored and the peak current transformed in the secondary circuit due to the mutual inductance, L_M. At no load, the magnetizing current, (I_{NL}), is essentially reactive and is equal to I_M. This assumes that the primary copper resistance, leakage reactance and equivalent core resistive loss components are small compared to L_M. This is a valid assumption for all but the smallest control transformers. Since I_{NL} is assumed purely reactive, then:

$$X_{L_M} = \frac{V_{pri}}{I_{NL}}$$

and

$$i_M = I_{NL}$$

I_{NL} can be determined from nameplate data. Where nameplate is not available, Figure 6 and Figure 7 can guide the designer.

Assuming a 3.5% value of magnetizing current from Figure 7 for a 20kVA transformer with $480V_{AC}$ primary, and $120V_{AC}$ secondary:

$$i_M = (0.035)\frac{20\text{kVA}}{480\text{V}}$$

$$= 1.46\text{A}$$

$$\hat{i}_M = \sqrt{2}i_M$$

$$X_{L_M} = 480\text{V}/1.46\text{A}$$

With this information one can select the needed semiconductor voltage ratings and required varistor energy rating.

Peak varistor current is equal to transformed secondary magnetizing current, i.e., $\hat{i}_M(N)$, or 8.24A. From Figure 2, the peak suppressed transient voltage is 310V with the V130LA10A selection, 295V with the V130LA20B. This allows the use of 300V rated semiconductors. Safety margins exist in the above approach as a result of the following assumptions:

1. All of the energy available in the mutual inductance is transferred to the varistor. Because of core hysteresis and secondary winding capacitance, only a fraction less than two-thirds is available.
2. The exciting current is not purely reactive. There is a 10% to 20% safety margin in the peak current assumption.

After determining voltage and peak current, energy and power dissipation requirements must be checked. For the given example, the single pulse energy is well below the V130LA20B varistor rating of 70J at 85°C maximum ambient temperature. Average power dissipation requirements over idling power are not needed because of the non-repetitive nature of the expected transient. Should the transient be repetitive, then the average power is calculated from the product of the repetition rate times the energy of the transient. If this value exceeds the V130LA20B capability of 1.0W, power varistors of the HA, DA, or DB Series may be required.

Should the ambient temperature exceed 85°C or the surface temperature exceed 85°C, the single pulse energy ratings and the average power ratings must be derated by the appropriate derating factors supplied on the data sheet

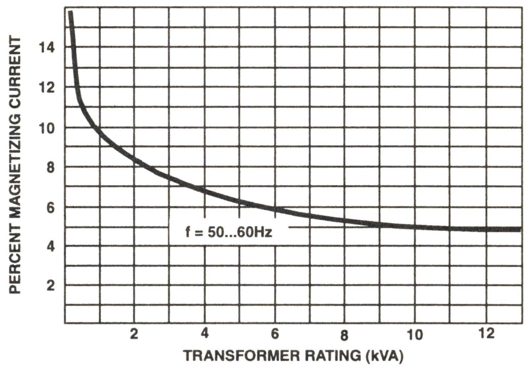


FIGURE 6. MAGNETIZING CURRENT OF TRANSFORMERS WITH LOW SILICON STEEL CORE

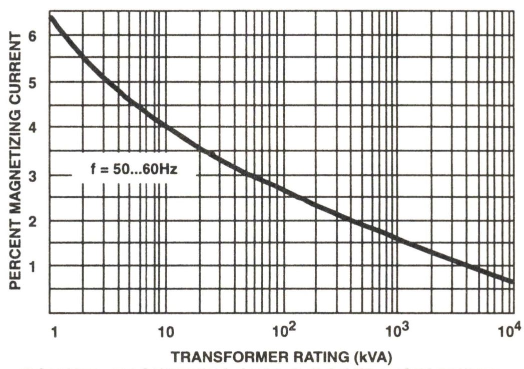


FIGURE 7. MAGNETIZING CURRENT OF TRANSFORMERS WITH HIGH SILICON STEEL CORE OR SQUARE LOOP CORE

Contact Arcing Due to Inductive Load

PROBLEM

To extend the life of the relay contacts shown in Figure 8 and reduce radiated noise, it is desired to eliminate the contact arcing.

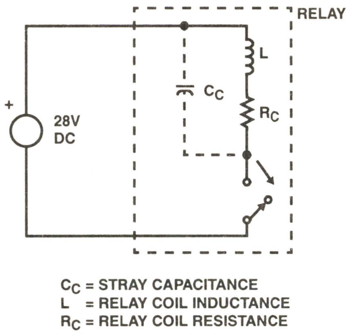


FIGURE 8. RELAY CIRCUIT

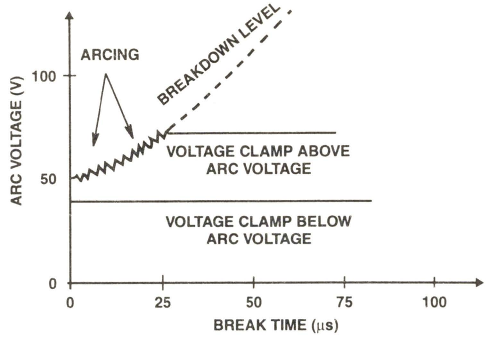


FIGURE 9. VOLTAGE CLAMP USED AS ARC SUPPRESSOR

When relays or mechanical switches are used to control inductive loads, it is necessary to use the contacts at only about 50% of their resistive load current rating to reduce the wear caused by arcing of the contacts. The energy in the arcing is proportional to the inductance and to the square of the current.

Each time the current in the inductive load is interrupted by the mechanical contacts, the voltage across the contacts builds up as -L di/dt. When the contacts arc, the voltage across the arc decreases and the current in the coil can increase somewhat. The extinguishing of the arc causes an additional voltage transient which can again cause the contacts to arc. It is not unusual for the restriking to occur several times with the total energy in the arc several times that which was originally stored in the inductive load. It is this repetitive arcing that is so destructive to the contacts.

In the example, R_C is 30Ω and the relay contacts are conducting nearly 1A. The contacts will draw an arc upon opening with more than approximately 0.4A or 12V. The arc continues until current falls below 0.4A.

SOLUTION

To prevent initiation of the arc, it is necessary to reduce the current and voltage of the contacts below the arc threshold levels at the time of opening, and then keep them below breakdown threshold of the contacts as they open. Two obvious techniques come to mind to accomplish this: 1) use of a large capacitor across the contacts, and 2) a voltage clamp (such as a varistor). The clamp technique can be effective only when the minimum arc voltage exceeds the supply voltage.

In this example a clamping device operating above the supply voltage will not prevent arcing. This is shown in Figure 9.

The capacitor technique requires the capacitance to be sufficiently large to conduct the inductor current with a voltage rate-of-rise tracking the breakdown voltage rate-of-rise of the contacts as they mechanically move apart. This is shown in Figure 10A.

The limitations in using the capacitor approach are size and cost. This is particularly true for those cases involving large amounts of inductive stored energy. Furthermore, the use of a large capacitor alone creates large discharge currents upon contact reclosure during contact bouncing. As a result, the contact material may melt at the point of contact with subsequent welding. To avoid this inrush current, it is customary to add a series resistor to limit the capacitive discharge current. However, this additional component reduces the network effectiveness and adds additional cost to the solution.

A third technique, while not as obvious as the previous two, is to use a combination approach. This technique shown in Figure 10B parallels a voltage clamp component with an R-C network. This allows the R-C network to prevent the low voltage initial arcing and the clamp to prevent the arcing that would occur later in time as the capacitor voltage builds up. This approach is often more cost effective and reliable then using a large capacitor.

Also, with AC power relays the impedance of a single large R-C suppressor might be so low that it would allow too much current to flow when the contacts are open. The combination technique of a small R-C network in conjunction with a varistor is of advantage here, too.

In this example a 0.22μF capacitor and 10Ω resistor will suppress arcing completely, but by reducing the capacitance to 0.047μF, arcing will start at 70V.

Thus, to use a varistor as a clamp in conjunction with the R-C network, it must suppress the voltage to below 70V at 1A and be capable of operating at a steady-state maximum DC voltage of 28V + 10%, or 30.8V (assumes a ±10% regulated 28V DC supply).

The three candidates that come closest to meeting the above requirement are the MA series V39MA2B model and the ZA series V39ZA1 and V39ZA05 models, all of which have maximum steady-state DC voltage ratings of 31V. The V39MA2B and V39ZA05 V-I characteristics at 1A shows a maximum voltage of 73V, while the V39ZA1 characteristic at 1A shows a maximum voltage of 67V. Thus, the latter varistor is selected. Use of a 0.068μF capacitor in place of the 0.047μF previously chosen would allow use of the V39MA2B or V39ZA05.

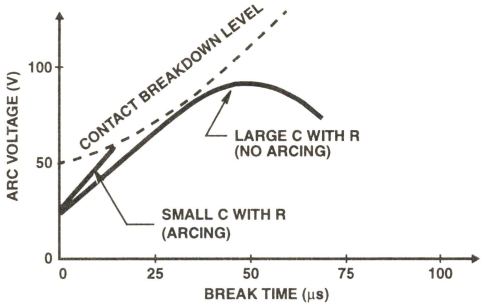


FIGURE 10A. R-C ARC SUPPRESSION

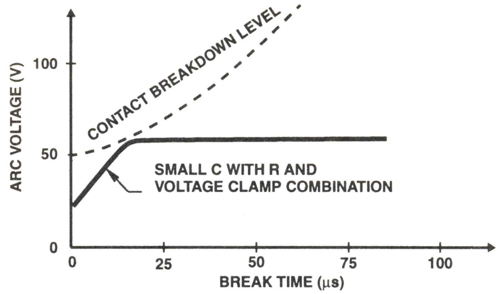


FIGURE 10B. R-C AND CLAMP ARC SUPPRESSION

FIGURE 10. RELAY ARC VOLTAGE SUPPRESSION TECHNIQUES

Placing only a Harris Varistor rated for $31V_{DC}$ across the contacts results in arcing up to the 66V level. By combining the two, the capacitor size and voltage rating are reduced and suppression complete.

Besides checking the varistor voltage and arcing elimination, the designer should review energy and peak current requirements. Varistor energy is determined from a measurement of the coil inductance and the calculation $E = 1/2\ Li^2$. Peak current, of course, is under 1A. Power dissipation is negligible unless the coil is switched often (several times per minute).

In those cases where multiple arcs occur, the varistor energy will be a multiple of the above $1/2\ Li^2$ value. The peak current is well within the rating of either the MA or ZA series of varistors, but the number of contact operations allowable for either varistor is a function of the impulse duration. This can be estimated by assuming a L/R_C time constant at the 1A or peak current value. Since the voltage across the varistor is 67V at 1A, the varistor static resistance is 67Ω. The coil R_C value is 28V/1A, or 28Ω. The coil inductance was found to be 20mH. Thus, the approximate time constant is:

$$\tau = L/R_C = \frac{20\text{mH}}{95} = 210\mu s$$

From the pulse rating curves of the V39ZA1 model, the number of allowable pulses exceeds 100 million.

Noise Suppression

PROBLEM

Switching of a small timer motor at 120V, 60Hz, was causing serious malfunctions of an electronic device operating from the same power line. Attempts were made to observe the transient noise on the line with an oscilloscope as the first step in curing the problem. Observed waveforms were "hash," i.e., not readily identifiable.

Noise in an electromechanical system is a commonly experienced result of interrupting current by mechanical contacts. When the switch contacts open, a hot cathode arc may occur if the current is high enough. On the other hand, low current will permit switch opening without an arc, but with ringing of circuit resonances. As a consequence, voltages can exceed the contact gap breakdown resulting in a replica of the old spark gap transmitter. It is the low current case that produces the most serious noise disturbances which can result in malfunctions or damage to electrical equipment. These pulses cause noise problems on adjacent lines, trigger SCR's and triacs, and damage semiconductors. In addition, they can disrupt microprocessor operation causing memory to be lost and vital instructions to be missed.

SOLUTION

A test circuit (Figure 11) was set up with lumped elements replacing the measured circuit values. The motor impedance was simulated by R_1, L_1, and C_1, and the AC line impedance by L_2 and C_2. A DC source allowed repeatable observations over the full range of current that could flow through the switch in the normal AC operation. A diode detector was used to observe the RF voltage developed across a 2" length of wire (50nH of inductance).

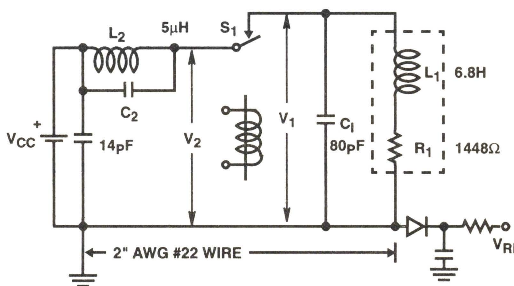
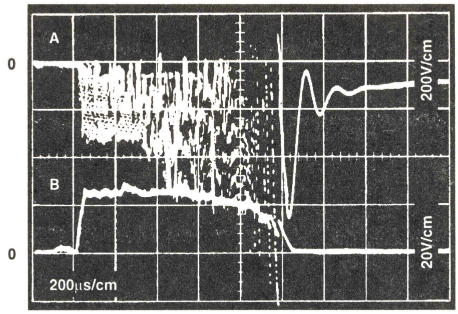


FIGURE 11. TEST CIRCUIT

The supply is set at 25mA to represent the peak motor current in normal $120V_{AC}$ operation. As switch S_1 was opened, the waveform in Figure 12 was recorded. Note the "showering arc" effect. The highest breakdown voltage recorded here is 1020V, and the highest RF detector output (shown in the lower trace) is 32V.

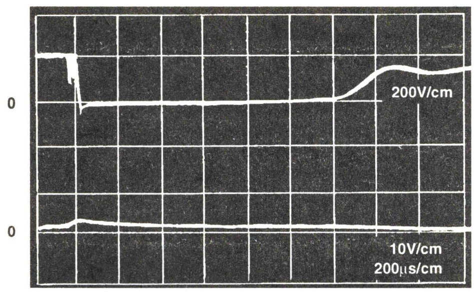


UPPER V_1: 200V/cm LOWER V_{RF}: 20V/cm

t: 0.2ms/cm

FIGURE 12. UNPROTECTED CONTACTS

Obviously, some corrective action should be taken and the most effective one is that which prevents the repeated breakdown of the gap. Figure 13 shows the waveform of V_1 (upper trace) and V_{RF} (lower trace) for the same test conditions with a Harris Varistor, type V130LA10A, connected directly across the switch terminals. The varistor completely eliminates the relaxation oscillations by holding the voltage below the gap breakdown voltage (about 300V) while dissipating the stored energy in the system.



UPPER V_1: 200V/cm LOWER V_{RF}: 20V/cm

t: 0.2ms/cm

FIGURE 13. VARISTOR PROTECTED CONTACTS

Protection of Transistors Switching Inductive Loads

PROBLEM

The transistor in Figure 14 is to operate a solenoid. It may operate as frequently as once per second. The circuit (without any suppression) consistently damages the transistor.

The inductor drives the collector voltage up when the transistor base is grounded (turning "off"). The inductor forces current to flow until the energy stored in its field is dissipated. This energy is dissipated in the reverse bias condition of the transistor and is sufficient to cause breakdown (indicated by a sudden collapse of collector voltage during the pulse).

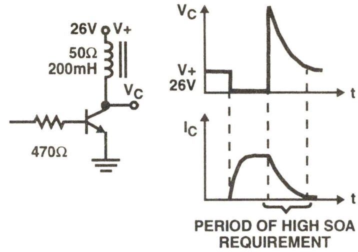


FIGURE 14A. BASIC SOLENOID CIRCUIT

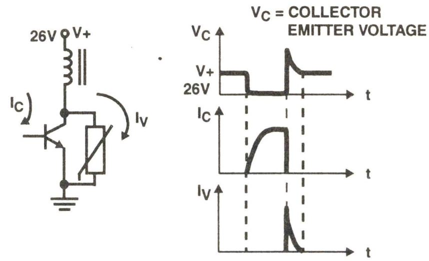


FIGURE 14B. SOLENOID CIRCUIT WITH VARISTOR PROTECTION

FIGURE 14. TRANSISTOR SWITCHING OF AN INDUCTIVE LOAD

SOLUTION

This condition can be eliminated either by shunting the transistor with a suppressor or by turning it on with a varistor connected collector-to-base. The first method will considerably reduce the demands upon the safe operating area (SOA) of the transistor. If the voltage is kept below its breakdown level, all energy will be dissipated in the suppressor. The latter method will cause the transistor to once again dissipate the stored energy, but in the forward-bias state in which the transistor can safely dissipate limited amounts of energy. The choice is determined by economics and reliability. A suppressor connected collector-emitter (C-E) will be more expensive than one connected C-B, since it is required to absorb more energy, but will allow the use of a transistor with reduced SOA.

If a collector-emitter varistor is used in the above example, it is required to withstand $28.6V_{DC}$ worst-case (26 + 10% regulation). The stored energy is 1/2 Li^2 or 1/2 (0.20) $(0.572)^2$ = 0.0327J. The energy contributed by the power supply is roughly equal to this (coil voltage ≈ supply voltage, since varistor clipping voltage ≈ 2 x supply voltage). Ignoring coil resistance losses for a conservative estimate, varistor energy dissipation is 0.065J per pulse. The peak current will be 0.572A, the same as the coil current when the transistor is switched off.

If the transistor operates once per second, the average power dissipation in the varistor will be 0.065W. This is less than the 0.20W rating of a small $31V_{DC}$ varistor (V39ZA1). From the data sheet it can be seen that if the device temperature exceeds 85^oC, derating is required.

The nonrecurrent joule rating is 1.5J, well in excess of the recurrent value. To determine the repetitive joule capability, the current pulse rating curves for the ZA series must be consulted. Two are shown in Figure 15.

To use Figure 27, the impulse duration (to the 50% point) is estimated from the circuit time constants and is found to be 1240µs. From Figure 27A, for this example, the 7mm V39ZA1 would not be limited to a cumulative number of pulses.

In cases where the peak current is greater and intersects with the recommended pulse life curves, the designer must determine the maximum number of operations expected over the life of the circuit and confirm that the pulse life curves are not exceeded. Figure 15B shows the curves for the larger, 14mm V39ZA6 device and, illustrates the resultant higher capability in terms of number of transients for a given peak pulse current and duration.

Also, it may be necessary to extrapolate the pulse rating curves. This has been done in Figure 16 where the data from Figure 15B is transposed. At low currents the extrapolation is a straight line.

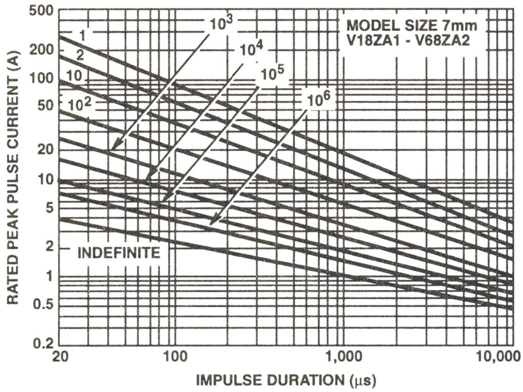


FIGURE 15A. ZA SERIES V18ZA1 TO V68ZA2 (MODEL SIZE 7mm)

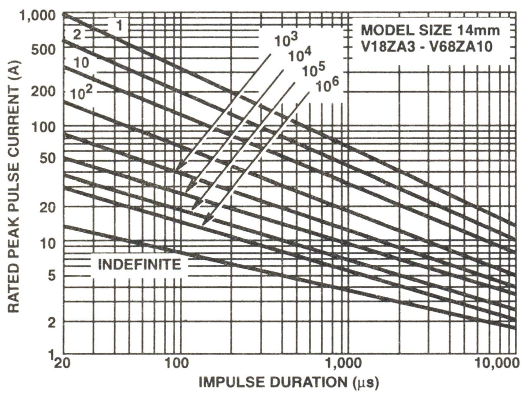


FIGURE 15B. ZA SERIES V18ZA3 TO V68ZA10 (MODEL SIZE 14mm)

Finally, the V-I characteristics curves must be consulted to determine the varistor maximum clamping voltage in order to select the minimum transistor breakdown voltage. In this example, at 0.572A the V39ZA6 (if chosen) provides a maximum of 61V requiring that the transistor have about a 65V or 70V capability.

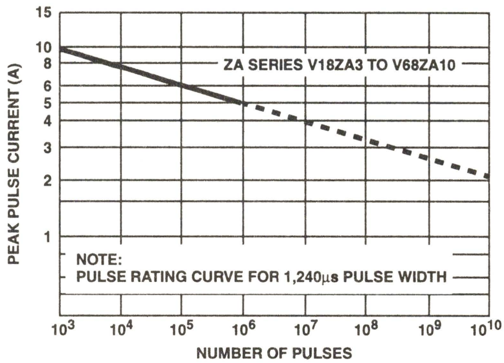
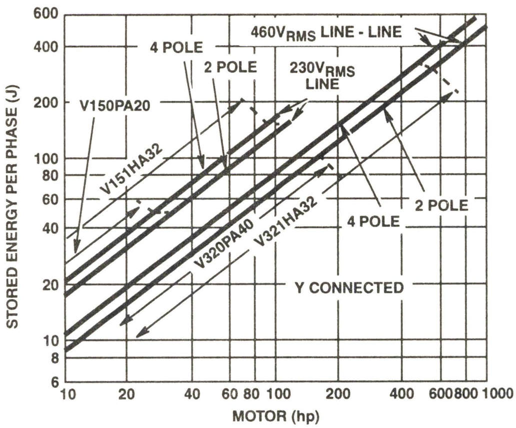


FIGURE 16. EXTRAPOLATED PULSE RATING CURVES

Motor Protection

Frequently, the cause of motor failures can be traced to insulation breakdown of the motor windings. The source of the transients causing the breakdown may be from either internal magnetic stored energy or from external sources. This section deals with the self-generated motor transients due to motor starting and circuit breaker operation. Externally generated transients and their control are covered in AN9768.

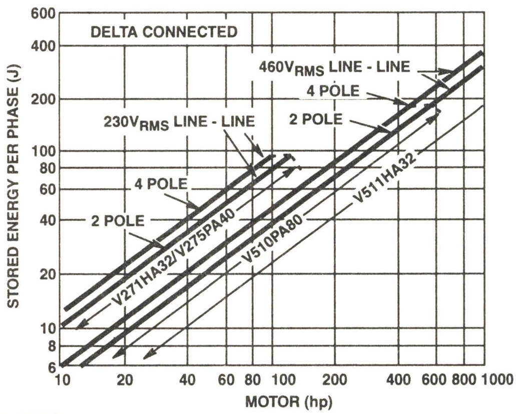
In the case of DC motors the equivalent circuit consists of a single branch. The magnetic stored energy can be easily calculated in the armature or field circuits using the nameplate motor constants. With AC induction motors the equivalent magnetic motor circuit is more complex and the circuit constants are not always given on the motor nameplate. To provide a guide for motor protection, Figures 17, 18, 19 were drawn from typical induction motor data. While the actual stored energy will vary according to motor frame size and construction techniques, these curves provide guidance when specific motor data is lacking. The data is conservative as it assumes maximum motor torque, a condition that is not the typical running condition. Stored energy decreases considerably as the motor loading is reduced. Experience with the suppression of magnetic energy stored in transformers indicates that Harris Varistors may be used at their maximum energy ratings, even when multiple operations are required. This is because of the conservatism in the application requirements, as indicated above, and in the varistor ratings. Thus, no attempt is made to derate the varistor for multiple operation because of the random nature of the transient energy experienced.



NOTES:

1. Y connected 60Hz.
2. Energy at max torque slip speed.
3. See Figure 20 for varistor circuit placement.

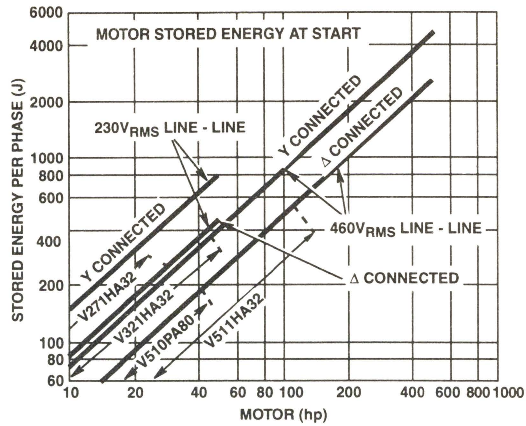
FIGURE 17. STORED ENERGY CURVES FOR TYPICAL WYE-CONNECTED INDUCTION MOTOR



NOTES:

4. Delta connected at 60Hz.
5. Energy at maximum torque slip speed.
6. See Figure 20 for varistor circuit placement.

FIGURE 18. STORED ENERGY CURVES FOR TYPICAL DELTA-CONNECTION INDUCTION MOTOR



NOTES:

7. 60Hz, see Figure 20 for varistor circuit placement.
8. Energy at start, i.e., SLIP = 1.
9. Induction motor.
10. 2, and 4 pole motors.

FIGURE 19. STORED ENERGY CURVES FOR A TYPICAL MOTOR WITH STALLED ROTOR

As an aid in selecting the proper operating voltage for Harris Varistors, Table 1 gives guidelines for wye-connected and delta-connected motor circuits at different line-to-line applied voltages. Figure 20 provides guidance in proper placement of the varistor.

Interruption of motor starting currents presents special problems to the user as shown in Figure 19. Since the stored magnetic energy values are approximately 10 times the running values, protection is difficult at the higher horsepower levels. Often the motor is started by use of a reduced voltage which will substantially reduce the stored energy. A reduction in starting current of a factor of two results in a fourfold reduction in stored energy. If a reduced voltage starter is not used, then a decision must be made between protection for the run condition only, and the condition of locked rotor motor current. For most applications, the starting condition can be ignored in favor of selecting the varistor for the worst-case run condition.

TABLE 1. PREFERRED VARISTOR VOLTAGE RATINGS FOR DELTA- AND WYE-CONNECTED MOTORS

RMS Line Voltage (Line-Line)	⟹	230	380	460	550	600
Delta Connected	Applied V. Varistor Ratings	230 250/275	380 420/480	460 510/575	550 575/660	600 660
Y Connected	Applied V. Varistor Ratings	133 150	220 250/275	266 320	318 420	346 420

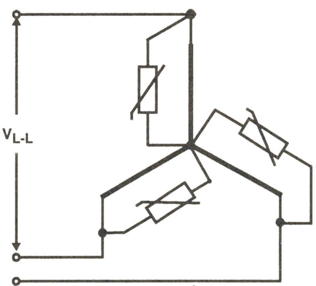
PROBLEM

To protect a two-pole, 75hp, 3ϕ, 460V_{RMS} line-to-line wye-connected motor from interruption of running transients.

Specific Motor Data Is Not Available

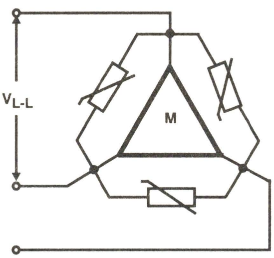
SOLUTION

Consult Figure 17 along with Table 1. Standard varistors having the required voltage ratings are the 320V_{RMS} rated models. This allows a 20% high-line voltage condition on the nominal 460V line-to-line voltage, or 266V line-neutral voltage. Figure 17 shows a two-pole 75hp, wye-connected induction motor, at the running condition, has 52J of stored magnetic energy per phase. Either a V320PA40 series or a V321HA32 series varistor will meet this requirement. The HA series Harris Varistor provides a greater margin of safety, although the PA series Harris Varistor fully meets the application requirements. Three varistors are required, connected directly across the motor terminals as shown in Figure 20.



$$V_{VARISTOR} = \frac{1}{\sqrt{3}} V_{L-L}$$

FIGURE 20A. WYE CONNECTED



$$V_{VARISTOR} = V_{L-L}$$

FIGURE 20B. DELTA CONNECTED

FIGURE 20. VARISTOR - 3ϕ INDUCTION MOTOR CIRCUIT PLACEMENT

Power Supply Crowbar

Occasionally it is possible for a power supply to generate excessively high voltage. An accidental removal of load can cause damage to the rest of the circuit. A simple safeguard is to crowbar or short circuit the supply with an SCR. To provide the triggering to the SCR, a high-voltage detector is needed. High voltage avalanche diodes are effective but expensive. An axial leaded Harris Varistor provides an effective, inexpensive substitute.

PROBLEM

In the circuit of Figure 21, the voltage, without protection, can exceed twice the normal 240V peaks, damaging components downstream. A simple arrangement to crowbar the supply is shown.

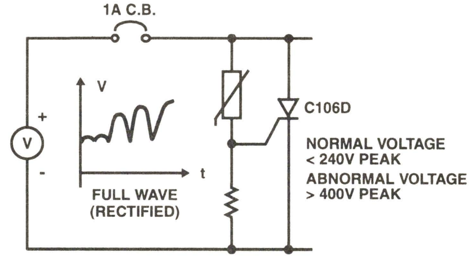


FIGURE 21. CROWBAR CIRCUIT

The supply shown can provide 2A_{RMS} of short-circuit current and has a 1A circuit breaker. A C106D SCR having a 4A_{RMS} capability is chosen. Triggering will require at least 0.4V gate-to-cathode, and no more than 0.8V at 200μA at 25^{o}C ambient.

SOLUTION

Check the MA series Harris Varistor specifications for a device capable of supporting 240V peak. The V270MA4B can handle $\sqrt{2}$ (171V_{RMS}) = 242V. According to its specification of 270V $\pm$10%, the V270MA4B will conduct 1mA_{DC} at no less than 243V. The gate-cathode resistor can be chosen to provide 0.4V (the minimum trigger voltage) at 1mA, and the SCR will not trigger below 243V. Therefore, R_{GK} should be less than 400Ω. The highest value 5% tolerance resistor falling below 400Ω is a 360Ω resistor, which is selected. Thus, R_{GK} is 378Ω maximum and 342Ω minimum. Minimum SCR trigger voltage of 0.4V requires a varistor of 0.4V/378Ω, or 1.06mA for a minimum varistor voltage of $\approx$245V. The maximum voltage to trigger the circuit is dependent upon the maximum current the varistor is required to pass to trigger the SCR. For the C106 at 25^{o}C, this is determined by calculating the maximum current required to provide 0.8V across a parallel resistor comprised of the 360Ω R_{GK} selected and the equivalent gate-cathode SCR resistor of 0.8V/200μA, since the C106 requires a maximum of 200μA trigger current. The SCR gate input resistance is 4kΩ and the minimum equivalent gate-cathode resistance is the parallel combination of 4kΩ and $R_{GK(MIN)}$, or 360Ω -5%, 342Ω. The parallel combination is 315Ω. Thus, $I_{VARISTOR}$ for maximum voltage-to-trigger the C106 is 0.8V/315Ω, or 2.54mA. According to the specification sheet for the V270MA4B, the varistor will not exceed 330V with this current. The circuit will, therefore, trigger at between 245 and 330V peak, and a 400V rated C106 can be used. The reader is cautioned that SCR gate

characteristics are sensitive to junction temperatures, and a value of 25°C for the SCR temperature was merely chosen as a convenient value for demonstrating design procedures.

The maximum energy per pulse with this waveform is determined as approximately 1/2 x K x I_{PK} x V_{PK} x τ (duration of 1/2 wave pulse), or 0.52mJ for this example. Since the voltage does not drop to zero in this case, the SCR remains on, and the varistor sees only one pulse; thus, no steady-state power consideration exists.

General Protection of Solid State Circuitry, Against Transients On 117V_{AC} Lines

PROBLEM

Modern electronic equipment and home appliances contain solid state circuitry that is susceptible to malfunction or damage caused by transient voltage spikes. The equipment is used in residential, commercial, and industrial buildings. Some test standards have been adopted by various agencies (see application notes AN9769 and AN9773) and further definition of the environment is underway by the IEEE and other organizations.

The transients which may occur on residential and commercial AC lines are of many waveshapes and of varying severity in terms of peak voltage, current, or energy. For suppressor application purposes, these may be reduced to three categories.

First, the most frequent transient might be the one represented by a 30kHz or 100kHz ring wave. This test surge is defined by an oscillatory exponentially decaying voltage wave with a peak open circuit voltage of 6kV. This wave is considered representative of transients observed and reported by studies in Europe and North America. These transients can be caused by distant lightning strikes or distribution line switching. Due to the relatively high impedance and short duration of these transients, peak current and surge energy are lower than the second and third categories.

The second category is that of surges produced by nearby lightning strokes. The severity of a lightning stroke is characterized in terms of its peak current. The probability of a direct stroke of a given severity can be determined. However, since the lightning current divides in many paths, the peak current available at an AC outlet within a building is much less than the total current of the stroke. The standard impulse used to represent lightning and to test surge protective devices is an 8/20µs current waveshape as defined by ANSI Standard C68.2, and also described in ANSI/IEEE Standard C62.41-1991 and IEC 664-1 (1992).

A third category of surges are those produced by the discharge of energy stored in inductive elements such as motors and transformers. A test current of 10/1000µs waveshape is an accepted industry test impulse and can be considered representative of these surges.

Although no hard-and-fast rules can be drawn as to the category and severity of surges which will occur, a helpful guideline can be given to suggest varistors suitable in typical applications.

The guideline of Table 2 recognizes considerations such as equipment cost, equipment duty cycle, effect equipment downtime, and balances the economics of equipment damage risk against surge protection cost.

Failure Modes and Varistor Protection

Varistors are inherently rugged and are conservatively rated and exhibit a low failure rate. The designer may wish to plan for potential failure modes and the resultant effects should the varistor be subjected to surge currents or energy levels above its rating.

Failure Modes

Varistors initially fail in a short-circuit mode when subjected to surges beyond their peak current/energy ratings. They also short-circuit when operated at steady-state voltages well beyond their voltage ratings. This latter mode of stress may result in the eventual open-circuiting of the device due to melting of the lead solder joint.

TABLE 2. HARRIS VARISTOR SELECTION GUIDELINE FOR 117V_{AC} APPLICATIONS

APPLICATION TYPE	DUTY CYCLE	LOCATION	EXAMPLE	SUGGESTED MODEL
Light Consumer	Very Low	A	Mixer/Blender	V07E130 or V10E130
Consumer	Low	A	Portable TV/Electronics	V14E130
Consumer	Medium	A	Home Theater, PC	V14E130, V20E130
Light Industrial/Office	Medium	B	Copier, Server	V20E130, V20E140
Industrial	Medium	B	Motors, Solenoid, Relay	V20E140, V131HA32
Industrial	High	B	Large Computer Motor Control	V131DA40 or DB40
Industrial	High	B	Elevator Control Heavy Motors	V151DA40 or DB40

When the device fails in the shorted mode the current through the varistor becomes limited mainly by the source impedance. Consequently, a large amount of energy can be introduced, causing mechanical rupture of the package accompanied by expulsion of package material in both solid and gaseous forms. Steps may be taken to minimize this potential hazard by the following techniques: 1) fusing the varistor to limit high fault currents, and, 2) protecting the surrounding circuitry by physical shielding, or by locating the varistor away from other components.

Fusing the Varistor

Varistor fusing should be coordinated to select a fuse that limits current below the level where varistor package damage could occur. The location of the fuse may be in the distribution line to the circuit or it may be in series with the varistor as shown in Figure 22. Generally, fuse rather than breaker protection is preferred. Breaker tripping may be too slow to prevent excessive fault energy in some applications.

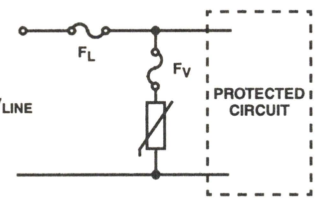


FIGURE 22. FUSE PLACEMENT FOR VARISTOR PROTECTION

In high power industrial circuits the line currents are generally so high as to rule out the use of a line fuse for varistor protection. The fuse may not clear under a varistor fault condition and would allow varistor failure. In low power (5-20A) applications it may be feasible to use the line fuse, F_L, only.

Use of a line fuse, F_L, rather than F_V, does not present the problem of having the fuse arc voltage being applied across the circuit. Conversely, with F_V alone, the fuse arc voltage adds to the varistor voltage, increasing the V_C, the transient clamp voltage. Since some fuses can have peak arc voltages in excess of twice peak working voltage, fuse clearing can have a significant effect on protection levels.

Another factor in the choice of location is the consequence of system interruption. Fuse location F_L will cause a shutdown of the circuit while location F_V will not. While the circuit can continue to operate when F_V clears, protection no longer is present. For this reason it is desirable to be able to monitor the condition of F_V.

Fusing Example (Light Industrial Application)

A process control minicomputer is to be protected from transients on a 115V nominal line. The minicomputer draws 7.5A from the line, which is guaranteed to be regulated to ±10% of nominal line voltage. A V130LA20A varistor is chosen on the basis that the worst-case surge current would be a 10/1000µs pulse of 100A peak amplitude. The rationale for this surge requirement is that the incoming plant distribution system is protected with lightning arrestors having a maximum arrestor voltage of 5kV. Assuming a typical 50Ω characteristic line impedance, the worst-case transient current through the varistor is 100A. The 1ms impulse duration is taken as a worst-case composite wave estimate. While lightning stroke discharges are typically less than 100µs, they can recur in rapid fire order during a 1s duration. From the pulse rating curves of the LA series size 20mm models, it is seen that the V130LA20 single pulse withstand capability at 1ms impulse duration is slightly in excess of 100A.

This is adequate for application in areas where lightning activity is medium to light. For heavy lightning activity areas, either a DA or DB series varistor might be desirable to allow a capability of withstanding over 70 transients. In making the choice between the LA series and higher energy series, the designer must decide on the likelihood of a worst-case lightning stroke and resultant fuse replacement should the varistor fail.

Assuming a low lightning activity area, the V130LA20A series is a reasonable choice. To coordinate the fuse with the varistor, the single pulse surge rating curve is redrawn as I^2t vs impulse duration as shown in Figure 23. The I^2t of the composite 10/1000µs impulse is found from:[1]

$$I^2t = \frac{1}{3}\hat{I}^2(10\mu s) + 0.722\,\hat{I}^2(\tau_{(0.5)} - 10\mu s)$$

When:

$\tau_{(0.5)} \geq 200\mu s$ (time for impulse current to decay by 0.5)

$$I^2t \approx 0.722\,\hat{I}^2\tau_{(0.5)}$$

Where: the first term represents the impulse I^2t contributed by the 10µs rise portion of the waveform and the second term is the I^2t contributed by the exponential decay portion.

Figure 23 shows a cross-hatched area which represents the locus of possible failure of the varistor. This area is equal to an I^2 value of from two to four times that derived from the data sheet peak current pulse life curves. The curve extending beyond the cross-hatched area and parallel to it is where package rupture will take place.

The criteria for fuse selection is given below.

A) Fuse melts; i.e., opens, only if worst-case transient is exceeded and/or varistor fails.

B) If varistor fails, fuse clearing limits I^2t applied to varistor values below that required for package rupture.

C) Fuse is rated at $130V_{RMS}$.

D) Fuse provides current limiting for solid-state devices.

Based on the above, a Carbone-Ferraz $12A_{RMS}$, $130V_{RMS}$, Class FA fuse is tentatively selected. The minimum melting I^2t and maximum clearing I^2t curves for the 12A fuse are shown superimposed on the varistor characteristics.

This fuse is guaranteed to melt at an I^2t of 40% above the estimated worst-case transient. Upon melting, clearing I^2t and clearing time will depend upon available fault current from the $130V_{RMS}$ line. Table 3 lists clearing times for the selected fuse versus available prospective circuit current.

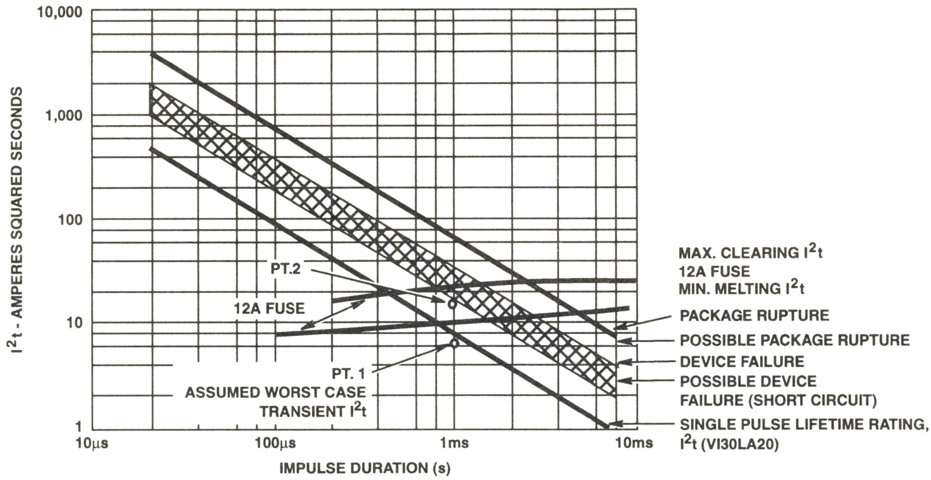


FIGURE 23. HARRIS VARISTOR - FUSE COORDINATION CHART

TABLE 3. 12A FUSE - PROSPECTIVE CURRENT vs CLEARING TIME

PROSPECTIVE CURRENT (A_{RMS})	CLEARING TIME (ms)
60	8.0
120	5.6
240	3.5
1200	1.3
3600	0.57

As Figure 23 shows, a clearing time of less than 1.5ms is desirable. For fault currents in excess of 1.2kA, the fuse will clear at less than $24A^2s$ and 1.3ms. This will prevent varistor package rupturing. However, the distribution line may be "soft," i.e., have a high source impedance at the 60Hz power frequency that limits the fault current to values below 1.2kA. Then, it is possible that the fuse would not protect the varistor package from rupturing, though it would serve to isolate the varistor in any case.

Upon further examination of this example, it is clear that the varistor will be protected from package rupturing even if the transient pulse current is 50% greater than that of the assumed value, resulting in an I^2t of $16A^2S$ (Point 2 on Figure 23).

Placement of the fuse for this example application could be in the line or in series with the varistor. If in series with the varistor, the line fuse should be a medium to slow speed, such as a "slow blow" type 15A fuse. That would assure a fault in the varistor would be isolated by the varistor fuse without interrupting the line fuse.

It is desirable to indicate the status of the varistor fuse if one is used in addition to the line fuse. The circuit shown in Figure 24 senses the presence of voltage across the varistor by use of a photocoupler. When the fuse interrupts the varistor circuit, the LED of the coupler becomes de-energized, and the coupler output signal can be used to annunciate an unprotected condition. Some fuse manufacturers provide indicating means upon fuse operation that may also be used to trip an alarm.

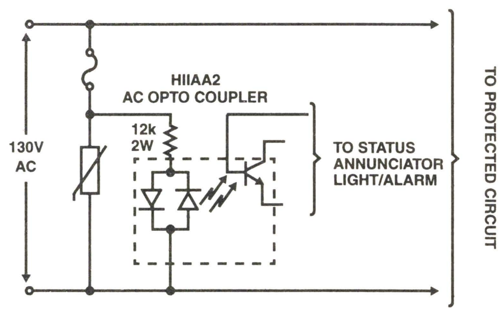


FIGURE 24. VARISTOR FUSE STATUS SENSING CIRCUIT

In selecting a fuse, the reader is advised to avoid data based on average values or data taken at operating conditions that are grossly different from the actual application. For example, DC data does not apply when the fuse will be used on an AC circuit. Also, test data taken in a resistive circuit with unity power factor does not hold for low power factor operation.

Series and Parallel Operation of Varistors

In most cases the designer can select a varistor that meets the desired voltage ratings from standard catalog models. Occasionally the standard catalog models do not fit the requirements either due to voltage ratings or energy/current ratings. When this happens, two options are available: varistors can be arranged in series or parallel to make up the desired ratings, or the factory can be asked to produce a "special" to meet the unique application requirement.

Series Operation of Varistors

Varistors are applied in series for one of two reasons: to provide voltage ratings in excess of those available, or to provide a voltage rating between the standard model voltages. As a side benefit, higher energy ratings can be achieved with series connected varistors over an equivalent single device. For instance, assume the application calls for a lead mounted varistor with an VRMS rating of 375V_{AC} and having a I_{TM} peak current capability of 6000A. The I_{TM} requirement fixes the varistor size. Examining the LA series voltage ratings near 375V_{AC}, only 320V and 420V units are available. The 320V is too low and the 420V unit (V420LA40B) results in too high a clamp voltage (V_C of 1060V at 100A). For a V130LA20B and a V250LA40B in series, the maximum rated voltage is now the sum of the voltages, or 380V. The clamping voltage, V_C, is now the sum of the individual varistor clamping voltages, or 945V at 100A. The peak current capability is still 6500A but the energy rating is now the sum of the individual energy ratings, or 200J.

In summary, varistors can be connected in series providing they have identical peak current ratings (I_{TM}), i.e., same disc diameter. The composite V-I characteristic, energy rating, and maximum clamp voltages are all determined by summing the respective characteristics and/or ratings of the individual varistors.

Parallel Operation of Varistors

Application requirements may necessitate higher peak currents and energy dissipation than the high energy series of varistors can supply individually. When this occurs, the logical alternative is to examine the possibility of paralleling varistors. Fortunately, all Harris Varistors have a property at high current levels that makes paralleling feasible. This property is the varistor's series-resistance that is prominent during the "up-turn region" of the V-I characteristic. This up-turn is due to the inherent linear resistance component of the varistor characteristic (see Application Note AN9767). It acts as a series balancing, or ballasting, impedance to force a degree of sharing that is not possible at lower current levels. This is depicted in Figure 25. At a clamp voltage of 600V, the difference in current between a maximum specified sample unit and a hypothetical 20% lower bound sample would be more than 20 to 1. Thus, there is almost no current sharing and only a single varistor carries the current. Of course, at low current levels in the range of 10A -100A, this may well be acceptable.

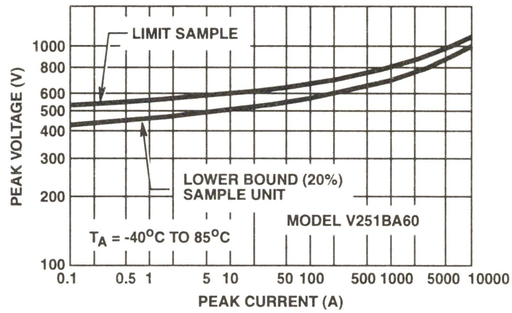


FIGURE 25. PARALLEL OPERATION OF VARISTORS BY GRAPHICAL TECHNIQUE

At high current levels exceeding 1000A, the up-turn region is reached and current sharing improves markedly. For instance, at a clamp voltage of 900V, the respective varistor currents (Figure 25) are 2500A and 6000A, respectively. While far from ideal sharing, this illustration shows the feasibility of paralleling to achieve higher currents and energy than achievable with a single model varistor.

Practically, varistors must be matched by means of high current pulse tests to make parallel operation feasible. Pulse testing should be in the range of over 1kA, using an 8/20μs, or similar pulse. Peak voltages must he read and recorded. High current characteristics could then be extrapolated in the range of 100A - 10,000A. This is done by using the measured data points to plot curves parallel to the data sheet curves. With this technique current sharing can be considerable improved from the near worst-case conditions of the hypothetical example given in Figure 25.

In summary, varistors can be paralleled, but good current sharing is only possible if the devices are matched over the total range of the voltage-current characteristic. In applications requiring paralleling, Harris should be consulted.

Some guidelines for series and parallel operation of varistors are given in Table 4.

TABLE 4. CHECKLIST FOR SERIES AND PARALLEL OPERATION OF VARISTORS

	SERIES	PARALLEL
Objective	Higher Voltage Capability Higher Energy Capability Non-Standard Voltage Capability	Higher Current Capability Higher Energy Capability
Selection Required	No	Yes
Models Applicable	All, must have same I_{TM} rating.	All models
Application Range	All voltages and currents.	All voltages - only high currents, i.e., >100A.
Precautions	I_{TM} ratings must be equal.	Must be identical voltage rated models. Must test and select units for similar V-I characteristics.
Effect on Ratings	Clamp voltages additive. Voltage ratings additive. Current ratings that of single device. Energy W_{TM}, ratings additive.	Current ratings function of current sharing as determined graphically. Energy ratings as above in proportion to current sharing. Clamp voltages determined by composite V-I characteristic of matched units. Voltage ratings that of single unit.

Reference

For Harris documents available on the web, see
http://www.semi.harris.com/
Harris AnswerFAX (407) 724-7800.

[1] Kaufman, R., "The Magic of I^2t," IEEE Trans. IGA-2, No. 5, Sept.-Oct. 1966.

Harris Semiconductor

APP NOTE

No. AN9773 January 1998

Harris Suppression Products

Varistor Testing

Introduction

This note details the common tests of varistor parameters and describes suitable test methods using simplified test circuits.

All tests are performed at 25°C, unless otherwise specified. The test circuits and methods given herein are intended as a general guide. Since the tests frequently entail high voltages and currents, the user must exercise appropriate safety precautions.

Engineering Evaluation

It is important to focus on the key characteristics and ratings to determine if the component can perform as expected. Typically, for a varistor, its nominal voltage, clamping voltage, standby current, insulation resistance, and capacitance are measured. The surge current, or energy, and waveshape available in the circuit together with its frequency of occurrence should be measured or computed. The characteristics of these expected transients should then be checked against the pulse ratings and the power dissipation ratings of the selected varistor type. Where suitable equipment is available, these ratings may be verified.

Product Qualification

A product qualification plan often will be used to detail the electrical and environmental tests to which sample components may be subjected. The suggested electrical characteristics tests could include (with appropriate conditions and limits): nominal varistor voltage, V_N; maximum clamping voltage, V_C; DC standby current, I_D (optional, especially for AC applications); insulation resistance; and capacitance. A test to ensure surge current withstand capability may be included in the qualification plan. This test must be carefully performed and specified (by using either 8/20μs or 10/1000μs waveshapes) consistent with the pulse lifetime rating chart of the varistor selected. Other qualification tests may be used to ensure mechanical integrity, humidity resistance, solderability, and terminal/lead strength.

Incoming Inspection

The equipment maker may wish to verify that shipments received consist of correct parts at the expected quality level. For incoming inspection of Harris Varistors, it is recommended that sample testing include nominal varistor voltage (V_N) tested against the minimum and maximum voltages specified on the purchase drawing/specification. Other electrical sampling tests frequently performed can include insulation resistance and capacitance. Tests such as maximum clamping voltage, V_C, and DC standby current, I_D, are usually checked only on a periodic audit basis.

Field Maintenance

Field maintenance testing is done to verify that the varistor is still providing the intended protection function.

The nominal varistor voltage should be tested against the minimum limits for the model using the method described in the Nominal Varistor Voltage V_N section. If the varistor is open, short, or more than 10% outside either limit, it should be replaced. The DC standby current may also be measured.

Measurement of Varistor Characteristics [1]

Nominal Varistor Voltage V_N

This is measured at a DC test current, I_N of 1mA for product models. A simplified circuit for instrumenting this test, shown in Figure 1, is suitable for varistors up through a rating of $300V_{RMS}$. Above the $300V_{RMS}$ rating, a higher supply voltage will be needed. Resistor R1 has a dual purpose. In conjunction with the variable voltage supply, E1, it forms a quasi-current source providing up to 6mA when switch S1 is closed. Also, R1 is used as a current sensor to measure current flowing through the varistor-under-test. To use the circuit, the operator places switch S2 in position I and S3 into position V_N. A test device is then inserted into the socket and S1 is closed. E1 is then adjusted to obtain a reading of 100V ±5V on the digital voltmeter. Approximately 1mA of current will be flowing in R1. When switch S2 is placed in position V, the varistor voltage will be indicated on the voltmeter. The values of R1 and E1 supply voltage can be scaled appropriately for other voltage-current test points.

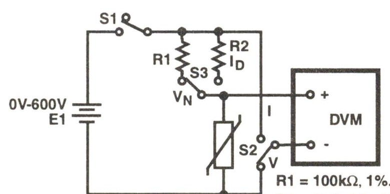


FIGURE 1. SIMPLIFIED CIRCUIT FOR VARISTOR VOLTAGE AND DC STANDBY CURRENT TESTS

If the varistor voltage test is implemented on automatic test equipment, a "soak" time of 20ms minimum should be allowed after application of test current before voltage mea-

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surement. This is necessary to allow varistor voltage to settle toward a steady-state value. Figure 2 illustrates the time response of a specimen varistor with a constant 1.0mA current applied. As can be seen, the varistor voltage initially may rise to a value up to 6% greater than final. With a 20ms or greater soak time, the measured value will differ by less than 2% from the steady-state value.

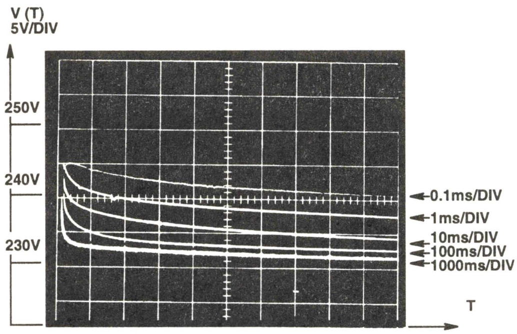

FIGURE 2. VOLTAGE-TIME V(T) CHARACTERISTICS OF A HARRIS VARISTOR (V130LA10A) OPERATING AT A CONSTANT DC CURRENT OF 1.0mA

For varistor models that are commonly used on 60Hz power lines, the V_N limits may be specified for a 1.0mA peak AC current applied. If an AC test is preferred by the user, a schematic approach similar to that shown in Figure 1 is used, except an AC Variac™ is substituted for the DC power supply, and an oscilloscope is substituted for the voltmeter. This circuit is equivalent to that of a typical curve tracer instrument.

To avoid unnecessary concern over minor measurement anomalies, three behavioral phenomena of metal-oxide varistors should be noted. First, it is normal for the peak varistor voltage measured with AC current to be about 2% to 5% higher than the DC value, as illustrated by Figure 3. This "AC-DC difference" is to be expected, since the one-quarter cycle period of a 60Hz wave is much less than the 20ms minimum settling time required for DC readout.

Second, it is normal for the varistor voltage to increase slightly when first subjected to electrical current, as shown in Figure 4. This might be considered a "break-in" stabilization of the varistor characteristics. During normal measurement the voltage shift typically is less than 1%. This voltage shift is of little consequence for most measurement purposes but might be noticeable when viewing a DVM as in the test method of Figure 1. The visual DVM observation should be made shortly after power is applied, with measurement to not more than three significant figures.

Third, it is normal for the varistor voltage-current characteristic to become slightly asymmetrical in polarity under application of DC electrical stress over time. The varistor voltage will increase in the same direction as the polarity of stress, while it will be constant or will decrease in the opposite polarity. This effect will be most noticeable for a varistor that has been subjected to unipolar pulse stresses or accelerated DC life tests. Therefore, to obtain consistent results during unipolar pulse or operating life tests, it is essential to provide a polarity identification for the test specimens. However, for initial readout purposes, this effect usually is insignificant.

Maximum Clamping Voltage, V_C

Two typical current impulses that may be used to define the varistor clamping voltage are the 8/20μs and the 10/1000μs pulses. Figure 5 shows typical varistor test waveforms for these two impulses.

The clamping voltage of a given model varistor at a defined current is related by a factor of the varistor voltage. Therefore, a test of the nominal varistor voltage against specifications may be sufficient to provide reasonable assurance that the maximum clamping voltage specification is also satisfied. When it is necessary to perform the V_C test, special surge generators are required. For shorter impulses than 8/20μs, precautions must be observed to avoid an erroneous "overshoot" in the measurement of the clamping voltage. The Equipment for Varistor Electrical Testing section gives general information on surge generators; a brief description of the "overshoot" effect follows.

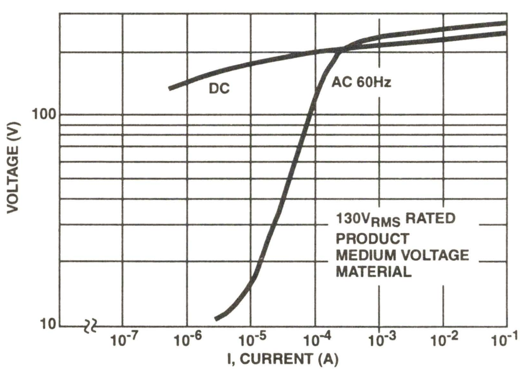

FIGURE 3. AC AND DC CHARACTERISTIC CURVES

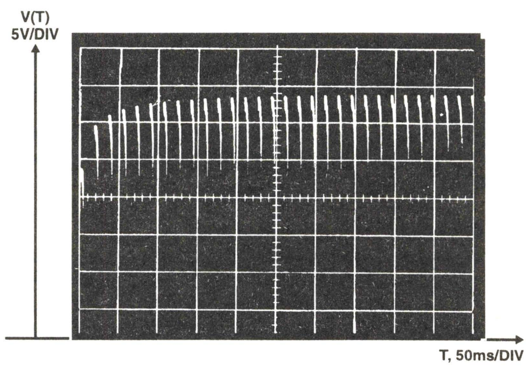

FIGURE 4. V130LA10A) VARISTOR VOLTAGE FOR THE INITIAL CYCLES OF 60Hz OPERATION AT A PEAK CURRENT OF 1.0mA

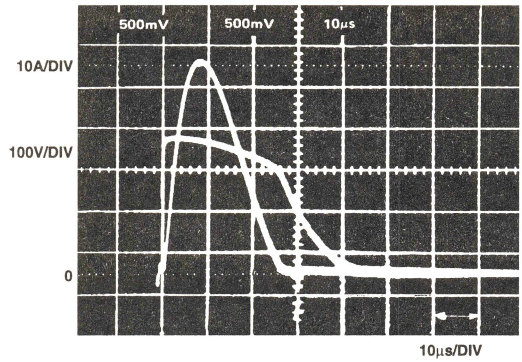

FIGURE 5A. 8/20µs, WAVE I_P = 50A, V_P = 315V

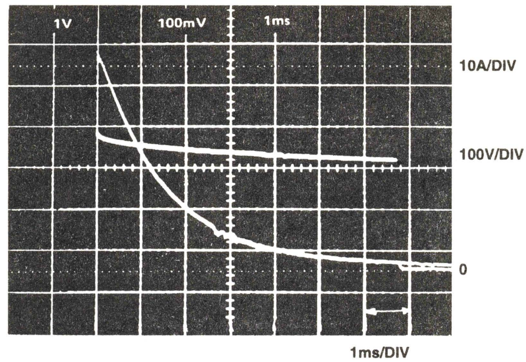

FIGURE 5B. 10/1000µs, WAVE I_P = 50A, V_C = 315V

FIGURE 5. TYPICAL CLAMPING VOLTAGE TEST WAVEFORMS (HARRIS VARISTOR TYPE V130LA10A)

The Harris Varistor specification sheets show the VI characteristic of the devices on the basis of maximum voltage appearing across the device during a current pulse of 8/20µs. If current impulses of equal magnitude but faster rise are applied to the varistor, higher voltages will appear across the device. These higher voltages, described as "overshoot," are partially the result of an intrinsic increase in the varistor voltage, but mostly of the inductive effect of the unavoidable lead length. Therefore, as some applications may require current impulses of shorter rise time than the conventional 8µs, careful attention is required to recognize the contribution of the voltage associated with lead inductance.[1]

The varistor voltage, because of its nonlinearity, increases only slightly as the current amplitude of the impulse increases. The voltage from the lead inductance is strictly linear and therefore becomes large as high current amplitudes with steep fronts are applied. For that reason, it is impractical to specify clamping voltages achieved by lead-mounted devices with current impulses having rise times shorter than 0.5µs, unless circuit geometry is very accurately controlled and described.

To illustrate the effect of lead length on the "overshoot," two measurement arrangements were used. As shown in Figures 6A and 6B, respectively, 0.5cm^2 and 22cm^2 of area were enclosed by the leads of the varistor and of the voltage probe.

The corresponding voltage measurements are shown in the oscillograms of Figures 6C and 6D. With a slow current front of 8µs, there is little difference in the voltages occurring with a small or large loop area, even with a peak current of 2.7kA. With the steep front of 0.5µs, the peak voltage recorded with the large loop is nearly twice the voltage of the small loop. (Note on Figure 6D that at the current peak, L di/dt = 0, and the two voltage readings are equal; before the peak, L di/dt is positive, and after, it is negative.)

Hence, when making measurements as well as when designing a circuit for a protection scheme, it is essential to be alert to the effects of lead length (or more accurately of loop area) for connecting the varistors. This is especially important when the currents are in excess of a few amperes with rise times of less than 1µs.

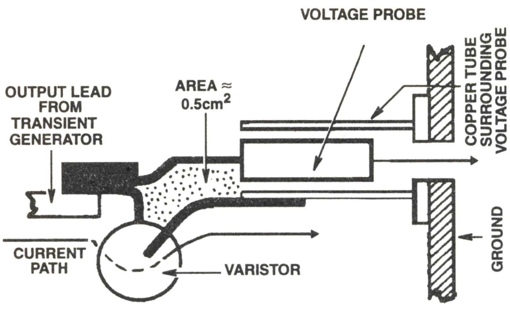

FIGURE 6A. MINIMAL LOOP AREA

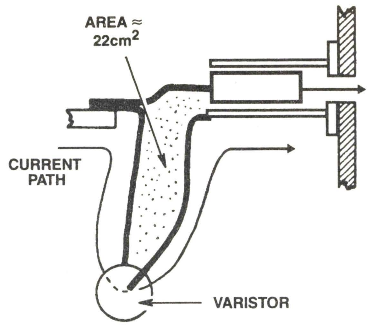

FIGURE 6B. EXCESSIVE LOOP AREA TYPICAL "OVERSHOOT" OF LEAD-MOUNTED VARISTOR WITH STEEP CURRENT IMPULSES

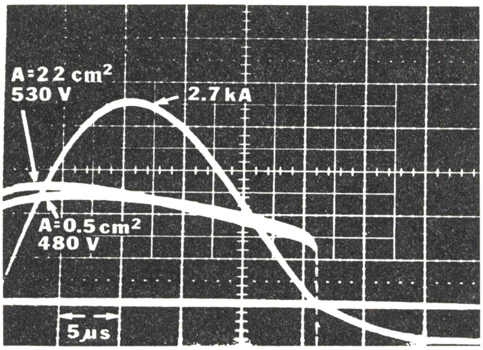

FIGURE 6C. CURRENT RISE OF 8µs

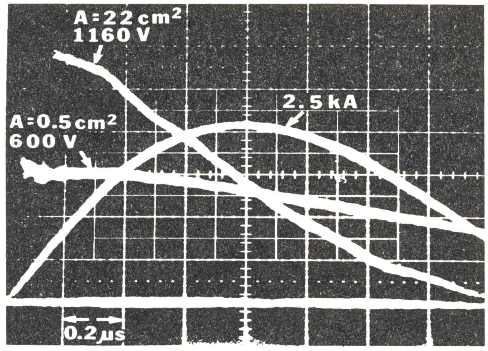

FIGURE 6D. CURRENT RISE OF 0.5µs

FIGURE 6. EFFECT OF LEAD LENGTH ON "OVERSHOOT"

With reasonable care in maintaining short leads, as shown in Figure 6A, it is possible to describe the "overshoot" effect as an increase in clamping voltage relative to the value observed with a 8/20µs impulse. Figure 7 shows a family of curves indicating the effect between 8µs and 0.5µs rise times, at current peaks ranging from 20A to 2000A. Any increase in the lead length, or area enclosed by the leads, would produce an increase in the voltage appearing across the varistor terminals - that is, the voltage applied to the protected load.

DC Standby Current, I_D

This current is measured with a voltage equal to the rated continuous DC voltage, $V_{M(DC)}$, applied across the varistor. The circuit of Figure 1 is applicable where current sensing resistor R2 has a value of 1000Ω. The test method is to set the voltage supply, E1, to the specified value with switch S1 closed and S2 in the V position. Then S2 is placed in position I and S3 in position, I_D. S1 is then opened, the test device is inserted in the test socket, and S1 is closed. The DVM reading must be converted into current. For example, if a maximum standby current of 200µA is specified, the maximum acceptable DVM reading would be 0.200V.

The measurement of DC standby current can be sensitive to the device behavioral phenomena of "break-in" stabilization and polarization of the VI characteristics, as described in the Nominal Varistor Voltage V_N section. If the device under test has prior unipolar electrical history, polarity indicators should be observed and test values interpreted accordingly.

The value of DC standby current also can be sensitive to ambient temperature. This is unlike varistor characteristics measured at currents of 1mA or greater, which are relatively insensitive to ambient temperatures. With $V_{M(DC)}$ around 85% of V_N, Figure 8 shows the typical DC standby current of a model V130LA10A varistor in the order of 10µA or 20µA at room temperature. I_D increases to about 80µA at 85°C, the maximum operating temperature without derating.

Capacitance

Since the bulk region of a Harris Varistor acts as a dielectric, the device has a capacitance that depends directly on its area and varies inversely with its thickness. Therefore, the capacitance of a Harris Varistor is a function of its voltage and energy ratings. The voltage rating is determined by device thickness, and the energy rating is directly proportional to volume.

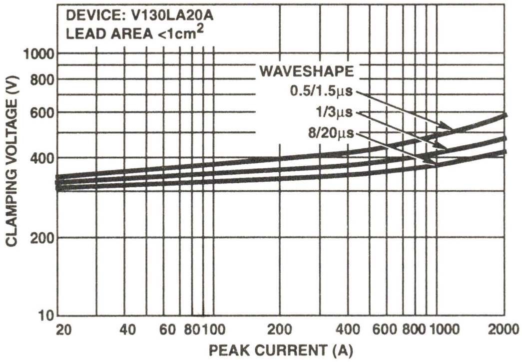

FIGURE 7. TYPICAL "OVERSHOOT" OF LEAD-MOUNTED VARISTOR WITH STEEP CURRENT IMPULSES

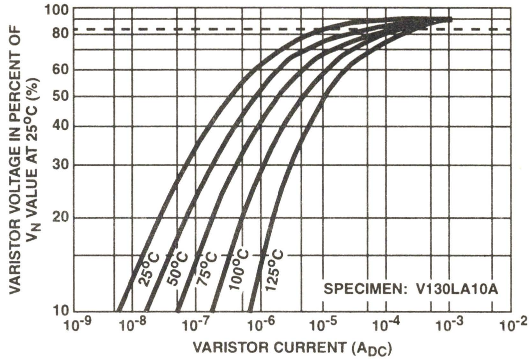

FIGURE 8. TYPICAL TEMPERATURE DEPENDENCE OF DC STANDBY CURRENT VARISTOR TYPE V130LA10A

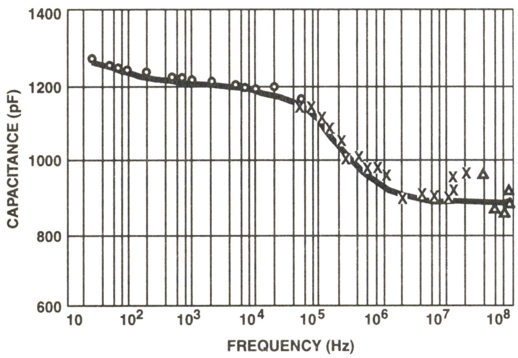

FIGURE 9. CAPACITANCE VARIATION WITH FREQUENCY

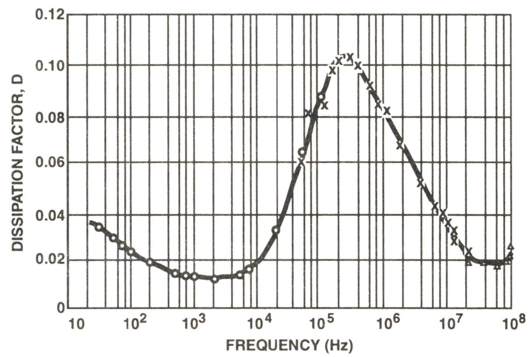

FIGURE 10. DISSIPATION FACTOR VARIATION WITH FREQUENCY

Harris Varistor capacitance can be measured through use of a conventional capacitance bridge and is found to vary with frequency, as shown in Figure 9. Typically, capacitance measurements are made at 1MHz. Dissipation factor also is frequency-dependent, as shown in Figure 10.

When measured with a DC bias, the capacitance and dissipation factor show little change until the bias approaches or exceeds the V_N value. Furthermore, the capacitance change caused by an applied voltage (either DC or AC) may persist when the voltage is removed, with the capacitance gradually returning to the prebias value. Because of this phenomenon, it is important that the electrical history of a Harris Varistor be known when measuring capacitance.

Miscellaneous Characteristics

A number of characteristic measurements can be derived from the basic measurements already described, including the nonlinear exponent (alpha), static resistance, dynamic impedance, and voltage clamping ratio. The data, however, may be obtained by measurement methods similar to those already given for nominal varistor voltage and maximum clamping voltage. These miscellaneous characteristics may be useful in some cases to enable comparison of Harris Varistors with other types of nonlinear devices, such as those based on silicon carbide, selenium rectifier or zener diode technologies.

Varistor Rating Assurance Tests

Continuous Rated RMS and DC Voltage [$V_{M(AC)}$ and $V_{M(DC)}$]

These are established on the basis of operating life tests conducted at the maximum rated voltage for the product model. These tests usually are conducted at the maximum rated ambient operating temperature, or higher, so as to accelerate device aging. Unless otherwise specified, end-of-lifetime is defined as a degradation failure equivalent to a V_N shift in excess of ±10% of the initial value. At this point the device is still continuing to function. However, the varistor will no longer meet the original specifications.

A typical operating life test circuit is shown in Figure 11. If the varistor is intended principally for a DC voltage application, then the AC power source should be changed to DC. It

is desirable to fuse the varistors individually so testing is not interrupted on other devices if a fuse should blow. The voltage sources should be regulated to an accuracy of ±2% and the test chamber temperature should be regulated to within ±3°C. The chamber should contain an air circulation fan to assure a uniform temperature throughout its interior. The varistors should receive an initial readout of characteristics at room ambient temperature i.e., 25 ±3°C. They should then be removed from the chamber for subsequent readout at 168,500, and 1000 hours. A minimum of 20 minutes should be allowed before readout to ensure that the devices have cooled off to the room ambient temperature.

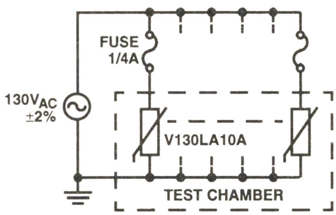

FIGURE 11. SIMPLIFIED OPERATING LIFE TEST CIRCUIT

Transient Peak Current, Energy, Pulse Rating, and Power Dissipation Ratings

Special surge generator equipment is required for testing. Since high energy must be stored at high voltages to perform these tests, especially on larger sizes of Harris Varistors, the equipment must be operated using adequate safety precautions.

The peak current rating, I_{TM} of Harris Varistors is based on an 8/20µs test impulse waveshape. The specifications include a maximum single value in the ratings table. A pulse rating graph defines the peak current rating for longer impulse duration as well, such as for a 10/1000µs wave. A family of curves defines the rated number of impulses with a given impulse duration and peak current.

Energy rating, W_{TM}, is defined for a 10/1000µs current impulse test wave. This waveshape has been chosen as being the best standard wave for tests where impulse energy, rather than peak current, is of application concern. A direct determination of energy dissipated requires that the user integrate over time the product of instantaneous voltage and current.

Peak voltage and current are readily measured with available equipment. Therefore, the energy rating can be tested indirectly by applying the rated peak impulse current of a 10/1000µs waveshape to the test specimen. Then, the energy dissipated in the varistor can be estimated from the known pulse waveshape. For a 10/1000µs waveshape the approximate energy is given by the expression $E = 1.4V_C\, I\tau$.

For example, a model V130LA10A varistor has a single pulse rating for a 10/1000µs impulse waveshape of about 75A peak, and a maximum clamping voltage at 75A of about 360V. Thus, the computation of estimated energy dissipation is 38J.

The transient power dissipation rating, P_{TAM}, is defined as the maximum average power of test impulses occurring at a specified periodic rate. It is computed as the estimated energy dissipation divided by the test pulse period. Therefore, varistors can be tested against this rating by applying two or more impulses at rated current with a specified period between pulses. For example, a model V130LA10A varistor has a pulse rating of two 10/1000µs test impulses with a peak current of about 65A. The estimated energy dissipation per pulse computed as per the preceding example is about 30J. If a period of 50s is allowed after the first test pulse, the estimated average power dissipation can be computed as about 0.6W, which is the specification rating. It should be noted that Harris Varistors are not rated for continuous operation with high-level transients applied. The transient power dissipation rating is based on a finite number of pulses, and the pulse rating of the varistor must be observed. See Figure 12.

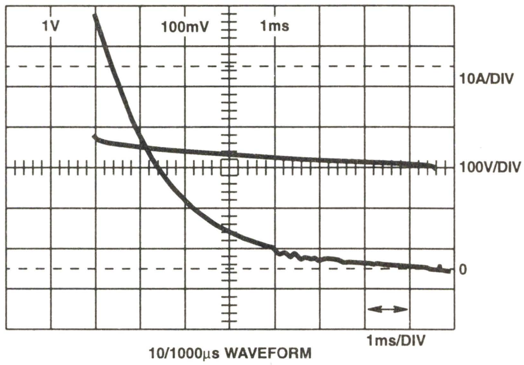

FIGURE 12. SURGE TEST WAVEFORMS

Table 1 outlines a suggested program of testing to verify varistor transient and pulse ratings with a minimum of expensive, time-consuming testing. New specimens should be used for each test level and failure judged according to the specification criteria.

TABLE 1. TESTING OF TRANSIENT CURRENT, ENERGY, PULSE RATING, AND POWER DISSIPATION RATINGS

TEST PARAMETER	NO. PULSES AT RATED CURRENT (ALTERNATING POLARITY)	TEST WAVE-SHAPE (µs)	MINIMUM PULSE PERIOD (s)
Maximum Peak Current	1 (same polarity as readout)	8/20	NA
Pulse/Energy Rating, Power Dissipation	2	10/1000 or 2ms square wave	50
Pulse Rating	10	8/20	25
Pulse Rating	100	8/20	12

Continuous Power Dissipation

Since Harris Varistors are used primarily for transient suppression purposes, their power dissipation rating has been defined and tested under transient impulse conditions. If the devices are to be applied as threshold sensors or coarse voltage regulators in low power circuits, then a dissipation test under continuous power is more appropriate. This continuous power test will aid the user in determining if the device is suitable for his specific application.

A circuit for continuous power dissipation testing is shown in Figure 13. The DC power supply voltage should be set to a value of approximately twice the nominal varistor voltage of the product model under test. In that case, nearly constant power dissipation is maintained in the varistor. Since the circuit transfers nearly equal power to the series resistor and varistor-under-test, the series resistor value is simply chosen to achieve the test design value of power dissipation. In Figure 13 a nearly constant power dissipation of about 0.6W is obtained.

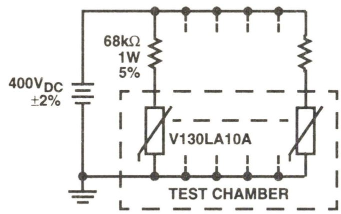

FIGURE 13. CONSTANT POWER LIFE TEST CIRCUIT

Mechanical and Environmental Testing of Varistors

Introduction

Many tests have been devised to check the reliability of electronic components when subjected to mechanical and environmental stresses. Although individual equipment makers may specify their own tests on component purchase documents, these tests are often based on an equivalent MIL-STD specification. Therefore, it is convenient to summarize these tests in MIL-STD terms. Since the ratings of Harris Varistors may vary with product series and model, the test conditions and limits should be as specified on the applicable detail specification.

Harris Varistors are available in a high reliability series. This series incorporated most standard mechanical and environmental tests, including 100% pre-screening and 100% process conditioning.

UL Recognition Tests

The standards of Underwriters Laboratories, Inc. (UL) under which applicable Harris Varistors have been tested and recognized are:

- UL-1449 Transient Voltage Surge Suppressors, File E75961
- UL-1414 Across the Line Components, File E56529
- UL-497B Protectors for Data Communications, File E135010

The tests were designed by UL and included discharge (withstand of charged capacitor dump), expulsion (of complete materials), life, extended life, and flammability (UL94V0) tests, etc.

Equipment for Varistor Electrical Testing

Impulse Generators

A convenient method of generating current or voltage surges consists of slowly storing energy in a capacitor network and abruptly discharging it into the test varistor. Possible energy storage elements that can be used for this purpose include lines (lumped or distributed) and simple capacitors, depending on the waveshape desired for the test. Figure 14 shows a simplified schematic for the basic elements of an impulse generator.

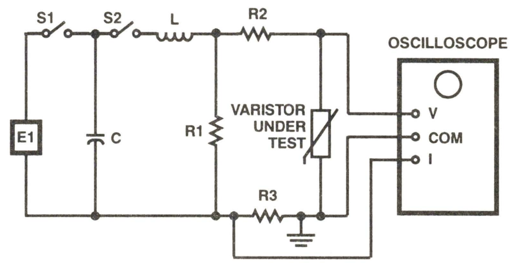

FIGURE 14. SIMPLIFIED CIRCUIT OF SURGE IMPULSE GENERATOR

The circuit is representative of the type used to generate exponentially decaying waves. The voltage supply, E1, is used to charge the energy storage capacitor, C, to the specified open-circuit voltage when switch S1 is closed. When switch S2 (an ignition or a triggered gap) is closed, the capacitor, C, discharges through the waveshaping elements of the circuit into the suppressor device under test. With capacitances in the order of 1µF to 10µF and charging voltages of 10kV to 20kV, the typical 8/20µs or 10/1000µs impulses can be obtained by suitable adjustment to the waveshaping components L, R1, and R2, according to conventional surge generator design.[2, 3, 4, 5]

Measurement Instrumentation

Transient measurements include two aspects of varistor application: (1) detection of transients to determine the need for protection, and (2) laboratory measurements to evaluate varistor performance. Transient detection can be limited to recording the occurrence of transient overvoltages in a particular system or involve comprehensive measurements of all the parameters which can be identified. Simple detection can be performed with peak-indicating or peak-recording instruments, either commercial or custom-made.

Test Waves and Standards

The varistor test procedures described in this section have been established to ensure conformity with applicable standards,[6] as well as to reflect the electromagnetic environment of actual circuits[7] which need transient protection.

Test Waves

A number of test waves have been proposed, in order to demonstrate capability of survival or unimpeded performance in the environment. A proposal also has been made to promote a transient control level concept[7] whereby a few selected test waves could be chosen by common agreement between users and manufacturers. The intent being that standard test waves would establish certain performance criteria for electronic circuits.

Source Impedance

The effective impedance of the circuit which introduces the transient is an extremely important parameter in designing a protective scheme. Impedance determines the energy and current-handling requirements of the protective device.

When a transient suppressor is applied, especially a suppressor of the energy-absorbing type, such as a varistor, the transient energy is then shared by the suppressor and the rest of the circuit, which can be described as the "source".

As in the case of waveshapes, various proposals have been made for standardizing source impedances. The following list summarizes the various proposals intended for AC power lines:

1. The Surge Withstand Capability (SWC) standard specified a 150Ω source.
2. The Ground Fault (UL-GFCI) standard is 50Ω source.[8]
3. The Transient Control Level (TCL) proposals of Martzloff et al [7] include a 50Ω resistor in parallel with a 50μH inductor.
4. The installation category concept of ANSI/IEEE Standard C62.41-1980 implies a range of impedances from 1Ω to 50Ω as the location goes from outside to inside.
5. The FCC regulation for line-connected telecommunication equipment implies a 2.5Ω source impedance.[9] However, the requirement of the FCC is aimed at ensuring a permanent "burning" of a dielectric puncture and does not necessarily imply that the actual source impedance in the real circuits is 2.5Ω.
6. Reported measurements[10] indicate the preponderance of the inductance in branch circuits. Typical values are μH per meter of conductors.
7. There is no agreement among the above proposals on a specific source impedance. Examining the numbers closer, one can observe that there is a variance between 2.5Ω to about 50Ω. Going back to ANSI/IEEE Standard C62.41-1980 by using the OCV (open circuit voltage) and SCI (short circuit current) for the different location categories, one can calculate a source impedance.

Any practical power circuit will always have some finite impedance due to the resistance and inductance of the power line and distribution transformer. Table 2 shows representations of the surge source impedance implied in the environment description of ANSI/IEEE C62.41-1980.

TABLE 2. SOURCE IMPEDANCE AT DIFFERENT LOCATION CATEGORIES IN LOW VOLTAGE AC SYSTEMS (UP TO 1000V)

Category A Ring Wave	6kV/200A = 30Ω
Category B Ring Wave	6kV/500A = 12Ω
Category B Impulse	6kV/3kA = 2Ω
Category C Impulse	10kV/10kA = 1Ω

The impedance of industrial or commercial systems generally supplied by underground entrances, or a separate substation of relatively large kVA rating, tends to be low, and the injection of any lightning transients occurs at a remote point. This results in lower transient peaks than those that can be expected in residential circuits, but the energy involved may be, in fact, greater. Therefore, transient suppressors intended for industrial use should have greater energy-handling capability than the suppressors recommended for line-cord-powered appliances.

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Harris AnswerFAX (407) 724-7800.

[1] Fisher, F.A., "Overshoot - A Lead Effect in Varistor Characteristics," Report 78CRD, General Electric, Schenectady, N.Y., 1978.

[2] Heller, B. and A. Veverka, "Surge Phenomena in Electrical Machine", ILIFFE Books Ltd., London, 1968.

[3] Greenwood, Allen, "Electrical Transients in Power Systems", Wiley Interscience, New York, 1971.

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[6] "Test Specifications for Varistor Surge-Protective Devices", ANSI/IEEE Std. C62.33, 1982.

[7] Martzloff, F.D., and F.A. Fisher, "Transient Control Level Philosophy and Implementation - The Reasoning Behind the Philosophy," 77CH1224-5EMC, "Proceedings of the 2nd Symposium on EMC", Montreux, June 1977.

[8] "Standard for Safety: Ground Fault Circuit Interrupters," UL943, Underwriters Laboratories, May 12,1976.

[9] "Longitudinal Voltage Surge Test #3," Code of Federal Regulations, Section 68.302(e), Title 47, Telecommunications.

[10] F.D. Martzloff, "The Propagation and Attenuation of Surge Voltages and Surge Currents in Low-Voltage AC Circuits," IEEE Transactions on Power Apparatus and Systems, PAS-102, pp. 1163-1170, May 1983.

Harris Semiconductor

APPNOTE

No. AN9774 January 1998 **Harris Suppression Products**

Surgectors for Telecommunications Systems

Introduction

This note discusses transient voltages associated with telephone line applications and highlights the attributes of the Harris surgector products as a means to suppress these transients.

System Transients

A telecommunication system can include subscriber stations linked together through the cable plant and a central office switching network. Included in the system are repeater amplifiers, multiplexers, and other electronic circuits. Supplying the electrical energy to run the system is a main power source.

The cable plant and the power supply provide a path by which damaging transients enter the system, to be transmitted to vulnerable electronic circuitry. The cable plant consists of conductors in shielded cables, which are suspended on poles (shared with power lines) or buried in the earth. A single cable is made up of many conductors, arranged in twisted pairs (tip and ring). These cables (even the ones underground) are susceptible to transient energy from lightning and conducting them to the central office or subscriber equipment.

The power used by a telecommunication system is usually obtained from commercial power lines. These lines, like the telephone cables, are either suspended on poles or buried. Transient energy can be induced into power lines and transmitted to the central office by direct conduction or by induction into the telephone cable plant.

Lightning - Induced Transients

Lightning is a common source of over voltage in communication systems. Quantitative information on lightning has been accumulated from many sources,[2] with research centers in the United States, Western Europe and South Africa. One of the most comprehensive surveys of available data has been compiled by Cianos and Pierce,[3] describing the amplitude, rate-of-rise, duration, etc., in statistical terms.

Lightning currents may enter the conductive shield of a suspended cable by direct or indirect stroke, or it may enter a cable buried in the ground by ground currents, as shown in Figure 1.

In the case of a suspended cable, the lightning current that enters the cable is seeking a ground and will travel in both directions along the cable. Some of the current will leave the shield at each grounded pole along its path.

Stroke currents leave a buried cable in a similar way but with a different mechanism. Since the cable shield has a finite electrical resistance, the current passing through it will produce a potential gradient along its length. This voltage will produce a potential difference between the cable and the soil, as shown in Figure 2.

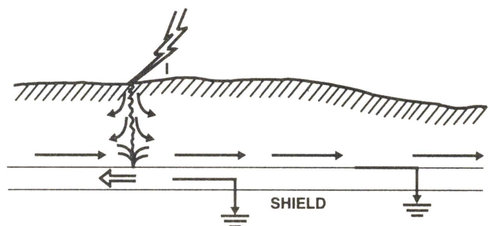


FIGURE 1. LIGHTNING CURRENT IN BURIED CABLE

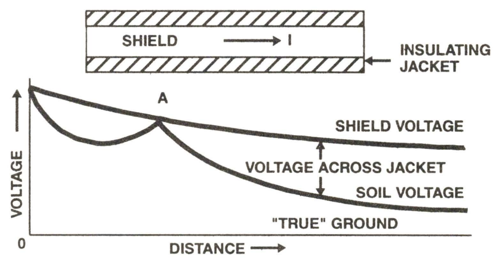


FIGURE 2. CONDITION FOR PUNCTURE OF CABLE JACKET

At some point (Point A) the shield-to-earth potential will exceed the dielectric strength of the jacket, causing it to puncture. Some of the lightning current then flows through the puncture into the soil, thus equalizing the potential at that point. The remaining current continues along the shield until another puncture occurs, providing another path to ground.

The surge voltage that appears at the ends of the cable depends upon the distance to the disturbance, the type of cable, the shield material, and its thickness and insulation, as well as the amplitude and waveshape of the lightning current in the shield.

Calculations of Cable Transients

The voltage surge induced into the conductors of a cable will propagate as a traveling wave in both directions along the cable from the region of induction. The cable acts as a transmission line. The surge current and voltage are related to each other by Ohm's law where the ratio of voltage to current is the surge impedance (Z_0) of the cable. Z_0 can also be expressed in terms of the inductance (L) and capacitance (C) per unit length of the cable by the equation,

$$Z_0 = \sqrt{L/C}(\Omega)$$

The series resistance of the shield and conductors, as well as losses due to corona and arcing, determine the energy lost as the disturbance propagates along the cable.

Tests conducted on telephone cables[4] have measured surge impedances of 80Ω between any of the conductors and the shield. Shield resistances between 5Ω and 6Ω per mile were found to be typical. These values and the applied lightning current waveform of Figure 3 were used to compute the worst case transient which would appear at cable terminals in a central office. The computation assumes the lightning current is introduced into a suspended cable shield at a point 2.75 miles from the central office. An average cable span between poles of 165 feet, with a ground connection on every fourth pole, was assumed. It was also assumed that the cable will support the voltage without arcing over.

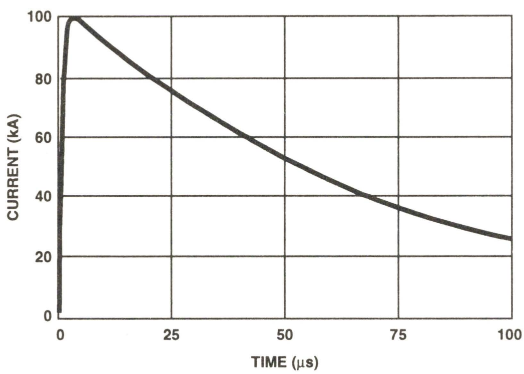


FIGURE 3. SEVERE LIGHTNING CURRENT WAVEFORM (2/50µs)

The resulting short-circuit current available at the central office is shown in Figure 4.

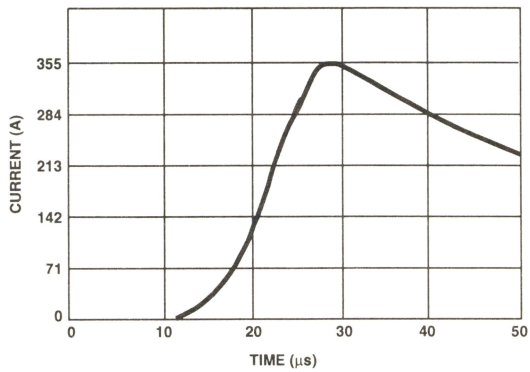


FIGURE 4. AVAILABLE CURRENT 2.75 MILES FROM 100kA LIGHTNING STROKE

The open-circuit voltage at the cable end is shown in Figure 5. This analysis shows that if a severe, 100kA lightning flash strikes a cable at a point 2.75 miles from a central office, a voltage transient reaching a peak of nearly 18kV may appear at the cable end, with about 355A of current available.

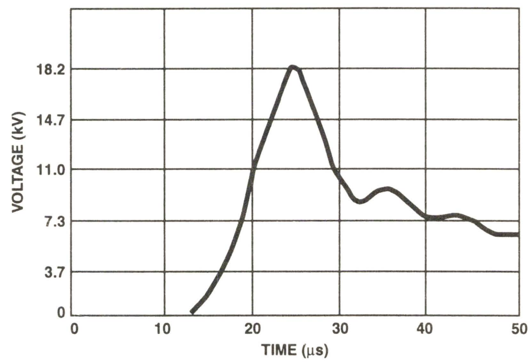


FIGURE 5. OPEN CIRCUIT VOLTAGE 2.75 MILES FROM 100kA LIGHTNING STROKE

The open-circuit voltage and available current which would result from stroke currents of various magnitudes is given in Table 1. Included in the table is the probability of occurrence, as given by Cianos and Pierce.[3] It should be realized that voltages in excess of 10kV probably would not be sustained due to cable insulation breakdown.

The values in Table 1 are based on the assumption of a single conductor cable with the stroke point 2.75 miles from the central station. For closer strokes the peak short-circuit current at the cable end will increase as shown in Table 2. These calculations were made assuming a breakdown at the stroke point, which gives the worst case result.

TABLE 1. LIGHTNING TRANSIENTS AT CABLE END 2.75 MILES FROM STROKE POINT

PEAK CURRENT (kA)	PROBABILITY OF OCCURRENCE (%)	TERMINAL OPEN CIRCUIT VOLTAGE (PEAK V)	TERMINAL SHORT-CIRCUIT CURRENT (PEAK A)
175	1	32,200	621
100	5	18,400	355
60	15	11,040	213
20	50	3,680	71

Since telephone cables actually have many pairs of wires rather than a single conductor, the peak currents in each wire will vary.

Assume a cable of six pairs is struck by lightning, inducing a stroke current of 100kA into the shield, at a distance of 0.25 mile from the protector. The transient current will be divided up among the twelve suppressors at the cable ends. Each protective device must handle up to 852A of peak current in order to clamp the voltage to a protected level.

TABLE 2. PEAK LIGHTNING-INDUCED CURRENTS IN VARIOUS LENGTHS OF TELEPHONE CABLE (100kA LIGHTNING STROKE)

DISTANCE TO STROKE (MILES)	PEAK CURRENTS (A)			
	AT STROKE POINT	AT CENTRAL OFFICE		
		SINGLE CONDUCTOR	6 PAIR CABLE	12 PAIR CABLE
2.75	630	355	-	-
1.50	630	637	-	-
1.00	734	799	-	-
0.50	1110	1120	712	453
0.25	1480	1480	852	463

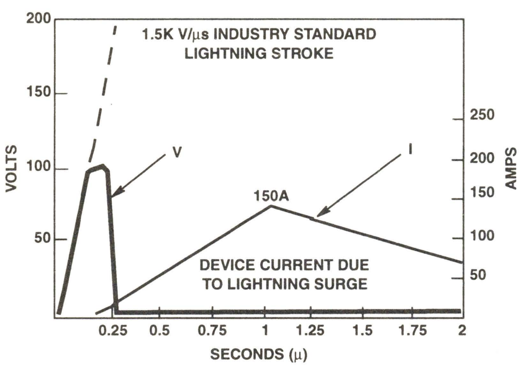


FIGURE 6. INDUSTRY STANDARD LIGHTNING STROKE

Power System Induced Transients

Since telephone cables very often share a pole and ground wire with the commercial AC utility power system, the high currents that accompany power system faults can induce over-voltages in the telephone cables. These faults can have long duration (compared to the lightning-induced transients) from a few milliseconds to several cycles of power frequency. Three types of over-voltage can occur in conjunction with power system faults:

Power Contact - (Sometimes called "power cross"). The power lines fall and make contact with the telephone cable.

Power Induction - The electromagnetic coupling between the power system experiencing a heavy fault and the telephone cable produces an over-voltage in the cable.

Ground Potential Rise - The heavy ground currents of power system faults flow in the common ground connections and cause substantial differences in potential.

Surgector Transient Voltage Surge Suppressors

The need for a surge suppressor stems from the increasing sophistication of electronics in the telecommunications industry. For example, the use of medium scale integreated (MSI) and very large-scale integrated (VLSI) circuits. These devices are used in equipment that transmits, processes, codes, switches, stores data, and has multifunction capability, but may be intolerant of voltage overloads.

The surgector is a monolithic silicon device. It consists of an SCR-type thyristor whose gate region contains a special diffused section that acts as a zener (avalanche) diode.

It combines the continuous voltage protection of the zener with the thyristor's ability to handle high current. As a result, the surgector can provide the much-needed secondary surge protection for telecommunications circuitry, data links, and other sensitive electronic circuits that are especially susceptible to damage from transient voltage.

Harris surgectors are listed as recognized components to UL497B standard for protectors.

Surgector Characteristics Include

- High input impedance until breakdown (i.e. low leakage)
- Repeatable breakdown/threshold voltage
- High surge current handling capability
- Responds to rapidly reoccurring surges
- Bidirectional protection
- No degradation of characteristics with use

Figure 7 shows the structure in cross section.

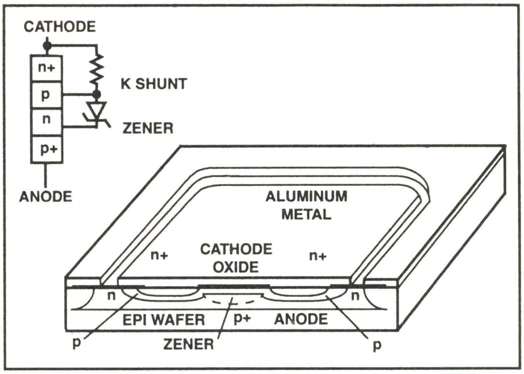


FIGURE 7. SURGECTOR VERTICAL STRUCTURE

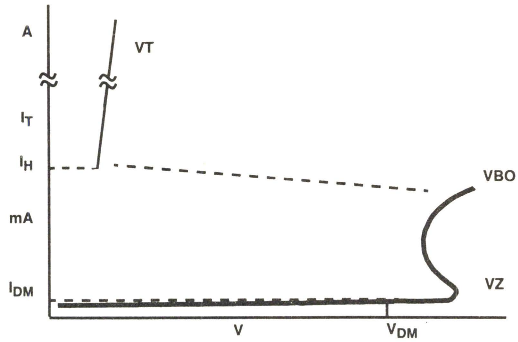
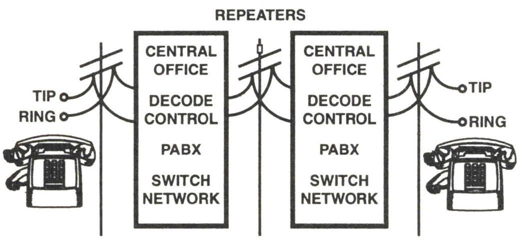


FIGURE 8. TYPICAL VOLT-AMPERE CHARACTERISTICS

Surgectors Provide Transient Protection for:

- Central Office Equipment
- Supervisory Equipment
- Switchgear Equipment
- Data Transmission
- Handsets
- EPABX, PABX, PBX
- Repeaters
- Line Concentrator
- Receivers
- Headsets
- Modem
- PCM



Surgector Operation

With its low leakage and low capacitance, the surgector allows normal operation of the circuit. Surgector devices are rated at 30V, 60V, 100V, 230V, and 270V. When a transient voltage reaches the avalanche breakdown voltage, the zener instantly clamps the voltage, as shown in Figure 8.

The current flows from the zener region into the thyristor gate, switching on the thyristor. The thyristor drops to low voltage, creating a low impedance in the circuit, and shunts the excess energy from the circuit to the ground.

While the transient is present, the surgector remains in the ON state, and the voltage across the circuit is low. Its precise value depends on the type of pulse and the type of surgector being used. When current falls to the "holding current," limit the surgector turns off.

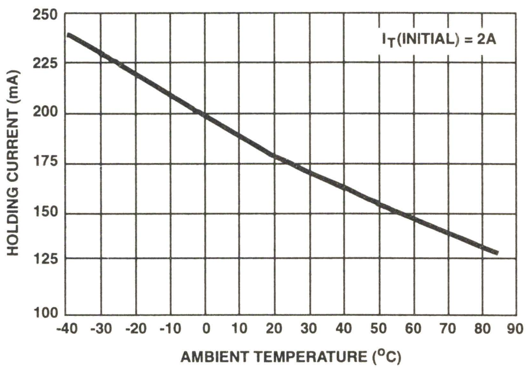


FIGURE 9. TYPICAL HOLDING CURRENT vs TEMPERATURE

Surgector Types

Harris surgector devices include Variable Clamp, Unidirectional and Bidirectional types. The variable clamp type is unidirectional but provides three terminals instead of two. The third terminal gives the user direct access to the SCR gate region. With this external gate control circuitry, any voltage between 5V and 270V can trigger the device depending on the type.

The Unidirectional and Bidirectional surgectors have two terminals, and are internally triggered at voltges between 30V and 270V, depending on the type.

Performance Characteristics

- Surgector devices have ratings for transient peak surge current of 300 to 600A for a 1 x 2μs pulse and appropriately scaled currents at 8 x 20, 10 x 560, and 10 x 1000μs. These rated surges can be applied to the surgector devices repeatedly without degradation.
- The surgector clamps the transient voltage within nanoseconds.
- The surgector is designed not to fail to an open condition on a 1 x 2 pulse below 450A (900A for the SGT27B27). This becomes especially important in telecom equipment designs which are required to meet UL-1459 requirements.
- There is no inherent limit on the surgector device's operating life.
- Surgector devices switch to the off-state once the pulse current drops below the intentionally high holding current threshold. (The holding current of the surgector must be greater than the normally available short-circuit current in the circuit to ensure that the surgector will return to the off-state.)
- Leakage is low; less than 50nA.
- The capacitance of surgector devices is also low, presenting about 50pF.

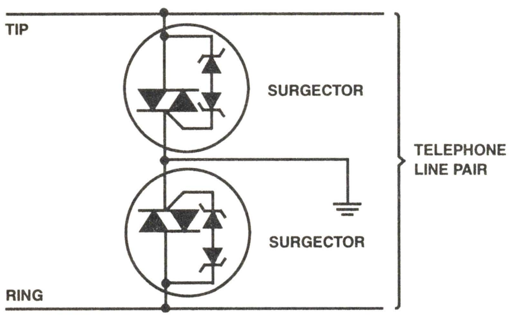


FIGURE 10. APPLICATION EXAMPLE OF TWO BIDIRECTIONAL SURGECTOR DEVICES PLACED BETWEEN THE TIP AND RING LINES

References

For Harris documents available on the web, see
http://www.semi.harris.com/
Harris AnswerFAX (407) 724-7800.

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[2] Golde, R.II., "Lightning Currents and Related Parameters," Lightning, Vol. 1, Physics of Lightning, Chapter 9, ed. R.H. Golde, Academic Press, 1977.

[3] Cianos, N. and E.T. Pierce, "A Ground Lightning Environment for Engineering Usage," Report No. 1, Stanford Research Institute, August 1972.

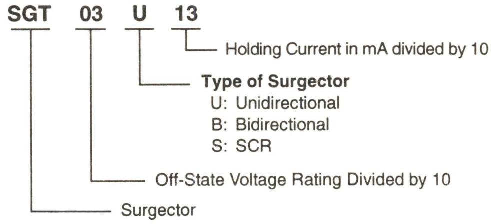
[4] Boyce, C.F., "Protection of Telecommunication Systems," Lightning, Vol. 2, Lightning Protection, Chapter 25, ed. R.1I. Golde, Academic Press, 1977.

[5] "Connection of Terminal Equipment to the Telephone Network," Federal Communications Commission Rules and Regulations, part 68, October 1982.

Nomenclature and Packages

Surgector type numbers use the following format: The first three characters - "SGT" - stand for surgector. The next two digits represent the maximum off-state voltage divided by 10. Following the voltage is a letter indicating either SCR (S), Unidirectional (U), or Bidirectional (B). The next two digits indicate holding current in milliamps divided by 10.

All versions of the surgector are housed in a modified TO-202 plastic package.



Surgector Packages

MODIFIED TO-202
PACKAGE STYLE

PACKAGE A PACKAGE B

TABLE 3. SURGECTOR TYPES AND KEY PARAMETERS

PART NUMBER	FUNCTION	V_Z MIN (V)	V_{BO} MAX (100V/µs)	I_{TSM} (1 x 2µs)	I_{TSM} (10 x 1000µs)	I_H (mA)	PACKAGE STYLE
SGT10S10 (Note 1)	VAR Clamp	100	Note 1	300	100	> 100	A
SGT27S10 (Note 1)	VAR Clamp	270	Note 1	300	100	> 100	A
SGT27S23 (Note 1)	VAR Clamp	270	Note 1	300	100	> 230	A
SGT03U13	Unidirectional	30	< 50	300	100	> 130	B
SGT06U13	Unidirectional	60	< 85	300	100	> 130	B
SGT23U13	Unidirectional	230	< 275	300	100	> 130	B
SGT21B13	Bidirectional	210	270	300	100	>130	B
SGT21B13A	Bidirectional	210	290	300	100	>130	B
SGT22B13	Bidirectional	220	280	300	100	>130	B
SGT22B13A	Bidirectional	220	290	300	100	>130	B
SGT23B13	Bidirectional	230	290	300	100	>130	B
SGT23B13A	Bidirectional	230	315	300	100	>130	B
SGT27B13	Bidirectional	270	345	300	100	>130	B
SGT27B13A	Bidirectional	270	360	300	100	>130	B
SGT27B13B	Bidirectional	270	375	300	100	>130	B
SGT27B27	Bidirectional	270	345	600	200	>270	B
SGT27B27A	Bidirectional	270	360	600	200	>270	B
SGT27B27B	Bidirectional	270	375	600	200	>270	B

NOTES:

1. Dependent on trigger circuit.
2. All surgectors supplied in modified JEDEC TO-202 Package.
   Package Style A = 3 lead version
   Package Style B = 2 lead version
3. All devices UL recognized to 497B - File Number E135010.

TVS 12

HARRIS QUALITY AND RELIABILITY

Harris Quality

Introduction

Harris Semiconductor's commitment to supply only top value products has made quality improvement a mandate for every person in our work force – from circuit designer to manufacturing operator, from hourly employee to corporate executive. Price is no longer the only determinant in marketplace competition. Quality, reliability, and performance enjoy significantly increased importance as measures of value in the finished product.

Quality cannot be added or considered after the fact. It begins with the development of capable process technology and product design. It continues in manufacturing, through effective controls at each process or step. It culminates in the delivery of products which meet or exceed the expectations of the customer.

The Role of the Quality Organization

The emphasis on building quality into the design and manufacturing processes of a product has resulted in a significant refocus of the role of the Quality organization. In addition to facilitating the development of SPC and DOX, Quality professionals support other continuous improvement tools such as control charts, measurement of equipment capability, standardization of inspection equipment and processes, procedures for chemical controls, analysis of inspection data and feedback to the manufacturing areas, coordination of efforts for process and product improvement, optimization of environmental or raw materials quality, and the development of quality improvement programs with vendors.

At critical manufacturing operations, process and product quality is analyzed through random statistical sampling and product monitors. The Quality organization's role is changing from policing quality to leadership and coordination of quality programs or procedures through auditing, sampling, consulting, and managing Quality Improvement projects.

To support specific market requirements, or to ensure conformance to military or customer specifications, the Quality organization still performs many of the conventional quality functions (e.g., group testing for military products or wafer lot acceptance). But, true to the philosophy that quality is everyone's job, much of the traditional on-line measurement and control of quality characteristics is where it belongs – with the people who make the product. The Quality organization is there to provide leadership and assistance in the deployment of quality techniques, and to monitor progress.

The Improvement Process

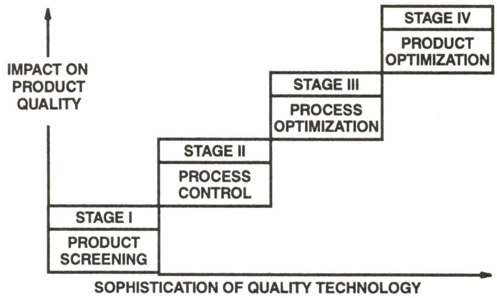


FIGURE 1. STAGES OF STATISTICAL QUALITY TECHNOLOGY

Harris Semiconductor's quality methodology is evolving through the stages shown in Figure 1. In 1981 we embarked on a program to move beyond Stage I, and we are currently in the transition from Stage III to Stage IV, as more and more of our people become involved in quality activities. The traditional "quality" tasks of screening, inspection, and testing are being replaced by more effective and efficient methods, putting new tools into the hands of all employees. Table 1 illustrates how our quality systems are changing to meet today's needs.

ISO 9000 Certification

The manufacturing operations of Harris Semiconductor have all received ISO certification. The ISO 9000 series of standards were very consistent with our goals to build an even stronger quality system foundation.

Designing for Manufacturability

Assuring quality and reliability begins with good product and process design. This has always been a strength in Harris Semiconductor's quality approach. We have a very long lineage of high reliability, high performance products that have resulted from our commitment to design excellence. All Harris products are designed to meet the stringent quality and reliability requirements of the most demanding end equipment applications, from military and space to industrial and telecommunications. The application of new tools and methods has allowed us to continuously upgrade the design process.

Controlling and Improving the Manufacturing Process - SPC/DOX

Statistical process control (SPC) is the basis for quality control and improvement at Harris Semiconductor. Harris manufacturing people use control charts to determine the normal variabilities in processes, materials, and products. Critical process variables and performance characteristics are measured and control limits are plotted on the control charts. Appropriate action is taken if the charts show that an operation is outside the process control limits or indicates a nonrandom pattern inside the limits. These same control charts are powerful tools for use in reducing variations in processing, materials, and products.

SPC is important, but still considered only part of the solution. Processes which operate in statistical control are not always capable of meeting engineering requirements. The conventional way of dealing with this in the semiconductor industry has been to implement 100% screening or inspection steps to remove defects, but these techniques are insufficient to meet today's demands for the highest reliability and perfect quality performance.

Harris still uses screening and inspection to "grade" products and to satisfy specific customer requirements for burn-in, multiple temperature test insertions, environmental screening, and visual inspection as value-added testing options. However, inspection and screening are limited in their ability to reduce product defects to the levels expected by today's buyers. In addition, screening and inspection have an associated expense, which raises product cost (see Table 1).

TABLE 1. APPROACH AND IMPACT OF STATISTICAL QUALITY TECHNOLOGY

STAGE		APPROACH	IMPACT
I	Product Screening	• Stress and Test • Defective Prediction	• Limited Quality • Costly • After-The-Fact
II	Process Control	• Statistical Process Control • Just-In-Time Manufacturing	• Identifies Variability • Reduces Costs • Real Time
III	Process Optimization	• Design of Experiments • Process Simulation	• Minimizes Variability • Before-The-Fact
IV	Product Optimization	• Design for Producibility • Product Simulation	• Insensitive to Variability • Designed-In Quality • Optimal Results

Harris engineers are, instead, using Design of Experiments (DOX), a scientifically disciplined mechanism for evaluating and implementing improvements in product processes, materials, equipment, and facilities. These improvements are aimed at upgrading process performance by studying the key variables controlling the process, and optimizing the procedures or design to yield the best result. This approach is a more time-consuming method of achieving quality perfection, but a better product results from the efforts, and the basic causes of product nonconformance can be eliminated.

SPC, DOX, and design for manufacturability, coupled with our 100% test flows, combine in a product assurance program that delivers the quality and reliability performance demanded for today and for the future.

Average Outgoing Quality (AOQ)

Average Outgoing Quality is a yardstick for our success in quality manufacturing. The average outgoing electrical defective is determined by randomly sampling units from each lot and is measured in parts per million (PPM). The current procedures and sampling plans outlined in ANSI/ASQC Z1.4, MIL-STD-883 and MIL-PRF-38535 are used by our quality inspectors.

The focus on this quality parameter has resulted in a continuous improvement to less than 100 PPM, and the goal is to continue improvement toward 0 PPM.

Training

The basis of a successful transition from conventional quality programs to more effective, total involvement is training. Extensive training of personnel involved in product manufacturing began in 1984 at Harris, with a comprehensive development program in statistical methods. Using the resources of Harris statisticians, private consultants, and internally developed programs, training of engineers, facilitators, and operators/technicians has been an ongoing activity in Harris Semiconductor.

Over the past years, Harris has also deployed a comprehensive training program for hourly operators and facilitators in job requirements and functional skills. All hourly manufacturing employees participate (see Table 2).

Incoming Materials

Improving the quality and reducing the variability of critical incoming materials is essential to product quality enhancement, yield improvement, and cost control. With the use of statistical techniques, the influence of materials on manufacturing is highly measurable. Current measurements indicate that results are best achieved when materials feeding a statistically controlled manufacturing line have also been produced by statistically controlled vendor processes.

To assure optimum quality of all incoming materials, Harris has initiated an aggressive program, linking key suppliers with our manufacturing lines. This user-supplier network is the Harris Vendor Certification process by which strategic vendors, who have performance histories of the highest quality, participate with Harris in a lined network; the vendor's factory acts as if it were a beginning of the Harris production line.

TABLE 2. SUMMARY OF TRAINING PROGRAMS

COURSE	AUDIENCE	TOPICS COVERED
SPC, Basic	Manufacturing Operators, Non-Manufacturing Personnel	Harris Philosophy of SPC, Statistical Definitions, Statistical Calculations, Problem Analysis Tools, Graphing Techniques, Control Charts
SPC, Intermediate	Manufacturing Supervisors, Technicians	Harris Philosophy of SPC, Statistical Definitions, Statistical Calculations, Problem Analysis Tools, Graphing Techniques, Control Charts, Distributions, Measurement Process Evaluation, Introduction to Capability
SPC, Advanced	Manufacturing Engineers, Manufacturing Managers	Harris Philosophy of SPC, Statistical Definitions, Statistical Calculations, Problem Analysis Tools, Graphing Techniques, Control Charts, Distributions, Measurement Process Evaluation, Advanced Control Charts, Variance Component Analysis, Capability Analysis
Design of Experiments (DOX)	Engineers, Managers	Factorial and Fractional Designs, Blocking Designs, Nested Models, Analysis of Variance, Normal Probability Plots, Statistical Intervals, Variance Component Analysis, Multiple Comparison Procedures, Hypothesis Testing, Model Assumptions/Diagnostics
Regression	Engineers, Managers	Simple Linear Regression, Multiple Regression, Coefficient Interval Estimation, Diagnostic Tools, Variable Selection Techniques
Response Surface Methods (RSM)	Engineers, Managers	Steepest Ascent Methods, Second Order Models, Central Composite Designs, Contour Plots, Box-Behnken Designs
Capability Studies	Techs, Facilitators, Engineers	Capability Indices (C_P and C_{PK}), Variance Components, Nested Models, Fixed and Random Effects

SPC seminars, development of open working relationships, understanding of Harris's manufacturing needs and vendor capabilities, and continual improvement programs are all part of the certification process. The sole use of engineering limits no longer is the only quantitative requirement of incoming materials. Specified requirements include centered means, statistical control limits, and the requirement that vendors deliver their products from their own statistically evaluated, in-control manufacturing processes.

In addition to the certification process, Harris has worked to promote improved quality in the performance of all our qualified vendors who must meet rigorous incoming inspection criteria.

Calibration Laboratory

Another important resource in the product assurance system is a calibration lab in each Harris Semiconductor operation site. These labs are responsible for calibrating the electronic, electrical, electro/mechanical, and optical equipment used in both production and engineering areas. The accuracy of instruments used at Harris is traceable to a national standards. Each lab maintains a system which conforms to the current revision of ANSI/NCSL Z540-1.

Each instrument requiring calibration is assigned a calibration interval based upon stability, purpose, and degree of use. The equipment is labeled with an identification tag on which is specified both the date of the last calibration and of the next required calibration. The Calibration Lab reports on a regular basis to each user department. Equipment out of calibration is taken out of service until calibration is performed. The Quality organization performs periodic audits to assure proper control in the using areas. Statistical procedures are used where applicable in the calibration process.

Manufacturing Science - CAM, JIT, TPM

In addition to SPC and DOX as key tools to control the product and processes, Harris is deploying other management mechanisms in the factory. On first examination, these tools appear to be directed more at schedules and capacity. However, they have a significant impact on quality results.

Computer Aided Manufacturing (CAM)

CAM is a computer based inventory and productivity management tool which allows personnel to quickly identify production line problems and take corrective action. In addition, CAM improves scheduling and allows Harris to more quickly respond to changing customer requirements and aids in managing work in process (WIP) and inventories.

The use of CAM has resulted in significant improvements in many areas. Better wafer lot tracking has facilitated a number of process improvements by correlating yields to process variables. In several places CAM has greatly improved capacity utilization through better planning and scheduling. Queues have been reduced and cycle times have been shortened - in some cases by as much as a factor of 2.

The most dramatic benefit has been the reduction of WIP inventory levels, in one area by 500%. This results in fewer lots in the area and a resulting quality improvement. In wafer

fab, defect rates are lower because wafers spend less time in production areas awaiting processing. Lower inventory also improves morale and brings a more orderly flow to the area. CAM facilitates all of these advantages.

Just In Time (JIT)

The major focus of JIT is cycle time reduction and linear production. Significant improvements in these areas result in large benefits to the customer. JIT is a part of the Total Quality Management philosophy at Harris and includes Employee Involvement, Total Quality Control, and the total elimination of waste.

Some key JIT methods used for improvement are sequence of events analysis for the elimination of non-value added activities, demand/pull to improve production flow, TQC check points and Employee Involvement Teams using root cause analysis for problem solving.

JIT implementations at Harris Semiconductor have resulted in significant improvements in cycle time and linearity. The benefits from these improvements are better on time delivery, improved yield, and a more cost effective operation.

JIT, SPC, and TPM are complementary methodologies and used in conjunction with each other create a very powerful force for manufacturing improvement.

Total Productive Maintenance (TPM)

TPM or Total Productive Maintenance is a specific methodology which utilizes a definite set of principles and tools focusing on the improvement of equipment utilization. It focuses on the total elimination of the six major losses which are equipment failures, setup and adjustment, idling and minor stoppages, reduced speed, process defects, and reduced yield. A key measure of progress within TPM is the overall equipment effectiveness which indicates what percentage of the time is a particular equipment producing good parts. The basic TPM principles focus on maximum equipment utilization, autonomous maintenance, cross functional team involvement, and zero defects. There are some key tools within the TPM technical set which have proven to be very powerful to solve long standing problems. They are initial clean, P-M analysis, condition based maintenance, and quality maintenance.

Utilization of TPM has shown significant increases in utilization on many tools across the Sector and is rapidly becoming widespread and recognized as a very valuable tool to improve manufacturing competitiveness.

The major benefits of TPM are capital avoidance, reduced costs, increased capability, and increased quality. It is also very compatible with SPC techniques since SPC is a good stepping stone to TPM implementation and it is in turn a good stepping stone to JIT because a high overall equipment effectiveness guarantees the equipment to be available and operational at the right time as demanded by JIT.

Harris Reliability

Introduction

At Harris Semiconductor, reliability is built into every product by emphasizing quality throughout manufacturing. This starts by ensuring the excellence of the design, layout, and manufacturing processes. The quality of the raw materials and workmanship is monitored using statistical process control (SPC) to preserve the reliability of the product. The primary and ultimate goal of these efforts is to provide full performance to the product specification throughout its useful life.

Reliability Engineering

The Reliability Engineering department is responsible for all aspects of reliability assurance at Harris Semiconductor:

- Charter
  - To ensure that Harris is recognized by our customers and competitors as a company that consistently delivers products with high reliability.

- Mission
  - To develop systems for assessing, enhancing, and assuring that quality and reliability are integrated into all aspects of our business.

- Vision
  - To establish excellence and integrity through all design and manufacturing processes as it relates to quality and reliability.

Values

- To be considered responsive and service oriented by our customers.
- To be acknowledged by Harris as a highly qualified resource for reliability assurance, product analysis, and electronic materials characterization.
- To successfully utilize the organization's talents through trained, empowered employees/employee team participation.
- To maintain an attitude of integrity, dignity and respect for all.

Strategy

- To provide quantitative assessments of product reliability focusing on the identification and timely elimination of design and processing deficiencies that degrade product performance and operating life expectancy.
- To provide systems for continuous improvement of reliability and quality through the assessment of existing processes, products, and packages.
- To perform product analysis as a means of problem solving and feedback to our customers, both internal and external.
- To exercise full authority over the internal qualifications of new products, processes, and packages.

The reliability organization is comprised of a team that possesses a broad cross section of expertise in these areas:

- Custom Military (Radiation Hardened)
- Automotive ASICs
- Harsh Environment Plastic Packaging
- Advanced Methods for Design for Reliability (DFR)
- Strength in Power Semiconductor
- Chemical/Surface Analysis Capabilities
- Failure Analysis Capabilities

The reliability focus is customer satisfaction (external and internal) and is accomplished through the development of standards, performance metrics, and service systems. These major systems are summarized below:

- A process and product development system known as ACT PTM (Applying Concurrent Teams to Product-To-Market) has been established. The ACT PTM philosophy is one of new product development through a team that pursues customer involvement. The team has the authority, responsibility, and training necessary to successfully bring the product to market. This not only includes product definition and design, but also all manufacturing capabilities as well.

- Standard test vehicles (over 100) have been developed for process characterization of wear-out failure mechanisms. These vehicles are used for conventional stresses (for modeling failure rates) and for wafer level reliability characterization during development.

- Common qualification standards have been established for all sites.

- A reliability monitoring system (also known as the Matrix monitoring system) is utilized for products in production to ensure ongoing reliability and verification of continuous improvement.

- The field return system is designed to handle a variety of customer issues in a timely manner. Product issues are often handled by routing the product into the PFAST (Product Failure Analysis Solution Team) system. Return authorizations (RAs) are issued where an entire lot of product needs to be returned to Harris. The Customer Return Services (CRS) group is responsible for the administration of this system (see Customer Return Services.)

- The PFAST system has been established to expedite failure analysis, failure root cause determination, and corrective actions for field returns. PFAST is a team effort involving many functional areas at all Harris sites. The purpose of this system is to enable Harris's Field Sales and Quality operations to properly route, track, and respond to our customer's needs as they relate to product analysis.

Design for Reliability (Wear-Out Characterization)

The concept of "Design for Reliability" focuses on moving reliability assessment away from tests on sample product to a point much earlier in the design cycle. Effort is directed at building in and verifying the reliability of a new process well before manufacture of the first shippable product that uses that technology. This gives these first new products a higher probability of success and achieves reduced product-to-market cycle times.

In practice, a set of standardized test vehicles containing special test structures are transferred to the new process using the layout ground rules specified for that process. Each test structure is designed for a specific wear-out failure mechanism. Highly accelerated stress tests are performed on these structures and the results can be extrapolated to customer use conditions. Generally, lognormal statistics are used to define wear-out distributions for the life prediction models. The results are used to establish reliability design ground rules and critical node lists for each process. These ground rules and critical nodes ensure that wear-out failures do not occur during the customer's projected use of the product.

Process/Product/Package Qualifications

Once the new process has successfully completed wear-out characterization, the final qualification consists of more conventional testing (e.g. biased life, storage life, temp cycle etc.). These tests are performed on the first new product designs (sampled across multiple wafer production lots). Successful completion of the final qualification tests concurrently qualifies the new process and the new products that were used in the qualification. Subsequent products designed within the now-established ground rules are qualified individually prior to introduction. New package configurations are also qualified individually prior to being available for use with new products.

Harris's qualification procedures are specified via controlled documentation and the same standard is used at Harris's sites worldwide.

Product/Package Reliability Monitors

Many of the accelerated stress-tests used during initial reliability qualification are also employed during the routine monitoring of standard product. Any failures occurring on the monitors are fully analyzed and the failure mechanisms identified, with containment and corrective actions obtained from Manufacturing and Engineering. This information along with all of the test results are routinely transmitted to a central data base in Reliability Engineering, where failure rate trends are analyzed and tracked on an ongoing basis. These data are used to drive product improvements, to ensure that failure rates are continuously being reduced over time.

Reliability data, including the Matrix Monitor results, can be obtained by contacting your local Harris sales office.

Customer Return Services

Harris places a high priority on resolving customer return issues. The Customer Return Services (CRS) department is responsible for determining the best manner to handle a return issue as illustrated in Figure 2.

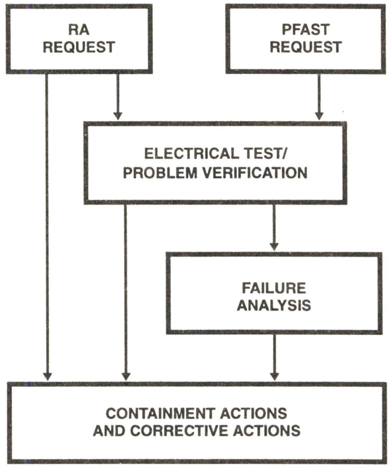


FIGURE 2. GENERAL RETURN FLOW

The diversity of return reasons requires that many different organizations be involved to test, analyze, and correct field return issues. The CRS group coordinates the responses from the supporting organizations to drive closure of issues within the customer response time requirements. The results from the work performed on customer returns are used to initiate corrective actions and continuous improvements within the factories.

The two methods used to return devices are by a RA (Return Authorization) request or by a PFAST (Product Failure Analysis Solution Team) request. The main difference between RA and PFAST is that the PFAST requests often require extensive analysis and a more formal response to the customer. All returns follow the same general procedure from the customer's perspective as seen in steps one to four of the customer return procedure.

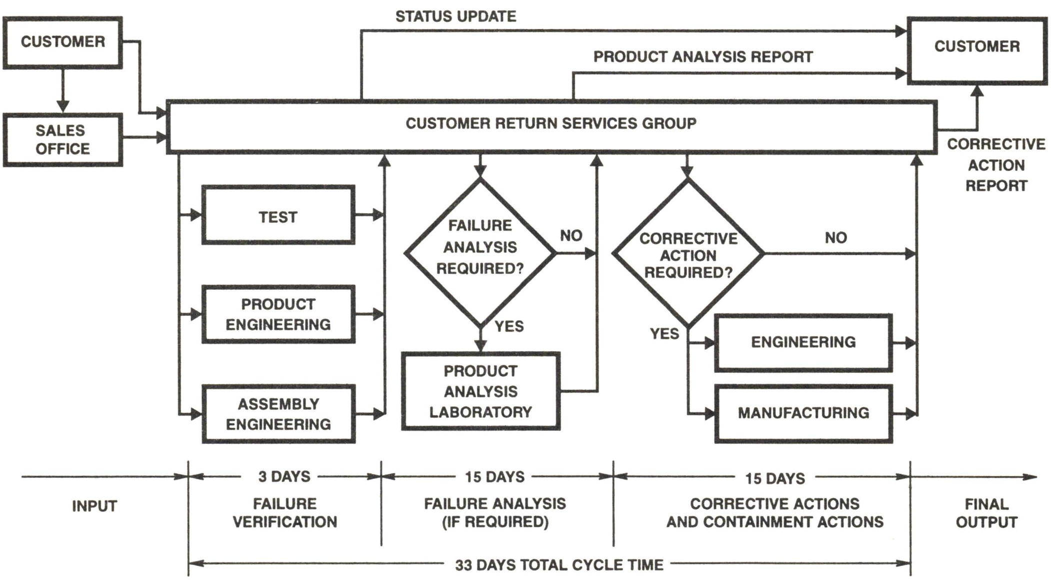
The RA request is used to return and replace an entire lot of product. The lot is returned to Harris for replacement or credit. Once the product is received various tests and evaluations will be performed to determine the appropriate actions that should be taken to resolve any problems or issues.

A PFAST request is used to return a small sample for analysis of a problem. The ultimate outcome of both types of requests is to determine corrective actions that would preclude the same problem occurring in the future. Where appropriate, a containment plan is also implemented to prevent a reoccurrence of the problem in the field. The customer return flow diagram (Figure 3) provides the typical activities and cycle times for processing a PFAST request.

- **Step 1** - Customer or Sales office contacts the Customer Return Services department. If a return is to be routed into the PFAST system, then a PFAST Action Request (see the PFAST form in this section) needs to be completed to understand the customer's issue and direct the analysis efforts.
  - **Phone Number: (407)-724-7400**
  - **FAX Number: (407)-724-7658**
  - **Internet: creturn@harris.com**
  - **PROFS: CRETURN**
- **Step 2** - The Customer Return Services department notifies all affected sales, factory, and engineering organizations of the issue.
- **Step 3** - When product is received, the issue is verified and any required analysis is performed. Where applicable, a preliminary analysis report is sent to the customer.
- **Step 4** - A determination of the root cause of failure initiates the corrective actions to address the source of the problem. A final corrective action report is sent to the customer if requested.

TABLE 3. CUSTOMER RETURN SERVICES

CHARTER	MISSION	RESPONSIBILITIES
To resolve product quality issues while providing feedback to both external and internal customers to facilitate corrective actions and continuous improvement of the product.	To provide a single point interface between the customer and the factory for resolving technical problems, issues, and field returns.	1. Maintain customer return history. 2. Track returns through the factory. 3. Establish a history library of problems and corrective actions. 4. Ensure closure with customers.



NOTE: The days indicated are the typical number of 'working days' not calendar days. Analysis difficulty and the nature of the corrective actions may either improve or degrade the total cycle time.

FIGURE 3. CUSTOMER RETURN FLOW DIAGRAM

HARRIS SEMICONDUCTOR

PFAST ACTION REQUEST

(Product Failure Analysis Solution Team)

Request # ____________

Date: ____________

Originator ____________	Customer ____________
Company/Phone No. ____________	Location ____________
Device Type/Part No. ____________	Customer's Reference No. ____________
No. Samples Returned ____________	Quantity Received ____________

Instructions and requirements are on the back of this form.

Has Field Applications been contacted for assistance? ☐ No ☐ Yes - Who was contacted ____________

SOURCE OF PROBLEM

(Enter the sequence of events in the boxes provided)

1. Visual/Mechanical
   ☐ Describe ____________
2. Incoming Test ☐ Not Performed
   ☐ 100% Tested ☐ Sample Tested
   No. Tested _______ No. of Rejects _______
   Are results representative of previous lots?
   ☐ YES ☐ NO
3. In Process/Manufacturing Failure
   ☐ Board Test ☐ System Test
   How many units failed? ________
   Failed after ________hours of testing
   Was unit retested at incoming inspection?
   ☐ YES ☐ NO
   Are results representative of previous lots?
   ☐ YES ☐ NO
4. Field Failure
   Failed after ________hours operation
   Estimated failure rate________ % per _______
   End User______________ Location ___________
   Min. _____°C Ave. _______°C Max. _______°C
5. Other

ACTION REQUESTED BY CUSTOMER

Specific Action Requested (Contact PFAST Coordinator for other options)

☐ Test Sample for Correlation Only
☐ Test Sample for Product Return >$5k
☐ Failure Analysis
☐ Other

Impact of Failed Units on Customer's Situation: ___________

Customer Contact with Specific Knowledge of Rejects
Name ____________
Position ______________ Phone______________

REASON FOR ELECTRICAL REJECT

(Where appropriate serialize units and specify for each)

Test Conditions Relating to Failure
Tester Used (Mfgr/Model) ____________
Test Temperature ____________
Test Time ☐ Continuous (T = ______sec)
☐ One Shot (T = _______sec)
Describe any observed condition to which failure appears sensitive ____________

1. ☐ DC Failure
   ☐ Open ☐ Short ☐ Leakage
   ☐ Power Drain ☐ Input Level ☐ Output Level
   Pin Number____________
2. ☐ AC Failure
   Power Supply Voltages = ______V
   Input Voltages V_{IH} = _______V V_{IL} = _______V
   Pin Number________
   Failing characteristics ____________
3. ☐ RAM and ROM Failures (ROM failures must be returned with a good master unit if failure analysis is requested).
   Address of Failing Location ____________
   Describe Pattern Used (If not standard patterns, give very complete description including address sequence). ____________

Include timing diagrams and circuit schematic if available.
ROM Programmer Used (If purchased unprogrammed) ____________

Conformal Coating (Mfgr/Model) ____________

Additional Comments:

FIGURE 4. PFAST ACTION REQUEST

INSTRUCTIONS FOR COMPLETING PFAST ACTION REQUEST FORM

The purpose of this form is to help us provide you with a more accurate, complete, and timely response to failures which may occur. Accurate and complete information is essential to ensure that the appropriate corrective action can be implemented. Due to this need for accurate and complete information, requests without a completed PFAST Action Request form will be returned.

Source of Problem:

This section requests the product flow leading to the failure. Mark an 'X' in the appropriate boxes up to and including the step which detected the failure. Also mark an 'X' in the appropriate box under "ARE RESULTS REPRESENTATIVE OF PREVIOUS LOTS?" to indicate whether this is a rare failure or a repeated problem.

Example 1. No incoming electrical test was performed; the units were installed onto boards; the boards functioned correctly for two hours and then 1 unit failed. The customer rarely has a failure due to the Harris device.

SOURCE OF PROBLEM
(Enter the sequence of events in the boxes provided)

1. VISUAL/MECHANICAL
   ☐ DESCRIBE ____________
2. INCOMING TEST ☒ NOT PERFORMED
   ☐ 100% TESTED ☐ SAMPLE TESTED
   NO. TESTED ______ NO. OF REJECTS ______
   ARE RESULTS REPRESENTATIVE OF PREVIOUS LOTS?
   ☐ YES ☐ NO
3. IN PROCESS/MANUFACTURING FAILURE
   ☒ BOARD TEST ☐ SYSTEM TEST
   HOW MANY UNITS FAILED? 1
   FAILED AFTER 2 HOURS OF TESTING
   WAS UNIT RETESTED AT INCOMING INSPECTION?
   ☐ YES ☒ NO
   ARE RESULTS REPRESENTATIVE OF PREVIOUS LOTS?
   ☐ YES ☒ NO
4. FIELD FAILURE
   FAILED AFTER ______ HOURS OPERATION
   ESTIMATED FAILURE RATE ______% PER ______
   END USER ______ LOCATION ______
   MIN. ____°C AVE. ____°C MAX. ____°C
5. OTHER ____________

Example 2. 100 out of the 500 units shipped were tested at incoming and all passed. The units were installed into boards and the boards passed. The boards were installed into the system and the system failed immediately when turned on. There were 3 system failures due to this part. The customer frequently has failures of this Harris device. The 3 units were not retested at incoming.

SOURCE OF PROBLEM
(Enter the sequence of events in the boxes provided)

1. VISUAL/MECHANICAL
   ☐ DESCRIBE ____________
2. INCOMING TEST ☐ NOT PERFORMED
   ☐ 100% TESTED ☒ SAMPLE TESTED
   NO. TESTED 100 NO. OF REJECTS 0
   ARE RESULTS REPRESENTATIVE OF PREVIOUS LOTS?
   ☒ YES ☐ NO
3. IN PROCESS/MANUFACTURING FAILURE
   ☒ BOARD TEST ☒ SYSTEM TEST
   HOW MANY UNITS FAILED? 3
   FAILED AFTER 0 HOURS OF TESTING
   WAS UNIT RETESTED AT INCOMING INSPECTION?
   ☐ YES ☒ NO
   ARE RESULTS REPRESENTATIVE OF PREVIOUS LOTS?
   ☒ YES ☐ NO
4. FIELD FAILURE
   FAILED AFTER ______ HOURS OPERATION
   ESTIMATED FAILURE RATE ______% PER ______
   END USER ______ LOCATION ______
   MIN. ____°C AVE. ____°C MAX. ____°C
5. OTHER ____________

Action Requested by Customer:

This section should be completed with the customer's expectations. This information is essential for an appropriate response.

Reason for Electrical Reject:

This section should be completed if the type of failure could be identified. If this information is contained in attached customer correspondence there is no need to transpose onto the PFAST Action Request form.

PFAST REQUIREMENTS

The value of returning failing products is in the corrective actions that are generated. Failure to meet the following requirements can cause erroneous conclusion and corrective action; therefore, failure to meet these requirements will result in the request being returned. Contact the local PFAST Coordinator if you have any questions.

Units with conformal coating should include the coating manufacturer and model. This is requested since the coating must be removed in order to perform electrical and hermeticity testing.

1. Units must be returned with proper ESD protection (ESD-safe shipping tubes within shielding box/bag or inserted into conductive foam within shielding box/bag). No tape, paper bags, or plastic bags should be used. This requirement ensures that the devices are not damaged during shipment back to Harris.
2. Units must be intact (lid not removed and at least part of each package lead present). This is a requirement since the parts must be intact in order to perform electrical test. Also, opening the package can remove evidence of the cause of failure and lead to an incorrect conclusion.
3. Programmable parts (ROMs, PROMs, UVEPROMs, and EEPROMs) must include a master unit with the same pattern. This requirement is to provide the pattern so all failing locations can be identified. A master unit is required if a failure analysis is requested.

FIGURE 4. PFAST ACTION REQUEST (Continued)

Product Analysis Lab

The Product Analysis Laboratory capabilities and charter encompass the isolation and identification of failure modes and mechanisms, preparing comprehensive technical reports, and assigning appropriate corrective actions. The primary activities of the Product Analysis Lab are electrical verification/characterization of the failure, package inspection/analysis, die inspection/analysis, and circuit isolation/probing. A variety of tools and techniques have been developed to ensure the accuracy and integrity of the product analysis. This section lists some of the tools and techniques that are employed during a typical analysis.

The electrical verification/characterization of devices failing electrical parameters is essential prior to performing an analysis. The information obtained from the electrical verification provides a direction for the analysis efforts. The following electrical verification/characterization equipment may be used to obtain electrical data on a device:

- HP82000M Mixed Signal Tester
- LV500 ASIC verification system
- LTS2020 Analog tester
- Curve Tracer
- Parametric Analyzer

Prior to die level analysis, package inspection and analysis are performed. These steps are performed routinely since valuable data may not be obtainable once the package is opened. The package inspection and analysis may require the use of some of the following lab equipment:

- X-Ray
- C-Mode Scanning Acoustic Microscope (C-SAM)
- Optical inspection microscopes
- Package opening tools and techniques

Once the device has been opened, die inspection and analysis can be performed. Depending on the type of failure, several tools and techniques may be used to identify the failure mechanism. Usually the faster and easier to use operations are performed first in an attempt to expedite the analysis. The list of equipment and techniques for performing die inspection and analysis is as follows:

- Optical microscopes
- Liquid crystal
- Emission microscope
- Scanning electron microscopes - SEM

The final step of circuit isolation is ready to be performed when an area of the circuit has been identified as the source of the problem through one of the previous analysis efforts. Circuit analysis is performed using the following probing and isolation tools:

- Mechanical probing
- Laser cutter and isolation
- E-Beam probing
- Cross sectioning and chemical deprocessing

A typical analysis flow is shown in the Figure 5 below. The exact analysis steps and sequence are determined as the situation dictates. For the analysis to be conclusive, it is essential that the failure mechanism correlates to the initial product failure conditions. Some failure mechanisms require elemental and chemical analysis to identify the root cause within the manufacturing process. Elemental and chemical analysis tasks are sent to the Analytical Services Lab for further evaluation.

The results of each analysis are entered into a computer data base. This data base is used to search for specific types of problems, to identify trends, and to verify that the corrective actions were effective.

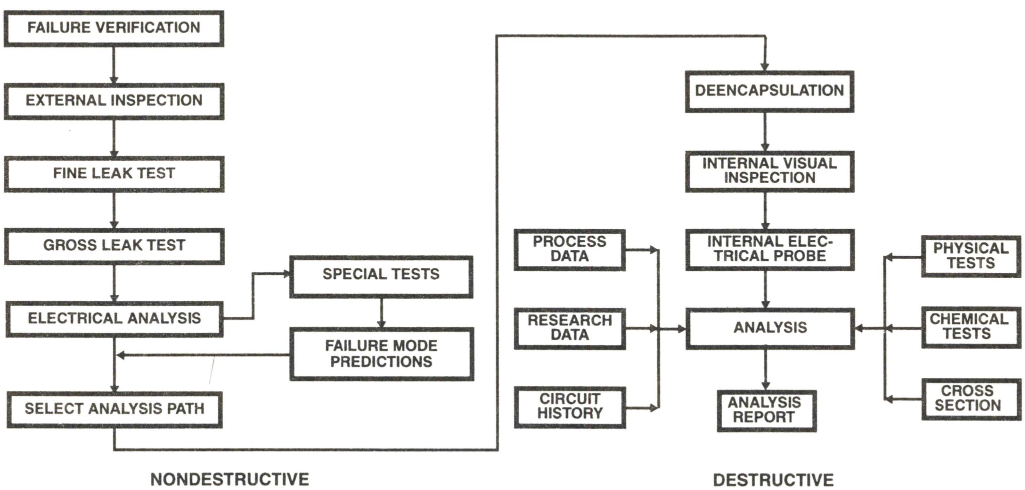


FIGURE 5. ANALYSIS SEQUENCE

Analytical Services Laboratory

Chemical and physical analysis of materials and processes is an integral part of Harris' Total Quality/Continuous Improvement efforts to build reliability into processes and products. Manufacturing operations are supported with real-time analyses to help maintain robust processes. Analyses are run in cooperation with raw material suppliers to help them provide controlled materials in dock-to-stock procurement programs.

Harris facilities, engineering, manufacturing, and product assurance are supported by the Analytical Services Laboratory. Organized into chemical or microbeam analysis methodology, staff and instrumentation from both labs cooperate in fully integrated approaches necessary to complete analytical studies.

The department also maintains ongoing working arrangements with commercial laboratories, universities, and equipment manufacturers to obtain any materials analysis in cases where instrumental capabilities are not available in our own facility. Figure 6 and Figure 7 show the capabilities of each area.

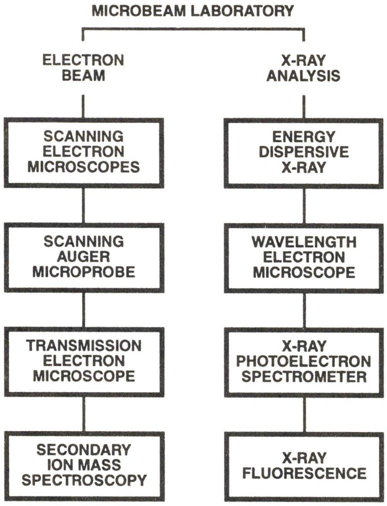


FIGURE 6. MICROBEAM LABORATORY

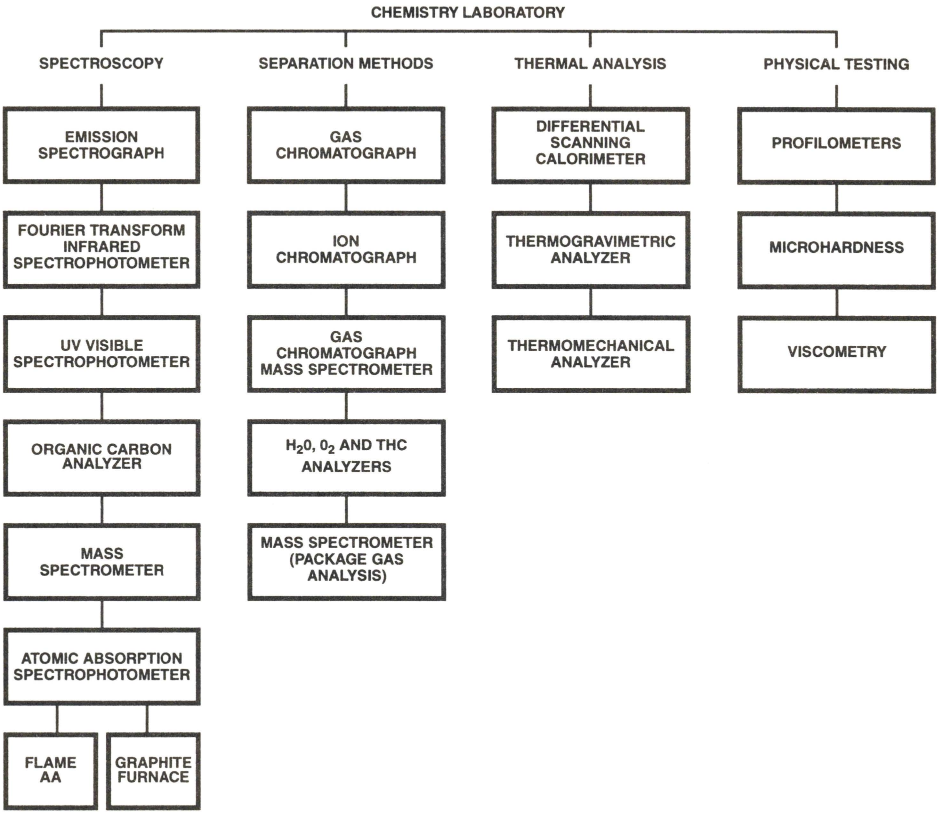


FIGURE 7. CHEMISTRY LABORATORY

Reliability Fundamentals and Calculation of Failure Rate

Table 4 defines some of the more important terminology used in describing the lifetime of integrated circuits. Of prime importance is the concept of "failure rate" and its calculation.

Failure Rate Calculations

Since reliability data can be accumulated from a number of different life tests with several different failure mechanisms, a comprehensive failure rate is desired. The failure rate calculation can be complicated if there are more than one failure mechanism in a life test, since the failure mechanisms are thermally activated at different rates The equation below accounts for these considerations along with a statistical factor to obtain the upper confidence level (UCL) for the resulting failure rate.

$$\lambda = \left[\sum_{i=1}^{\beta} \frac{x_i}{\sum\limits_{j=1}^{k} TDH_j \, AF_{ij}} \right] \times \frac{M \times 10^9}{\sum\limits_{i=1}^{\beta} x_i}$$

where,

λ = failure rate in FITs (Number fails in 10^9 device hours)

β = number of distinct possible failure mechanisms

k = number of life tests being combined

x_i = number of failures for a given failure mechanism $i = 1, 2, \ldots \beta$

TDH_j = Total device hours of test time (unaccelerated) for Life Test j, $j = 1, 2, 3, \ldots k$

AF_{ij} = Acceleration factor for appropriate failure mechanism $i = 1, 2, \ldots k$

M = $X^2_{(\alpha,\, 2r+2)}/2$
where,
X^2 = chi square factor for $2r + 2$ degrees of freedom
r = total number of failures ($\Sigma\, x_i$)
α = risk associated with UCL;
i.e. $\alpha = (100\text{-}UCL(\%))/100$

In the failure rate calculation, Acceleration Factors (AF_{ij}) are used to derate the failure rate from the thermally accelerated life test conditions to a failure rate indicative of actual use temperature. Although no standard exists, a temperature of 55^oC has been popular. Harris Semiconductor Reliability Reports will derate to 55^oC and will express failure rates at 60% UCL. Other derating temperatures and UCLs are available upon request.

TABLE 4. FAILURE RATE PRIMER

TERMS	DEFINITIONS/DESCRIPTION
Failure Rate λ	Measure of failure per unit of time. The early life failure rate is typically higher, decreases slightly, and then becomes relatively constant over time. The onset of wear-out will show an increasing failure rate, which should occur well beyond useful life. The useful life failure rate is based on the exponential life distribution.
FIT (Failure In Time)	Measure of failure rate in 10^9 device hours; e.g., 1 FIT = 1 failure in 10^9 device hours, 100 FITS = 100 failure in 10^9 device hours, etc.
Device Hours	The summation of the number of units in operation multiplied by the time of operation.
MTTF (Mean Time To Failure)	Mean of the life distribution for the population of devices under operation or expected lifetime of an individual, MTTF = $1/\lambda$, which is the time where 63.2% of the population has failed. Example: For λ = 10 FITS (or 10 E-9/Hr.), MTTF = $1/\lambda$ = 100 million hours.
Confidence Level (or Limit)	Probability level at which population failure rate estimates are derived from sample life test: 10 FITs at 95% UCL means that the population failure rate is estimated to be no more that 10 FITs with 95% certainty. The upper limit of the confidence interval is used.
Acceleration Factor (AF)	A constant derived from experimental data which relates the times to failure at two different stresses. The AF allows extrapolation of failure rates from accelerated test conditions to use conditions.

Acceleration Factors

Acceleration factor is determined from the Arrhenius Equation. This equation is used to describe physiochemical reaction rates and has been found to be an appropriate model for expressing the thermal acceleration of semiconductor failure mechanisms.

$$AF = EXP\left[\frac{E_a}{k}\left(\frac{1}{T_{USE}} - \frac{1}{T_{STRESS}}\right)\right]$$

where,

AF = Acceleration Factor

E_a = Thermal Activation Energy (See Table 5)

k = Boltzmann's Constant (8.63×10^{-5} eV/°K)

Both T_{use} and T_{stress} (in degrees Kelvin) include the internal temperature rise of the device and therefore represent the junction temperature.

Activation Energy

The Activation Energy (E_a) of a failure mechanism is determined by performing at least two tests at different levels of stress (temperature and/or voltage). The stresses will provide the time to failure (t_f) for the two (or more) populations thus allowing the simultaneous solution for the activation energy as follows:

$$\ln\ (t_{f1}) = C + \frac{E_a}{kT_1} \qquad \ln\ (t_{f2}) = C + \frac{E_a}{kT_2}$$

By subtracting the two equations and solving for the activation energy, the following equation is obtained:

$$E_a = \frac{k[\ln(t_{f1}) - \ln(t_{f2})]}{(1/T1 - 1/T2)}$$

where,

E_a = Thermal Activation Energy (See Table 5)

k = Boltzmann's Constant (8.63×10^{-5} eV/°K)

T_1, T_2 = Life test temperatures in degrees Kelvin

TABLE 5. FAILURE MECHANISM

FAILURE MECHANISM	ACTIVATION ENERGY	SCREENING AND TESTING METHODOLOGY	CONTROL METHODOLOGY
Oxide Defects	0.3eV - 0.5eV	High temperature operating life (HTOL) and voltage stress. Defect density test vehicles.	Statistical Process Control of oxide parameters, defect density control, and voltage stress testing.
Silicon Defects (Bulk)	0.3eV - 0.5eV	HTOL and voltage stress screens.	Vendor statistical Quality Control programs, and Statistical Process Control on thermal processes.
Corrosion	0.45eV	Highly accelerated stress testing (HAST)	Passivation dopant control, hermetic seal control, improved mold compounds, and product handling.
Assembly Defects	0.5eV - 0.7eV	Temperature cycling, temperature and mechanical shock, and environmental stressing.	Vendor Statistical Quality Control programs, Statistical Process Control of assembly processes, proper handling methods.
Electromigration - Al Line - Contact	 0.6eV 0.9eV	Test vehicle characterizations at highly elevated temperatures.	Design ground rules, wafer process statistical process steps, photoresist, metals and passivation.
Mask Defects/ Photoresist Defects	0.7eV	Mask FAB comparator, print checks, defect density monitor in FAB, voltage stress test and HTOL.	Clean room control, clean mask, pellicles, Statistical Process Control of photoresist/etch processes.
Contamination	1.0eV	C-V stress at oxide/interconnect, wafer FAB device stress test and HTOL.	Statistical Process Control of C-V data, oxide/ interconnect cleans, high integrity glassivation and clean assembly processes.
Charge Injection	1.3eV	HTOL and oxide characterization.	Design ground rules, wafer level Statistical Process Control and critical dimensions for oxides.

TVS 13

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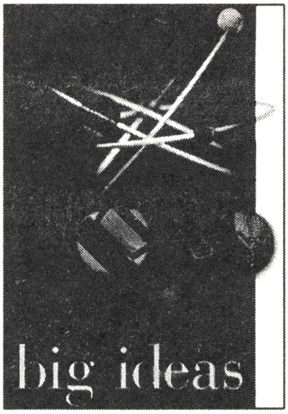

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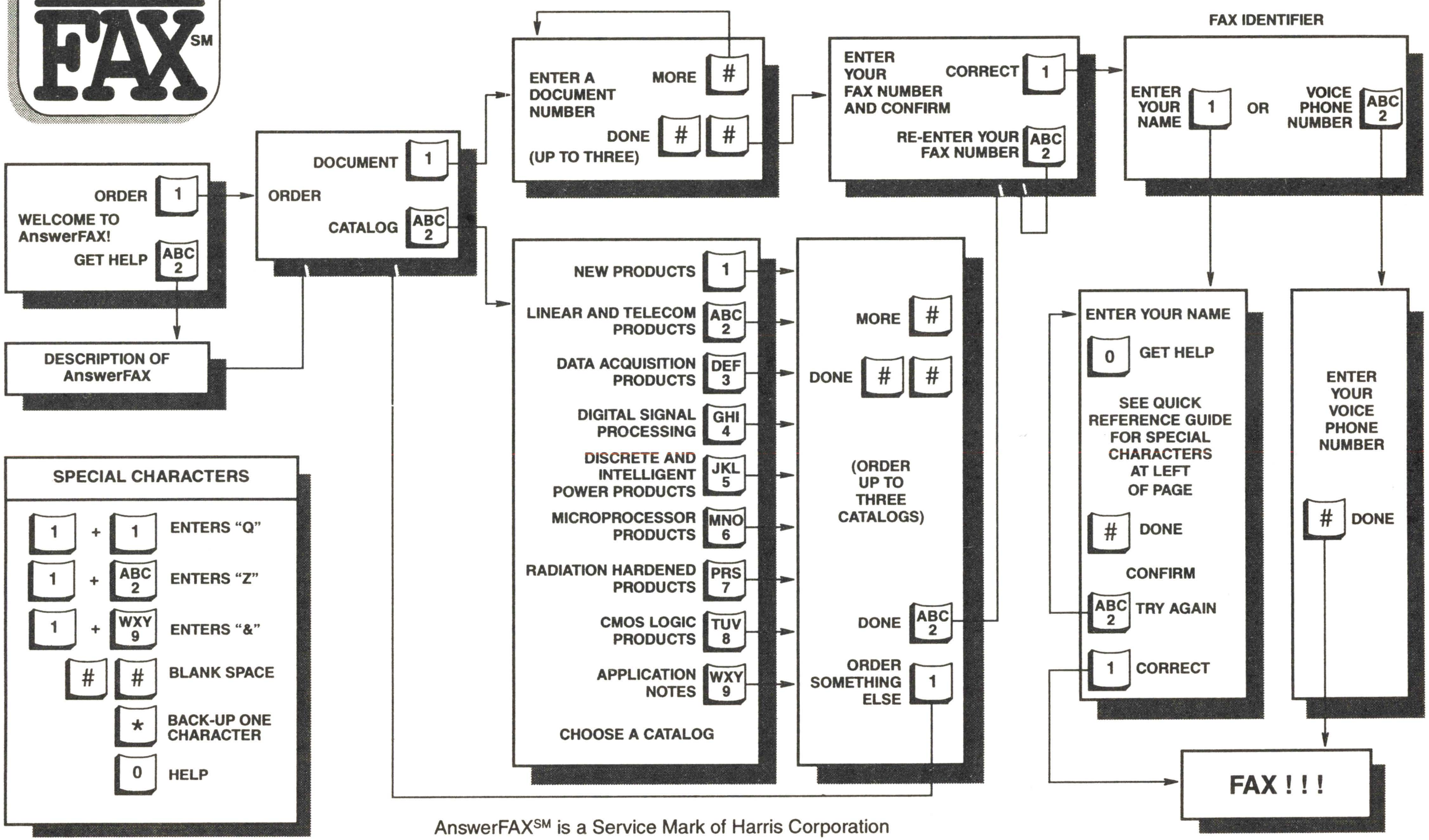

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FAX: 214 265 4668

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Newark Electronics
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TEL: (304) 345-3086

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FAX: 414 782 7921

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Burbank, CA 91504-1052
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Cuidad Del Sol
Zapopan, Jalisco
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Future Electronics DO Brasil LTDA
Rua Luzitant
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13-015-121 Campinas SP
Brazil
TEL: 55-19-232-7052
FAX: 55-19-236-9834

Graftec Brasil Ltda.
Rua Baronesa de Itu,
336 cj. 51/52 Sao Paulo - SP
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7410 Pebble Dr.
Ft. Worth, TX 76118
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Arrow Alliance Group
25 Hub Drive
Melville, NY 11747
TEL: (516) 391-1300

Arrow CMS Distribution Group
1350 McCandless Drive
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TEL: (408) 441-4050

Arrow Semiconductor Group
25 Hub Drive
Melville, NY 11747
TEL: (516) 391-1300

Arrow Supplier Services Group
25 Hub Drive
Melville, NY 11747
TEL: (516) 391-1300

Bell Microproducts
1941 Ringwood Avenue
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TEL: (800) 995-1999
FAX: (408) 451-1600

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7433 Harwin Drive
Houston, TX 77036
TEL: (713) 780-7770
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237 Hymus Blvd.
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FAX: (514) 695-3707

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237 Hymus Blvd.
Pointe Claire, Quebec
Canada, H9R 5C7
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Gerber Electronics
128 Carnegie Row
Norwood, MA 02062
TEL: (617) 769-6000, x156
FAX: 617 762 8931

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H-1134 Budapest
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FAX: 36-1-2706277

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PL-02672 Warszawa
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Arrow Finland
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SF - 00521 Helsinki
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FAX: 358 9 476 663 29

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FAX: 358 9 69 22 32 6

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64714 Michelstadt
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FAX: 30 1 34 14 304

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TEL: 30 1 32 53 626
FAX: 30 1 32 16 063

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Aviv Electronics
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IS - 43100 Ra'anana
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FAX: 972 9 741 6510

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FAX: 39 2 660 170 20

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FAX: 39 51 73 24 91

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FAX: 31 30 603 5924

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EBV Elektronik
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